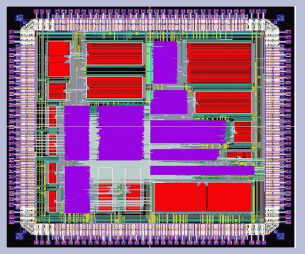
Gaisler Research



LEON3FT GINA Development

Activity Outline

- **Preparation for the development of GINA processor**
  - Requirement analysis
  - Development of a FT multi-core architecture
  - Development of FPGA validation board
  - Adaption of operating systems
  - Verification and validation of both fault-tolerance and multi-processing capabilities
- **9 Months development project**
  - Contract 18533/04/NL/JD, CO3
  - Three work packages
  - Gaisler Research (prime)
  - Pender Electronic Design (board design)

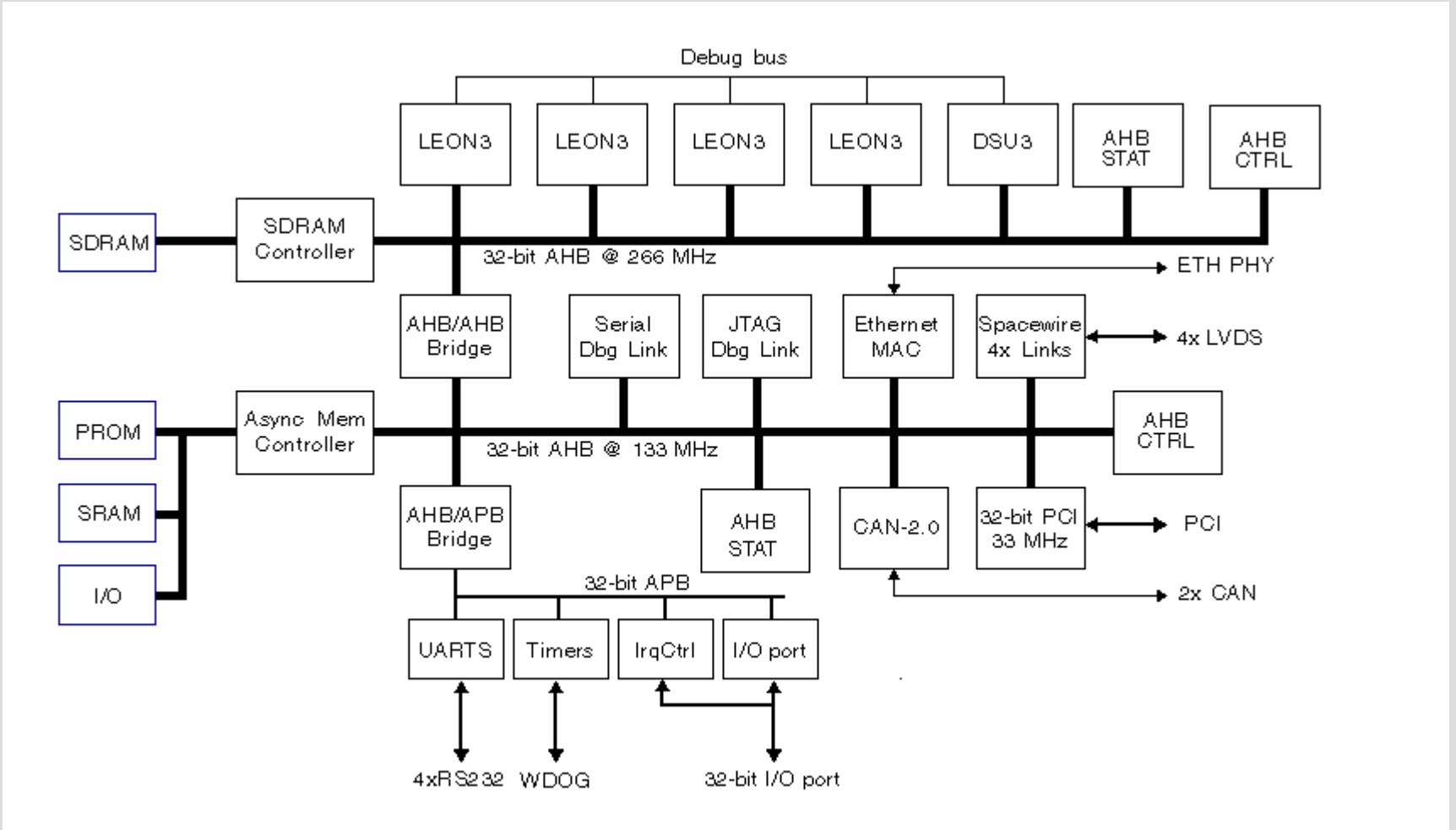
Baseline requirements

- **Hardware**
  - Configurable SOC plaform
  - Fault-tolerance in all cores
  - High-performance processor with MMU/FPU
  - Large range of on-chip interfaces
  - Fully synthesizable and portable to FPGA
- **Software**
  - Multi-processor support in O/S
  - Standard tool-chain

Initial trade-off

- **Architecture based on GRLIP SOC platform**
  - Flexible, configurable, portable
  - Large range of integrated IP cores
  - LEON3FT with MMU and GRFPU
  - Spacewire, CAN, Ethernet SDRAM/DDR
  - Fully synthesizable and portable to FPGA
  - Plug&Play to simplify software porting
- **Software**
  - RTEMS multi-processor extensions
  - eCos shared-memory multi-processor support

GINA Architecture V1



Implementation details

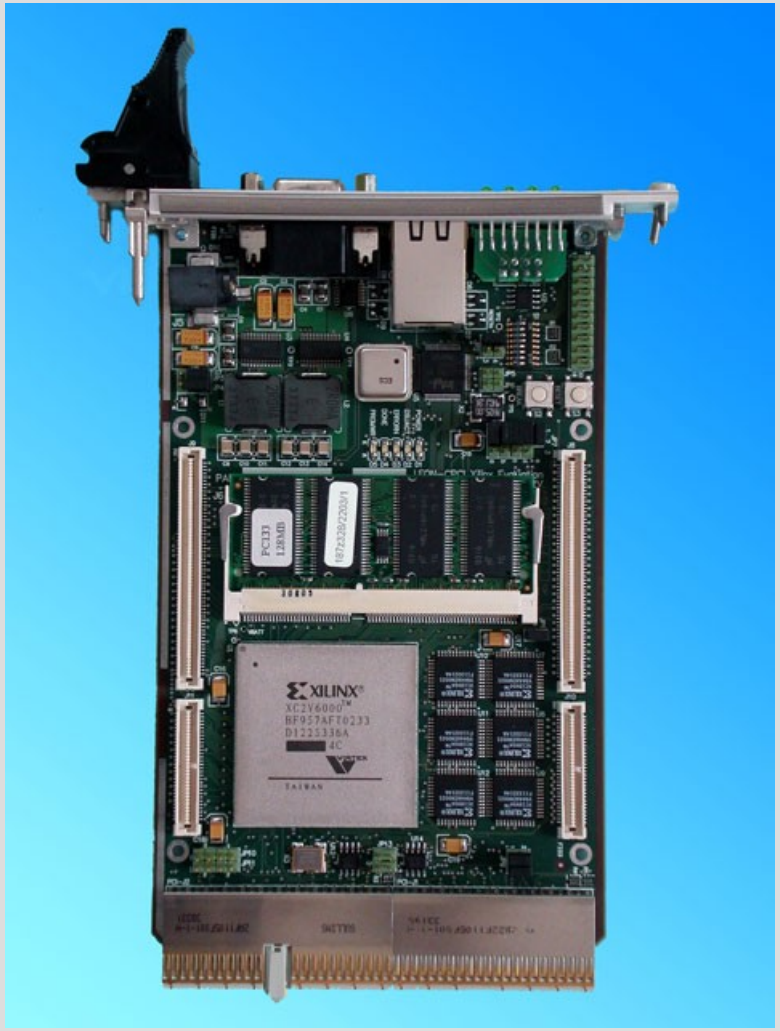
- **Processors**
  - 4x LEON3FT, MMU, GRFPU, 32 Kbyte cache
- **Bus Structure**
  - Dual 32-bit AHB uses, 266/133 MHz
  - Bi-directional AHB/AHB bridge with clock synchroniza-tion and split-transfer support
  - Dual APB buses
- **On-chip peripherals**
  - 4x SpW with RMAP and DMA
  - 2x CAN-2.0, 4x UART
  - 32-bit PCI bridge
  - 10/100 Mbit Ethernet MAC

Software adaptation

- **eCos**
  - Full LEON3 support of SMP
  - Application transparent
  - Task scheduled on available processor nodes
- **RTEMS**
  - LEON3 support for multi-processor extensions
  - Loosely-coupled message passing MP
  - Fixed configuration at link time
- **Verification**
  - Basic development done on GRSIM MP Simulator
  - Final tests performed on real hardware
  - eCos and RTEMS test suites passed with fault-injection

Virtex4-LX200 Validation board

- Xilinx Virtex4 LX200 FPGA
- CPCI form factor
- 16 Mbyte Flash
- 8 Mbyte SRAM with ECC
- 256 Mbyte SDRAM with ECC
- 10/100 Mbit ethernet PHY
- 32/64 bit PCI backplane
- Mezzanine with drivers/conn.
  - 4x Spacewire @ 200 Mbit
  - 2x 1553
  - 2x CAN
  - 4x RS422/RS232



Hardware/Software validation

- **GINA V1 implemented on XC4V-LX200**
  - 4-Processor system @ 30 MHz, 85% utilization
  - Full set of peripherals
  - Full FT in all on-chip cores
- **Software validation**
  - eCos test suite
  - RTEMS SP/MP test suite
  - RTEMS TTCP Network application
  - Various RTEMS/eCos applications (FFT, TS, AOCS)
  - Simultaneous execution of eCos and RTEMS
  - Fault-injection through GRMON during all test
- **Validation fully successful!**

Possible extensions

- **Additional GRLIB cores**
  - 32/64-bit DDR controller
  - 1000 Mbit ethernet MAC, RMII, RGMII
  - USB-2.0 host/device
- **Improved SOC platform**
  - 64-bit AHB bus
  - USB-2.0 host/device
- **New LEON3FT features**
  - 64-bit cache and AHB interface
  - MMU synchronization and bus snooping
  - Dynamic clock gating
- **Software**
  - VxWorks-6.3 with MP support

Summary

- **GINA provides a fast path to 1 GIPS/GFLOPS**
  - 6 months to tape-out
  - Limitation set by availability of semiconductor process
- **GRLIP Plug&Play allows derivate architecture**
  - Simple and secure configuration
  - Software compatibility
  - Adaptive debugging
  - Vendor specific extensions/additions
- **GRLIP Portability allows fast prototyping**
  - Built-in technology mapping API for FPGA/ASIC
  - Source code delivery for end-user adaptation
  - Independent ownership, commercially supported