ESA Round Table 2006 on Next Generation Microprocessors for Space Applications
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GINA: A Multi-Core Approach

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GINA stands for Giga INstruction Architecture

The initial GINA project was first presented in October 2004 to D/TEC
It was then further presented @ the SDSS in October 2005 @ ESTEC Noordwijk
and @ DASIA in July 2006 in Berlin

More Computing Power for Tomorrow Space Applications (1)

The ALRP's LAW for the development of new space processors:

- Because the duration of the development of new space advanced processor is at least 5-6 years
- Because the cost of the development of new space processor is about 6-8 millions Euro

➢ One should not develop a new space processor that has not at least a fivefold performance improvement with respect to the previous generation

More Computing Power for Tomorrow Space Applications (2)

2 MIPS	0.5 MFLOPS
10 MIPS	2.5 MFLOPS
20 MIPS	5 MFLOPS
100 MIPS	25 MFLOPS
1000 MIPS	**1000 MFLOPS**

that are the GINA processor targets

Note: that it will be a tenfold improvement with respect to the previous generation, two times the minimum previously defined, but already we see coming requirements for high end applications in the range of 400-600 MIPS. We have to anticipate future requirements.

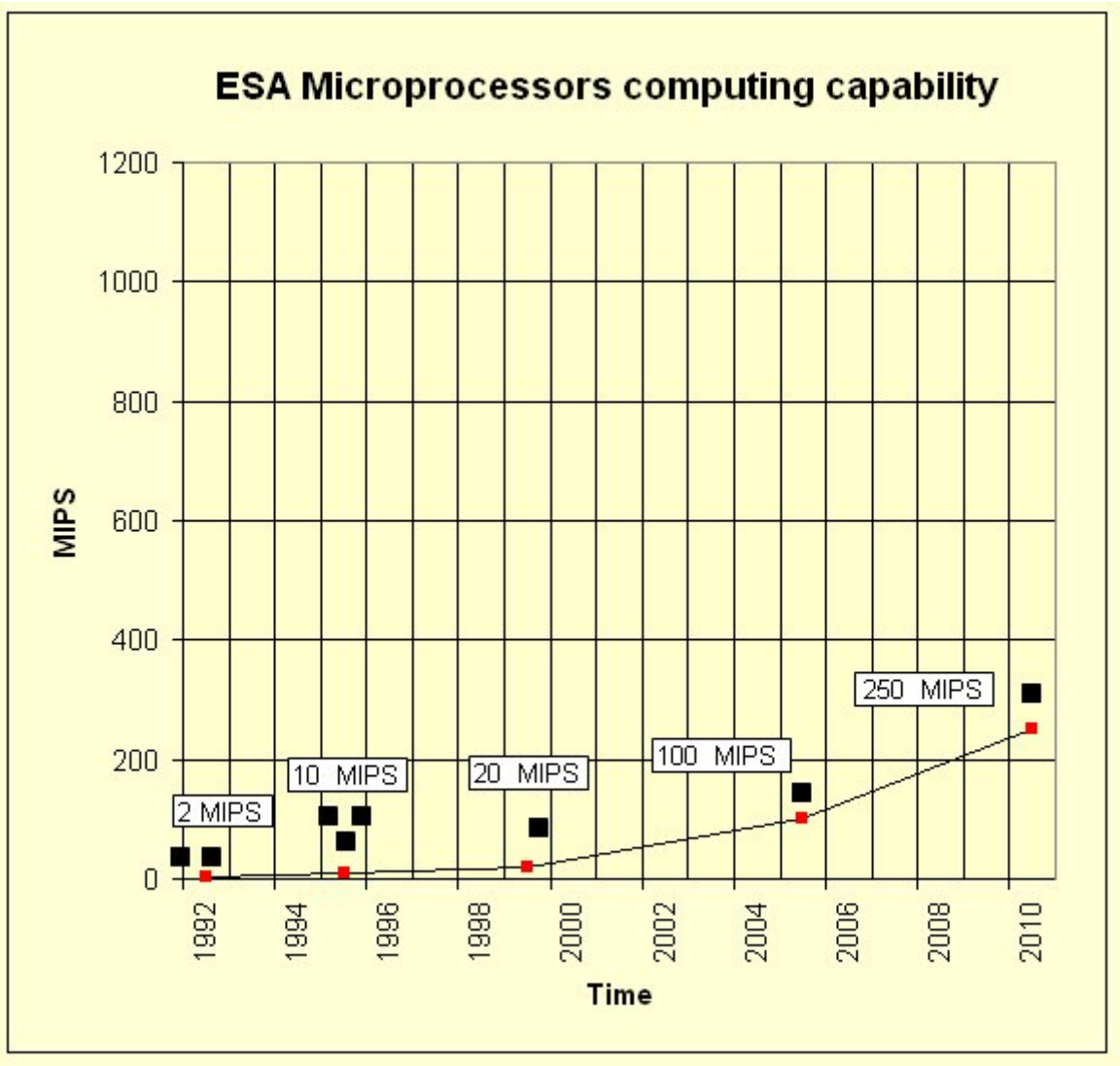
How can we increase the computing power of a microprocessor?

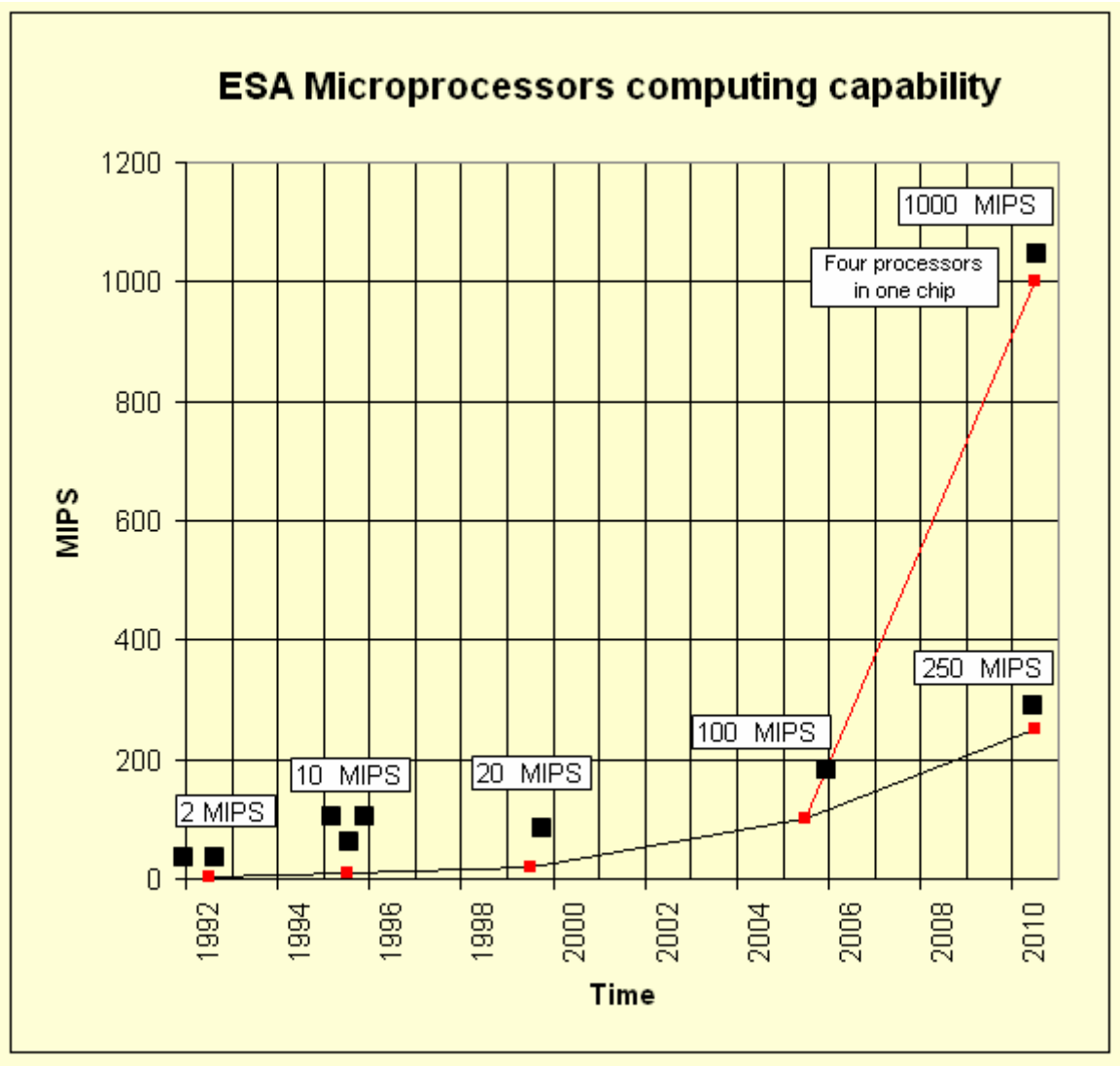
- Increase the clocking speed by using a faster CMOS process (the target frequency is 266 MHz)
- Improve the design: use of the 7-stage pipeline LEON3 IP core (the LEON2 is a 5-stage pipeline) and make use of the faster pipelined GFPU operating in serial mode

➢ *but there is some limitation to the above and at best we will get only a twofold+ improvement in performance with respect to the AT697*

- Make use of more capable system architectural features such as the use of caches (already used in the AT697) and the use of a multi-core architecture

➢ *due to the above clock speed limitation these new system architectural features are a must in order to obtain a significant improvement in performance*


ESA Microprocessors computing capability
MIPS
1200
1000
800
600
400
200
0
2 MIPS
10 MIPS
20 MIPS
100 MIPS
250 MIPS
1992
1994
1996
1998
2000
2002
2004
2006
2008
2010
Time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Four processors in one chip

Can we do it in Europe ?

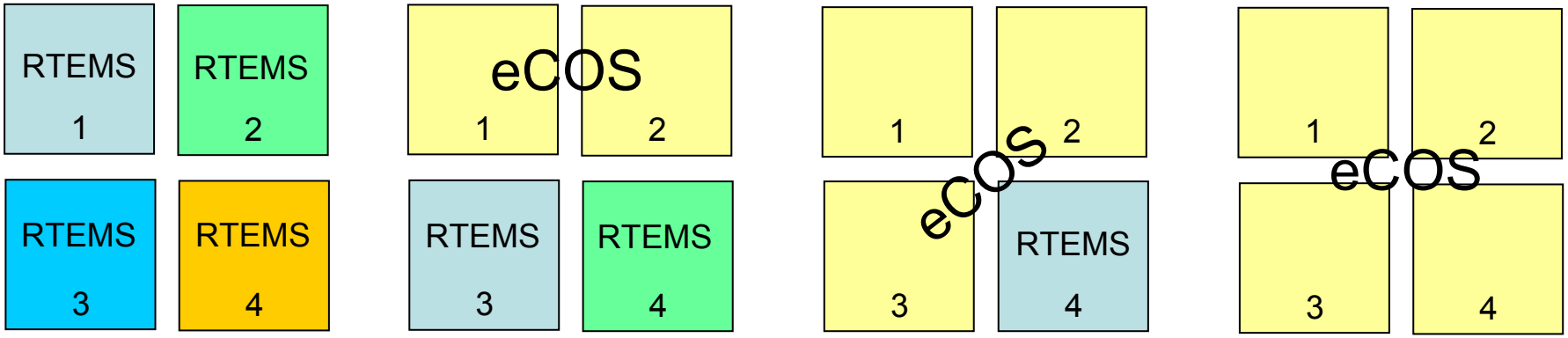
- YES: Europe has the design competence that has been build over the past 15 years with the development of the four previous ESA microprocessors (and we shall maintain that competence !)
- YES: we have performant commercial IP cores available in Europe and they can be adapted for space use
- YES: we have the technology, CMOS processes of 90 nm and 65 nm are available today in Europe

Short preliminary specification for the GINA processor

- Provide 1000 MIPS and 1000 MLOPS computing power
- Clocking speed target of 266 MHz
- Four processors each with caches and FPU in a single device
- The four processors share the same memory space
- The processors shall be SPARC V8 compliant
- It shall be tolerant to SEU induced errors (it shall be software transparent)
- It shall provide a SPARC V8 compliant memory management
- It shall be possible to use each processor individually with its own OS
- It shall support multiprocessing operations
- It shall provide power down mode for each individual processor
- It shall be possible to reset/restart each processor individually
- It shall be possible to debug each processor individually

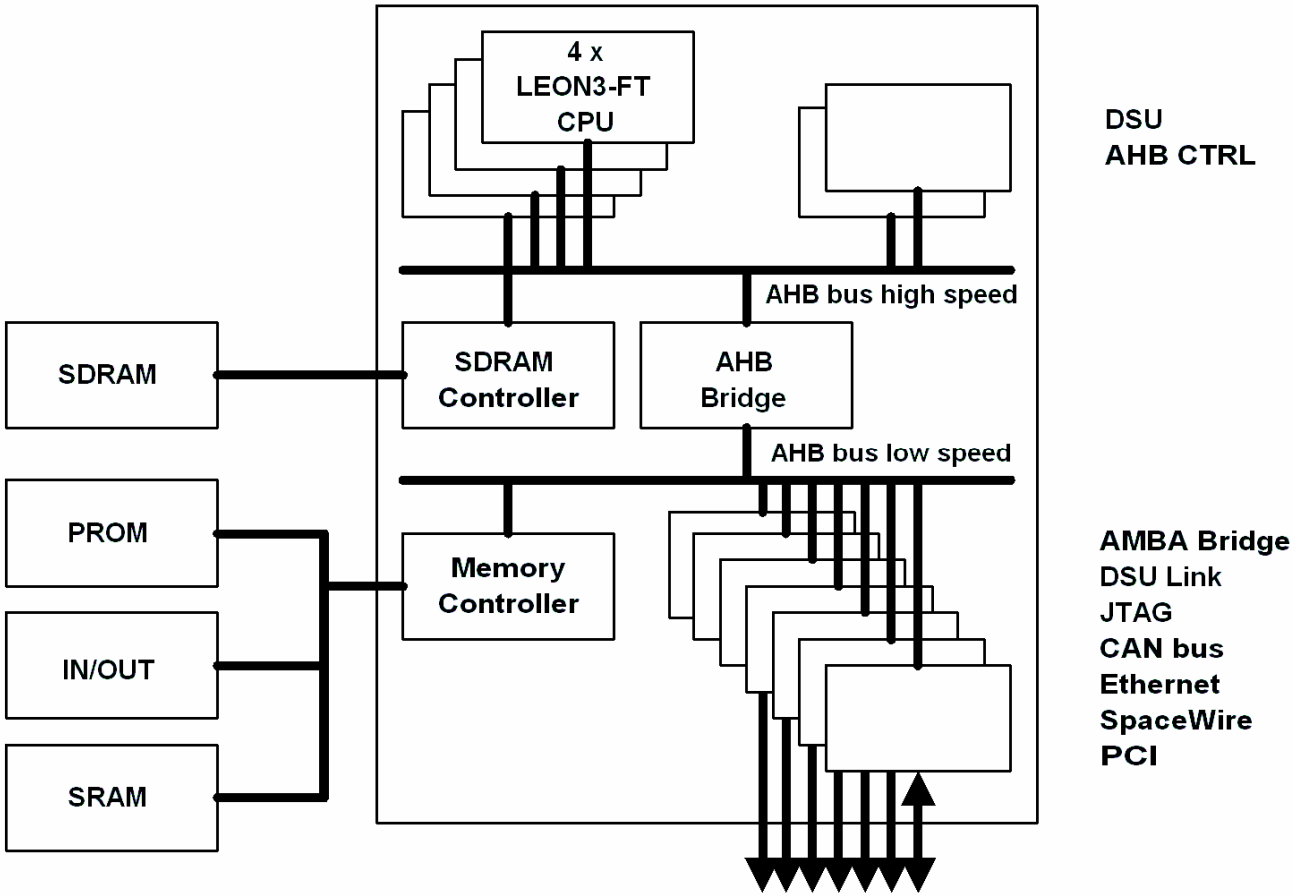
The GINA processor shall be an enabler for new on-board data systems

- It shall provide a flexible use of the processors by offering the possibility to run simultaneously heterogeneous operating systems



- Use the MMU in direct map mode to prevent that the different images may overwrite each others but still maintain the bus snooping capability that is important for the cache coherency in a multiprocessor system
- Other OS will be later available in addition to RTEMS and eCOS

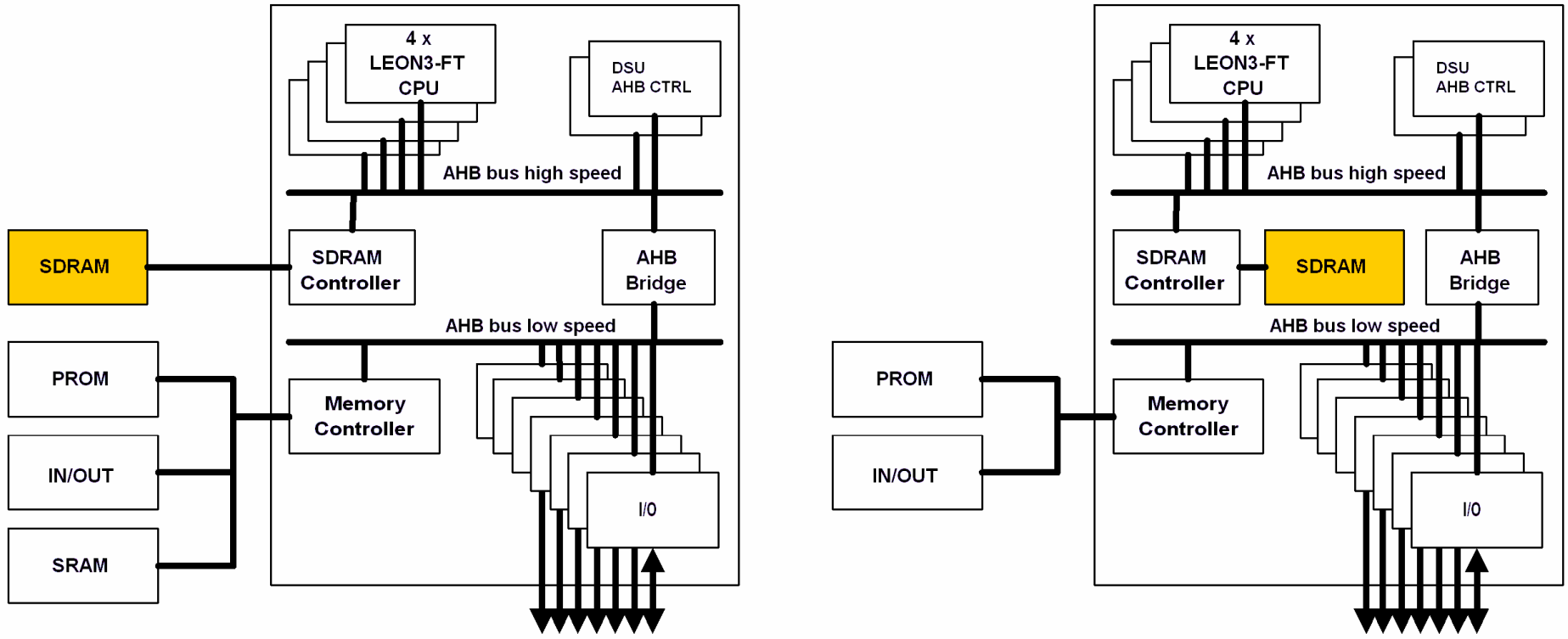
The GINA basic architecture with dual AHB bus



Possible Adaptations and Additions

- Additional hardware to support multiprocessor operation?
- Two-core versus Four-core architecture?
- Moving the SDRAM from Outside to Inside !

Moving the SDRAM from Outside to Inside (1)



Moving the SDRAM from Outside to Inside (2)

- Today there is the possibility to have up to 256 Mb inside the chip,
- When putting 64 Mb (8 MB) in the chip with RS protection the space applications will not require any additional external RAM and SDRAM
- That will result in significant pin saving (more than 80pins)
- That will solve the problem of obsolescence and procurement SDRAM parts
- That will decrease significantly the board area occupation

The software challenge of the GINA processor

- The use of caches in the AT697 (LEON2-FT) was the first challenge for software (such as schedulability analysis or WCET)
- The GINA processor with its multiprocessor architecture will add a very challenging new dimension for the software (on that subject see the presentations of K. Hjortnaes and G. Bretame)

Applications for the GINA processor

- Today processor requirements for space applications range from several MIPS (telecom platform controllers), 10 to 70 MIPS (middle and high performance missions of today and tomorrow), and to several 100 MIPS in the near future
- The GINA processor with its multi-core approach can cover that complete range of requirements without any penalties
- No penalty in power consumption: you have the choice to use one, two, three, or four of cores as needed. The unused cores will go automatically in power saving mode
- It is also possible to decrease the clock frequency of the operating cores when the high computing power is not required saving additional power
- The present estimate for the power consumption is 2-3 W at max frequency
- No penalty in pin count/foot print: the multi-core architecture is sharing the same memory space and there is no need for additional pins for the multi-core
- We target the use of a MCGA 479 package that offers a very small foot print

Package Foot Print

MA31750 Chip Set
2825 mm2
152 leads

MA31750
84-Lead Flatpack
40x40 mm

MA31751
68-Lead Flatpack
35x35 mm

ERC32 Chip Set
5139 mm2
672 leads

TSC691
256-lead MQFP
45x45 mm

TSC692
160-lead
MQFP
33x33 mm

TSC693
256-lead MQFP
45x45 mm

ERC32 Single Set
2025 mm2
256 leads

TSC695
256-lead MQFP
45x45 mm

LEON2-FT
625 mm2
349 columns

TSC697
MCGA 349
25x25 mm

GINA
841 mm2
472/625 columns

GINA
MCGA 472
29x29 mm

NOTE:

ERC32 MQFP packages: 8 mm2 per lead
LEON and GINA MCGA packages: 1.8 mm2 per column

Preliminary development plan for the GINA processor

Four phases have been defined for the development of the GINA processor

Phase 1: Design and Validation of the core elements, the basic architecture, and the supporting Operating Systems

Phase 2: Specification and Architecture Consolidation

Phase 3: Proof of concept on a silicon demonstrator
(may be not using the final target CMOS process)

Phase 4: Product development of the prototype and the flight devices on final target CMOS process

Development of the GINA processor
Phase 1 contract

Definition:	Design and Validation of the core elements, the basic architecture, and the supporting Operating Systems
Contractor:	Gaisler Research (S)
Start date:	September 2005
End date:	March 2006

Development of the GINA processor Phase 1 short tasks description

Work Package 1 Requirements Analysis and Specification

- for SEU tolerance of the IP cores
- multiprocessing support of the IP cores
- multiprocessing support of the Operating Systems (RTEMS and eCOS)

Work Package 2 Design and Verification

- configuration and adaptation of existing IP cores
- adaptation of RTEMS and eCOS to support the multiprocessor configuration
- verification by simulation (functionalities, SEU tolerance and multiprocessor operation)

Work Package 3 System validation on a FPGA board

- validate the system (functionality, SEU tolerance, multiprocessor operation)

Phase 1 Development of the GINA processor

- The four-core and dual AHB bus GINA architecture has been validated
- A FPGA board (XILINX Virtex 4) is available and can be used for further software evaluation on a representative GINA multi-core processor
- The Summary Report is available

More details on the Phase 1 work and results in the following presentation by Gaisler Research

The next ESA Microprocessor Generation

Some questions:

- What microprocessor were you flying 10 years ago?
- What will be your computing requirements in 10 to 15 years from now?

Early spacecrafts were flying the 8-bit RCA1802 and the Fairchild 9450 and today PROBA 2 is going to fly the AT697E

We have to anticipate requirements !

And don't forget:

We have to provide to the European space community a ***guaranteed access*** to a high performance processor for space applications

The next ESA Microprocessor Generation

1000 MIPS

1000 MFLOPS

G I

N A

References

- A Giga INstruction Architecture (GINA) for the future ESA microprocessor based on the LEON3 IP core,
  Paper and presentation @ DASIA 2006 (Berlin),
  by André L. R. Pouponnot (ESA)

- ESA Contract 18533/04/NL/JD, COO3, Development of LEON3-FT-MP, Summary Report,
  by Jiri Gaisler (Gaisler Research)

- Current Trends in Multi-Processor System-on-Chip Development
  Presentation by Giovanni Beltrame (ESA)