



PowerPC- based Processor Modules for Space Applications

Patria Systems OY Jaakko Toivonen

12.09.2006



PowerPC- based Single Board Computers

- Two Single Board Computer (SBC) modules targeted for space applications: PowerCDH and PowerCDH3
- PowerPC selected for performance (MIPS/W), maturity and availability
- PowerCDH:

- Radiation tested PowerPC603R processor
- External interfaces and the amount of on-board memory can be easily tailored for each mission.
- PowerCDH is the basis for MIXS+SIXS instrument DPU for the BepiColombo mission.
- PowerCDH3:
 - PowerPC 7448 (optionally 7447A) processor made with Silicon on Insulator (SOI) technology.
 - The PowerCDH3 development model will be available in Q2/2007.





PowerCDH



PowerCDH Features

- Originally Developed for Danish Small Satellite, Rømer, for Command and Data Handling Unit (Rømer CDH)
- Powerful (150 MIPS typ.) single board computer for space applications and harsh environments
- Based on *radiation tested* PowerPC 603R and RT FPGAs Memory Control Unit with EDAC (SW transparent)
- 16 MB SRAM, 5 MB EEPROM, 64 kB PROM (RadHard)
- High Speed Serial & dual CAN interfaces
- Power Consumption optimised design: 2W - 10W
- Radiation tolerance:
 > 20 krad
- Good tools support (C, C++, ADA95, debugging)



PowerCDH Breadboard (RØMER CDH)



Interfaces:

 2 x CAN bus, CAN 2.0B (ISO 11898) compliant, speed 1 Mbps Patria

- Two high speed synchronous serial interfaces (LVDS), or optional SpaceWire Links (ECSS-E-50-12).
- Timing correlation pulse output, RS-422
- Three external interrupt inputs, RS-422
- 8 internal & 8 external analogue inputs for housekeeping telemetry
- UART and COP (JTAG) Debug ports



Software and Tools

- Binary compatible with PowerPC-603e
 - Well proven, widely used design
 - Good compiler support (C, C++, ADA95, ...)
 - GNU tools are available for free on the web
- Boot strap (assembly and C code) and basic test SW provided for evaluation
- Basic BSP for RTEMS available
- BSPs for other RTOS can be developed on request
- Debugging Environment:
 - FLASH can be used instead of PROM (breadboard)
 - Debug UART Interface, eight GPIO lines
 - CPU Debugging via COP interface e.g.: with Lauterbach debugger
 - BootPROM Emulation Support
 - External System Clock Input and PLL bypassing



PowerCDH Features

- Good Radiation Tolerance (tested)
 - CPU is the weakest link. However it is very SEU tolerant!
 - Worst Case CPU SEU probability: 1.41 x10⁻⁴ Errors/day
 => 1 Error in 7092 days (snapshot of the report below)

7. ON ORBIT ERROR RATES CALCULATION

Rates have been calculated using SPACERAD software based on CREME model. The following hypothesis have been used :

- M=1
- Sensitive volume : 50*50*2 µm.
- Geomagnetic shielding : FASTQUIET
- Solar min.

For each of the 8 test programs, error rates have been calculated for 4 separate missions :

- Geostationary orbit (35793 km, 0°),
- SPOT polar orbit (830 km, 97°) ,
- International Space Station (375, 51.6°).
- ROEMER/ MOLNIYA orbit (39867-500km, 63.43°).

Mission	On orbit SEU rates due to heavy ions							
	(SEU/day/bit)			(SEU/day/component)				
Program	REGP603	CACD63R	CACI63R	FFT603R	TRIE63R	TRIEC63R	TRIF63R	TRIFC63R
ROEMER	4.91E-7	8.58E-7	2.03E-9	6.29E-5	9.69E-5	1.40E-4	1.01E-4	1.24E-4
GEO	4.48E-7	8.48E-7	2.06E-9	5.18E-5	7.98E-5	1.41E-4	8.40E-5	1.24E-4
SPOT	1.62E-7	2.99E-7	7.20E-10	1.95E-5	3.01E-5	4.95E-5	3.15E-5	4.38E-5
ISS	4.32E-8	9.32E-8	2.27E-10	4.43E-6	6.91E-6	1.56E-5	7.34E-6	1.38E-5





PowerCDH Features (cont.)

- PowerPC 603R radiation tolerance:
 - Latch-up immune
 - TID > 25 krad,
 - LET > 30.3 MeV/(mg/cm²)
- Atmel PowerPC 603R (QML Q) devices from radiation tested LOT available at Patria
- 255-pin CI-CGA package evaluated successfully. ESA official approval pending.
- PCB layout design requires the use micro vias, blind vias and possibly also burried vias. ESA approval for these routing methods is TBD.





PowerCDH Specifications Summary

- CPU: PowerPC 603R,150 MIPS, ~1 DMIPS / MHz, 450 MIPS peak
- Data Bus Width: 32 bits
- CPU / Bus Clock Frequency: 150 / 25 MHz
- Cache: 16 kB Instruction and 16 kB Data Cache
- Volatile Memory: 16 MB SRAM EDAC protected
- Non-Volatile Memory: 64 kB PROM (OTP), 5 MB EEPROM
- Support Functions: Watchdog timer (programmable 0 1 sec). Housekeeping telemetry with 8 external inputs + Internal telemetry (temperatures and voltages)
- Radiation Tolerance: Latch-up immune
 - TID > 20 krad, SEU Rate < 1 upset / 1 year for LEO orbit
- **Power Supply:** +2.5 V, +3.3 V and +5 V, **Consumption** 2 10 W
- **Dimensions:** 200 x 180 x 20 mm³, **Mass** < 900 g (including Frame)
- Temperature Range: -40 °C ... +55 °C





PowerCDH3



PowerCDH3 Architecture

- PowerPC 7448 processor (optionally 7447A)
- Target performance: ~1000 MIPS
- Flash, EEPROM for non-volatile program storage
- SRAM, SDRAM for software execution
- Three SpaceWire Interfaces
- Dual Mil-Bus 1553B RT
- CompactPCI Master / Peripheral use
- Single voltage supply
- Generous debugging interfaces



Interface

to Memory

Sub-System

32 KB

nstruction Cache



- PowerPC 7448 (optionally 7447A) @ 800 MHz
 - 90 nm SOI Technology
 - 32 kB L1 caches for Instructions & Data
 - 1 MB L2 cache EEC protected
 - Superscalarity: 4 instructions / clock cycle

11 independent execution units

- AltiVec Engine speeds up image processing
- Core voltage 0.9 V ... 1.3 V
- I/O voltage 1.8 V (2.5 V possible)
- PPC 60x System bus speed: 50 MHz
- Flexible clocking, configurable multipliers





Sequencer Unit

BHT/

BILC

FPR Is sue

32 KB

Data

Cache

1 MB Unified L2 Cache

System Interface Unit

60x/MPX Bus Interface

360 Contact HiCTE

BGA Package

Instruction Fetch

Branch Unit

Dispatch Unit

GPR Issue

Completion

Uniτ

CEX_SEX0_SEX1_SEX2

and and state and state and





PowerCDH3 System Control

- System, Memory & Interface controls in FPGA (System Control Unit, SCU)
- Actel HiRel radiation tolerant antifuse FPGA (RTAX2000S)
- Built-in voting of internal registers (flip-flops)
- Logics capacity: 2M gates, ~250 000 ASIC gates
- CI-CGA Package, 624 pins, 418 User I/Os available
- Prototyping in EBB with commercial grade,
 896 balls BGA attached to 'prototyping interposer socket'







© 3D Plus



PowerCDH3 Memory

• Boot Memory:

• 2 MB Flash memory, to be replaced with RadHard OTP PROM

• Program Storage:

• 4 MB EEPROM, switchable Power ON/OFF for improved TID tolerance

• Program Execution:

- 8 MB Fast SRAM (~17 ns access), with EDAC (SECDED)
- All error corrections transparent to software. Corrected errors counted & reported to software
- 256 MB SDRAM (SO-DIMM), intended for data processing storage
 - Proprietary EDAC for Single Event Failure Interruptions (SEFI)
- SDRAM Implemented with 3D Stacked Memory Cubes in EQM / Flight Model





PowerCDH3 System Peripherals

• Microcontroller (Atmel AVR)

- Flexible debugging support; GPIO, Ethernet connectivity (EBB)
- TapSpacer[™]
 - Remote JTAG Boundary-Scan connectivity provides thorough testing of all on-board electronics via one interface

Watchdog timer

- Programmable 0..1 sec. disabling possibility in EBB
- Two 32-bit general purpose timers
 - Prescaling, cascading, 20 ns granularity (TBC)
- Interrupt control
 - 16 Interrupt Requests, masking, ISR (SW) driven priority
- CPU Thermal protection
 - Warning level interrupt, critical level system shut-down





PowerCDH3 Interfaces

- Power: Single supply 5V, (30W)
- CompactPCI: 32-bits, 33 MHz, selectable Master / Peripheral operation
 - Implemented with Actel IP-Block (RTL)
 - Compliant with the standard with slightly reduced functionality
 - DMA Channel towards SDRAM Array (TBC)
- **SpaceWire:** Three independent interfaces
 - Implemented with IP-Blocks provided by ESA/ESTEC
 - DMA Channel towards SDRAM Array
- Mil-Bus 1553B: Dual Redundant, Remote Terminal
 - Implemented with Actel IP-Block (Netlist)
 - Shared messaging memory in SRAM
- Debug Interfaces:
 - GPIO, Ethernet 10/100 LAN, PPC COP, JTAG, TapSpacer[™], EIA-232



Test SW Development

LPT:

-

Parallel Interface

Debug

-

JTAG/ BDN

- Test SW Command & Control via EIA-232 bus
- Test SW can be updated on-board, on-line
- Test SW has control over all external interfaces
- Use of a real-time Linux kernel shall also be evaluated. MontaVista Linux has been chosen for this purpose.
- Freescale MCEVALHPC2-7448 development platform used for early SW development
- Development environment and tools:
 - Linux workstation
 - GCC cross compilation toolset
 - Lauterbach In-Circuit Debugger (JTAG/COP)







- **CPU:** MPC7447A or MPC7448
- **Performance:** > 900 MIPS sustainable, > 4000 MIPS peak
- CPU / Bus Clock Frequency: 800 MHz / 50 MHz
- Memory Capacity:

CPU Caches: L1: 32 kB+32 kB, L2: 1 MB EEC (7448)
Boot strap: 128 kB RH OTP PROM in flight version
Program Storage: 4 MB EEPROM, optional power switch-off
Program Execution: 8 MB SRAM, EDAC Protected (SECDED)
Data Storage: 256 MB SDRAM, SEFI tolerant, EDAC Protected (SECDED)

Patria

- Interfaces: CompactPCI, Mil-Std-1553B, SpaceWire
- Dimensions: Double Euro card 233 x 200 mm ; Mass budget < 1.2 kg
- Power Budget: Typical 15 ... 25 W, Low power 6 W
- The PowerCDH3 development model will be available in Q2/2007.





PowerCDH3 Design Challenges

Performance

- SCU FPGA is the bottleneck for high bus frequency
- Speed of SDRAM accesses and SpaceWire interfaces are to be optimised
- Careful layout design and routing of PCB is imperative (micro, blind and burried vias)
- Clocking of CPU alone is not an issue, except for thermal design

Thermal Design

- The higher performance the bigger dissipation, balance and trade-offs
- CPU and memory devices will be hot-spots
- CPU Cooling with heat pipes is studied

Radiation Tolerance

• Assessment for CPU SEU tolerance is needed

Hardware - Software Integration and Interoperability



Contact Information

- Patria www.patria.fi
 - Space Electronics
 - Naulakatu 3
 - FIN-33100 Tampere, Finland
 - Tel. +358 20 4691
 - space@patria.fi
- Direct Contact:
 - Jaakko Toivonen
 - +358 40 869 2338
 - jaakko.toivonen@patria.fi
 - Fax: +358 20 469 2693