ASTRIUM

Requirements review
Needs for launchers, space vehicles & orbital infrastructures

Next Generation Microprocessors
for Space Applications

ESA Round Table - September 11,12,13 - 2006 - ESTEC

P. Cormery,

Data management & SW
ASTRIUM Space Transportation Sas

S. Rakers

Avionics engineering
ASTRIUM Space Transportation Gmbh

OUTLINE

ASTRIUM

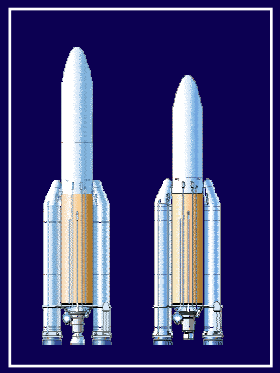
- **Scope of applications**
- **Status and perspectives for launchers**
  - **Roadmap elements**
    - Overview
    - New On-Board Computer for Ariane 5
  - **Most demanding technical requirements for data-processing**
  - **Constraints for the migration from existing solution to next generation**

- **Status and perspectives for other space vehicles and orbital infrastructures**
  - **Technological overview**
    - Future requirements
    - Operating systems, SW & tools
    - Digital avionics & study, in ST Bremen

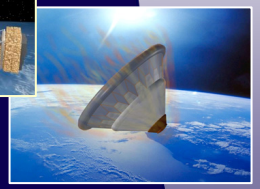
ASTRIUM

Astrium ST Scope of Applications for on-board systems

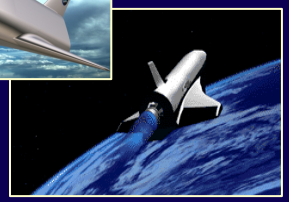
Launchers:
- **Ariane**



Orbital Systems:
- **Columbus**
- **ATV**
- **Operations**
- **Atmospheric Reentry Systems**



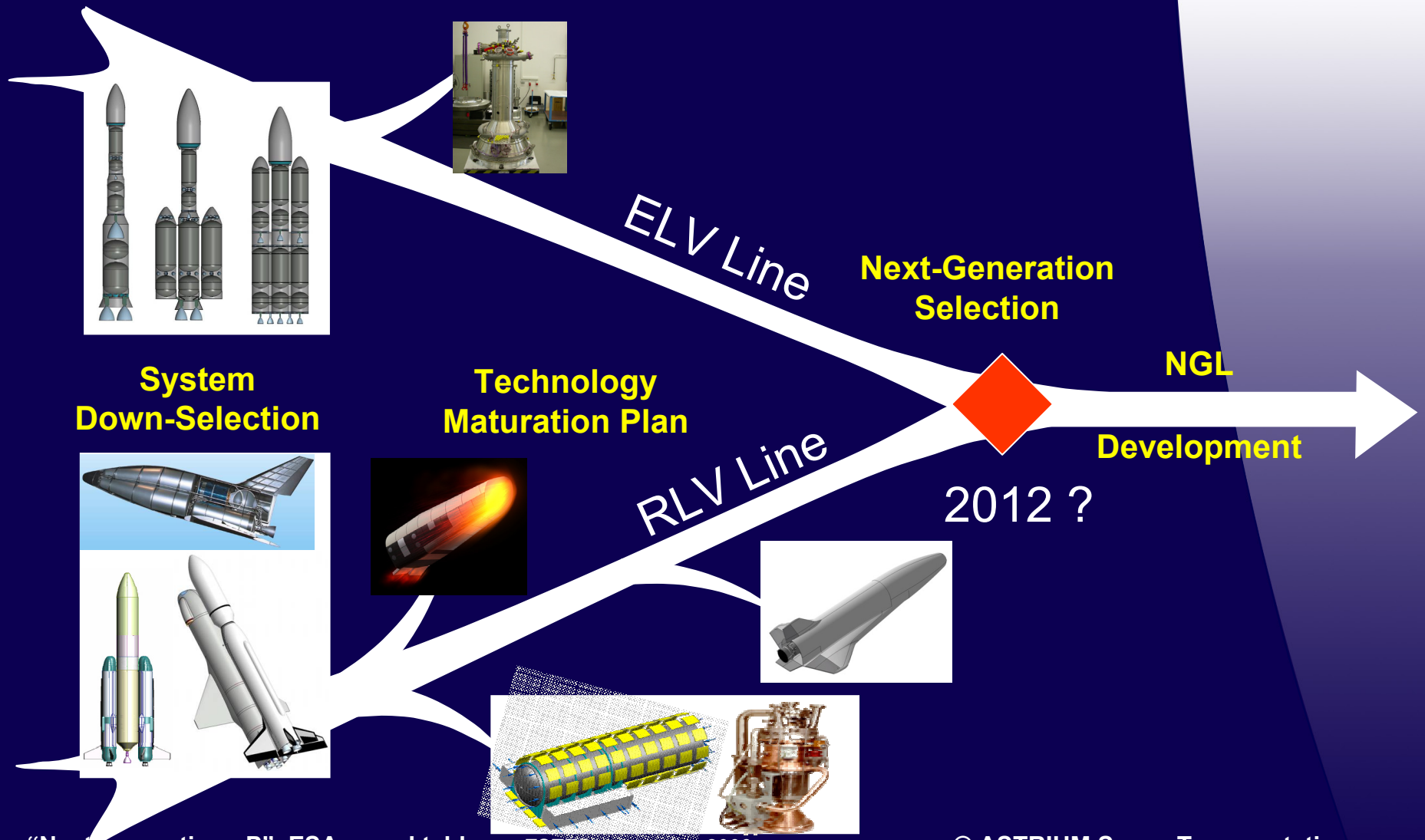
Future Launchers



Ballistic Missiles Missile Defence

ASTRIUM

From Ariane to Next Generation Launchers

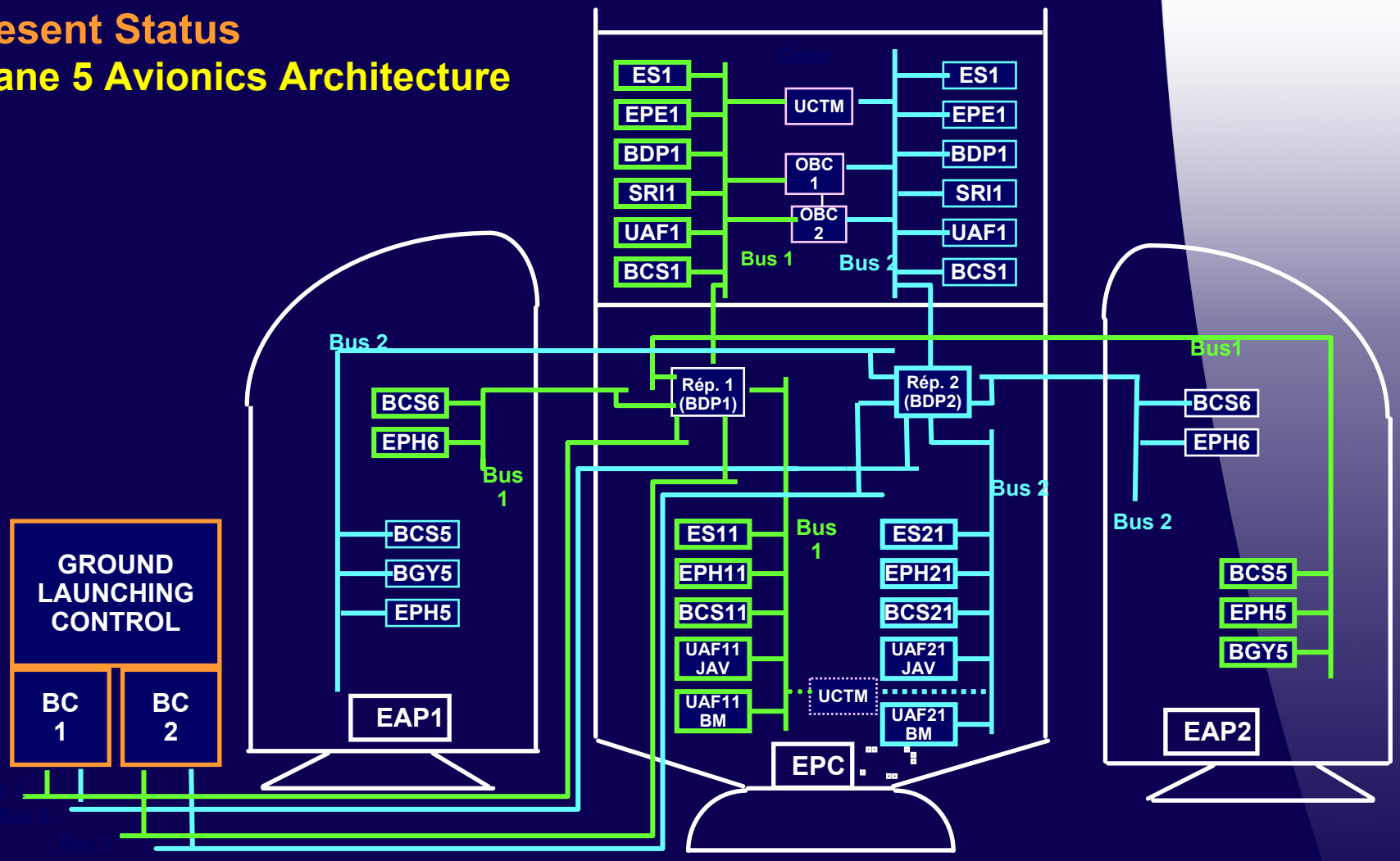


New On-Board Computer for Ariane 5

ASTRIUM

- **Present Status**

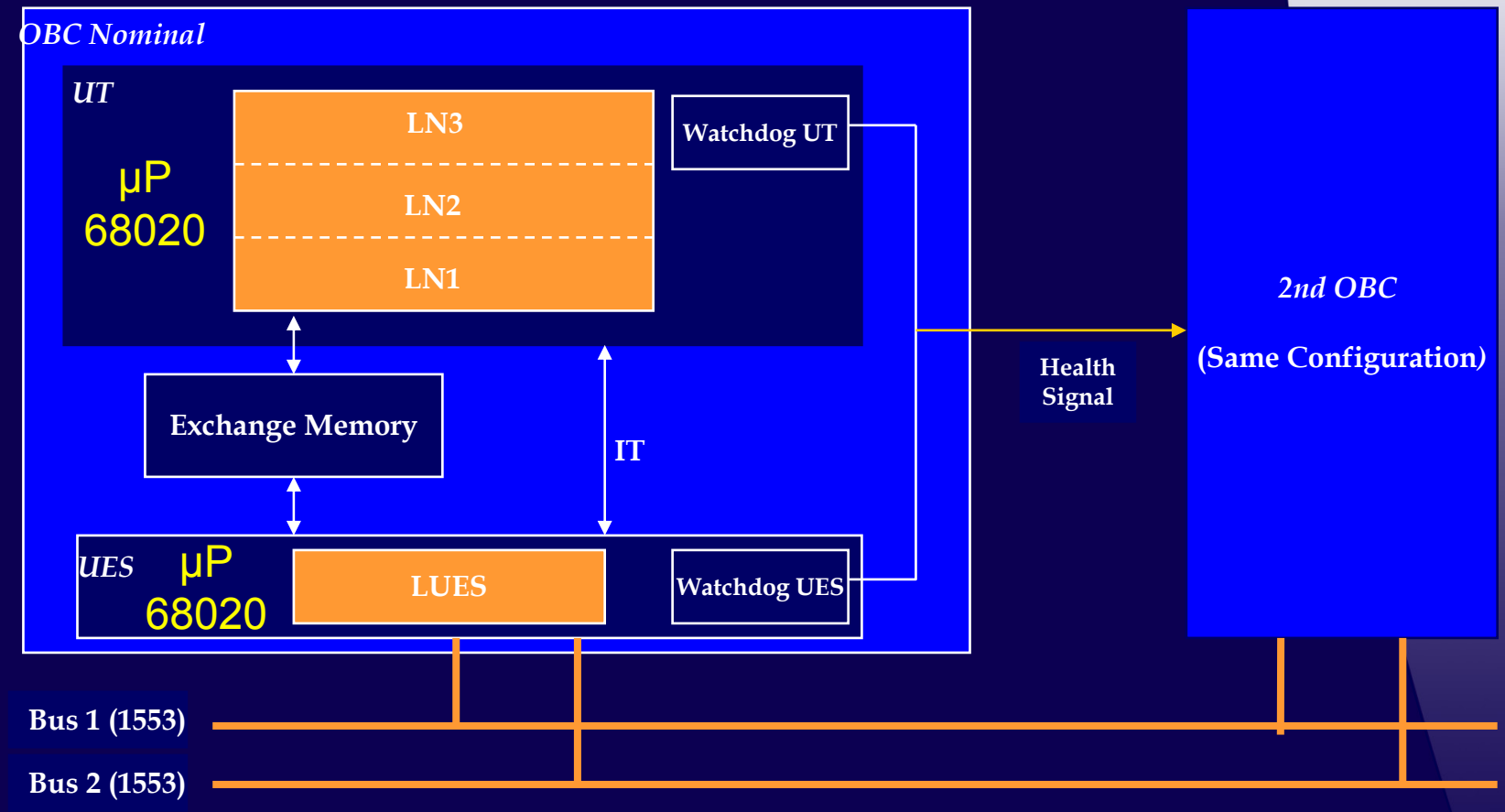
Ariane 5 Avionics Architecture



New On-Board Computer for Ariane 5

ASTRIUM

- **Present Status**
  On Board Computer



New On-Board Computer for Ariane 5

ASTRIUM

- **Many components of the OBC are obsolete (µP68020, SRAM, ASIC,…)**
  - **For A5 PA Batch, the coverage of the OBC production needs has been solved either by the constitution of a stock (this is the case for µP68020) or the substitution by new components which has been anticipated when possible**

- **The status of the stocks will not allow to produce more than 20 OBC (10 launchers) after PA Batch.**
  - **4 years are necessary to develop a new OBC**
    - ✓ **Analysis on A5 "cadence" for the next 5 years shows that it is already impossible to increase the A5 production, up to 8 by year**
    - ✓ **We have to start the development next year**
      - ☞ **Choice of the adequate Processor candidate**

Migration from existing solution to next generation

ASTRIUM

- **minimal period of 10 years to be covevered with the new OBC production**
- **Recuring Costs reduction**
- **Strong constraints to make the migration with minimal system impact on existing A5 SEL (Flight SW, missionisation tools and data-base, simulation tools, qualification platform, SW development environment, …)**
  - **Management of other Obsolescences**
  - **Porting of existing Fligth SW without change on interfaces / LN1 services**
  - **…**

« Sizing » technical requirements for A5 data-processing

ASTRIUM

- **Performances**
  - The Existing 68020 is covering the needs of power processing for different missions and existing versions of Ariane 5
  - The ERC32 gives the capability to implement more demanding functions for future missions / launchers characteristics evolutions
  - The LEON gives sufficient power processing for important changes of the avionics architecture on the future launchers (merging of functions on integrated Equipment to reduce recuring costs)

- **Radiation Tolerance Requirements**
  - Cumulated dose negligible in the case of A5 flight
  - SEE compatibility to be respected for A5 missions (GTO, GEO, SSO,..)

New On-Board Computer for Ariane 5

ASTRIUM

- **Explorative R&T study performed with LEON evaluation Board**
  - **favorable results about functional compatibility, but acceptability of WCET with cash still to be demonstrated for A5 (on-going study to be finalised by the end of this year)**
  - **confortable margins for new architecures, additional functions and use of innovative SW methods & tools**

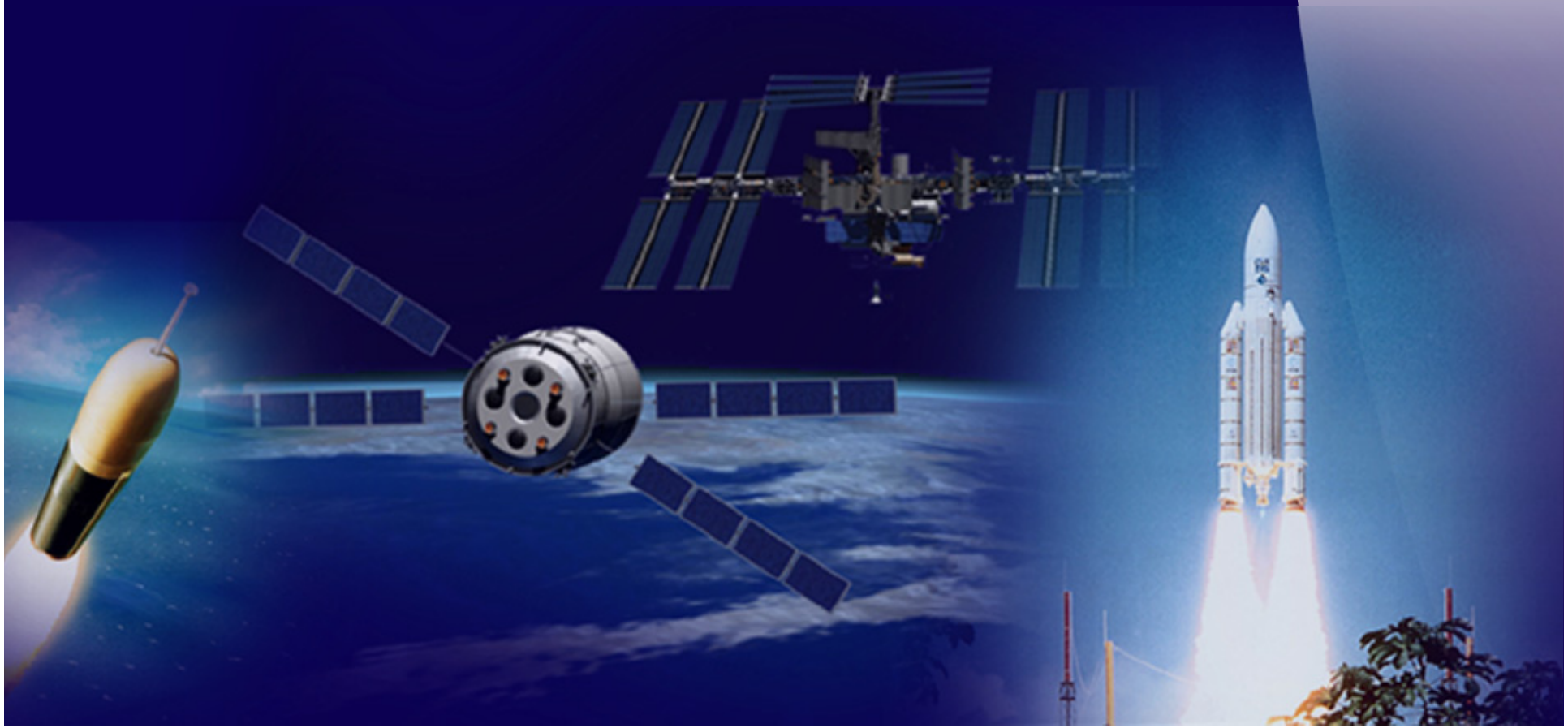
☞ **Functional adequation should be OK with AT697E, but is there a sufficient level of garanty to have a qualified AT697F on time for post PA A5 (without any additional shift of the development) ?**

✓ **Risk reduction and roadmap consolidation ?**

✓ **ERC32 as an alternative solution or Backup ?**

ASTRIUM

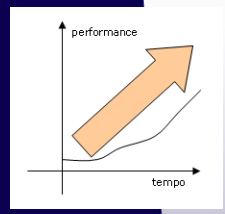
Orbital Infrastructure needs by ASTRIUM ST



ASTRIUM

Future Orbital Infrastructure Requirements

- Significant gain of performance
  - Fast control loops (~ 50 s^{-1}) require new CPU technology (AT697)
  - Fast backplanes, e.g. **Compact-PCI** bus as VME successor
  - Large memory arrays (256 – **1024 MByte**)



- Obsolescence of parts requires new designs
  - ERC32, RAM, EPROM etc. become obsolete

- Modular system (industry compatible) for cost effectiveness
  - Tailor system to needs of mission (environment, safety, cost...)
  - Compatibility with industry standards (e.g. cPCI, 19”) to **incorporate COTS**
  - **Configurable redundancy** concepts

- Modern & fast interfaces (but also legacy I/F to stay compatible)
  - Spacewire, CAN, Ethernet, AFDX
  - MIL-STD-1553B, RS-422
  - compact PCI bus (bus bridge, connectors etc)

- Solve ITAR problematic
  - European parts (LEON etc), IP-cores, System-on-Chip, COTS ...

Operating systems, Software, Tools

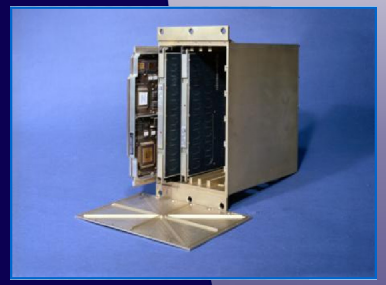
- O/S: for SPARC architecture preferably VxWorks, rather than RTEMS
  - re-use of existing code with low porting effort
  - large flexibility
  - powerful development tools available
  - widely spread
- Use of other industrial O/S desirable, but not available for SPARC
  - QNX, broadly used in automobile industry
- Model-based code generation with Matlab/Simulink for control loops
  - GNC
  - Scientific Payloads

ASTRIUM

Digital Avionics heritage by ASTRIUM-ST

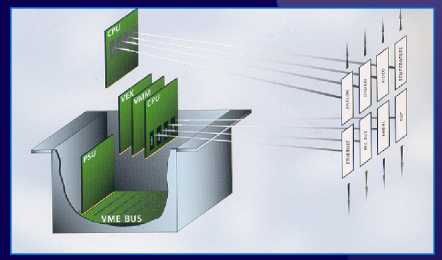
Unique Digital Avionics devices recently made by ASTRIUM ST Bremen:

- **Fault-tolerant computer (DMS-R FTC)** as the central ISS control unit – operational
- **Standard Payload Computer (SPLC)** is implemented in many COF/US-Lab payloads – operational
- **FTC** (re-use of DMS-R FTC) as the main centralized control unit for ATV – qualified
- **Propulsion Drive Electronics (PDE)** for ATV – qualified



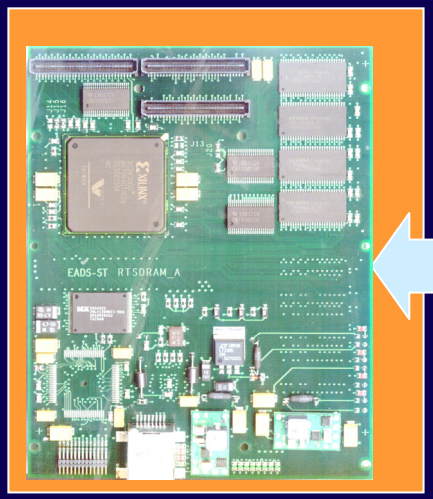
Common baseline:

- **Open architecture**, based on standardized + commercial (VME) backplane
- Building block system: **modular + scaleable** architecture
- Identical hardware with **configurable redundancy** concepts
- Modularity reflects in S/W architecture: **re-use of S/W** over complete product life cycle (demonstrator – flight H/W)

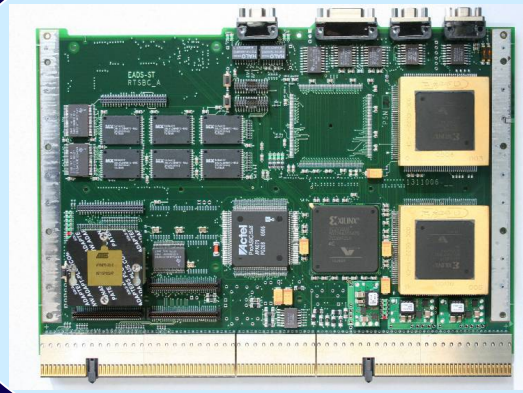


ASTRIUM

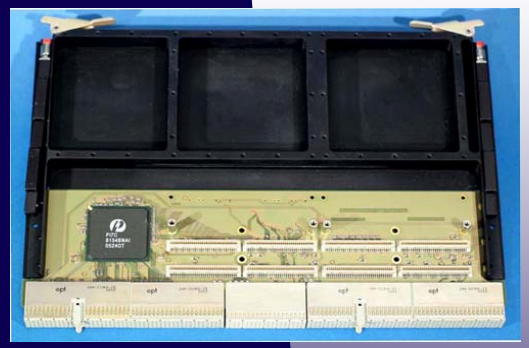
Study project SPAICE (design bread board)



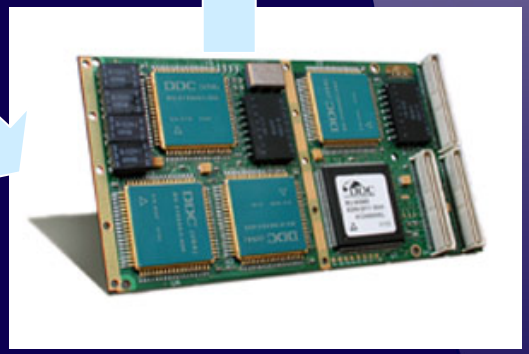
Radiation tolerant
memory extension



compactPCI
single board computer
(AT 697)



COTS cPCI PMC carrier



COTS MIL-Bus PMC module
(or other PMCs)