CENTRE NATIONAL D'ÉTUDES SPATIALES

Round-table on Next Generation Microprocessors for Space Applications :

CNES requirements w.r.t. Next Generation General Purpose Microprocessor

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Outline

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- Three main classes of applications
  - Data Handling P/F central computers
  - Hybrid “Data Handling / Data Processing” computers
  - High Performance P/L data processing computers
- Derived requirements
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Present situation (1/2)

- **Availability of european space qualified general purpose microprocessors is mandatory for independence reasons**
  - **US rad hard products under ITAR : RAD6000 (Bae), PPC603e (Honeywell)**
  - **space qualified rad tolerant microprocessors will be needed in all cases for data handling central computers of commercial missions (telecoms, observation, navigation, …)**
- **Processing performances of this EU space microprocessor should increase continuously to allow :**
  - **for improvement of spacecrafts' autonomy**
  - **for improvement of flight SW development productivity : standard layered architectures, reusability of building blocks**
  - **for improvement of on-board reprogrammable P/L data processing capability**

Present situation (2/2)

- **Development of a new generation space microprocessor is becoming a more tedious process each time :**
  - **industry ROI uncertain due to niche market**
  - **agencies funding limited w.r.t. increased complexity of design and cost of technology**
  - **development time often much longer than planned (e.g. : AT697)**

- **Net result : EU hirel space microprocessor are lagging more & more behind COTS counterparts**
  - **factor 100 in performance :**
    - LEON@100MHz = 100 Mips ; PENTIUM4@3.2GHz = 9700 Mips
  - **for the same technology, operating frequency is much lower :**
    - For 0.18 µm : AMD Athlon 1.5GHz, LEON2 100MHz
  - **For the next generation a factor 1000 on performance is likely**

- **COTS microprocessors usage for high end on-board data processing applications is becoming unavoidable**

Three main classes of applications

- **Data Handling P/F central computers :**
  - **Command / Control tasks**
  - **high availability & safety requirements**

- **Hybrid "data handling / data processing" computers :**
  - **typical of P/L computers mixing C/C tasks and number crunching applications for P/L data reduction before TM to ground**
  - **fairly high availability & safety requirements (for commercial & high-end science missions)**

- **High Performance P/L Data Processing computers :**
  - **dedicated computer for very demanding data reduction processing for which in-flight reprogrammability is required (e.g. : GAIA)**

Data Handling P/F central computers

- **Main characteristics and derived requirements :**
  - **high availability, safety critical, high environmental constraints**
    - → **hirel rad-tol microprocessor required (in particular for commercial missions)**
  - **slowly evolving processing power requirements (due to increased autonomy trend)**
    - → **post-LEON not needed before 5 or 6 years**
  - **multi-core not needed (potentially not wanted due to added complexity if not transparent for SW development)**
  - **very high level of SW validation required**
    - → **determinism of operation is desirable : observability and predictability of cache operation would be a plus**
  - **Upward compatibility with Sparc V8 instructions set is required**

Hybrid “data handling / data processing” computers

- **Main characteristics and derived requirements :**
  - **typical of P/L computers mixing C/C tasks and number crunching applications for P/L data reduction before TM to ground**
  - **high availability & safety requirements (for commercial & high-end science missions)**
    - → **hirel rad-tol microprocessor required (in particular for commercial missions)**
  - **rapidly increasing data processing power requirements (due to data reduction algorithms complexity or emergence of regenerative telecom P/L)**
    - → **post-LEON @ 1 Gips typ. available in 2 to 3 years would be needed**
  - **multi-core acceptable but not required**
    - → **segregation of C/C and P/L data processing tasks can be achieved through RTOS**

High Performance P/L Data Processing Computers

- **Main characteristics and derived requirements :**
  - **high end scientific P/L with very demanding data reduction processing (>Gops), computer vision for robotic P/L, …**
    - → **no solution based on hirel microprocessor**
    - → **state-of-the-art COTS microproc. needed with fault tolerant architecture to circumvent SEEs**
      - → **Maxwell SBC750 : based on PPC750FX (IBM) – 1800 Mips**
      - → **SpaceMicro Proton 100K/200K : based on DSP TMS320C6xxx – 1400-4000 Mips**
  - **fault tolerant architectures should cover the whole range of fault coverage as derived from availability requirements of the missions :**
    - → **temporal duplex, HW duplex, HW triplex**
    - → **developped for popular COTS microproc. family : e.g. PowerPC**
  - **permanent techno survey (radiations test) needed + strategic lot procurement and qualification (COTS generic approach)**
    - → **team up with aeronautics to share cost : e.g. SCADRI project for PPC**

Derived requirements (1/3)

- **Driving applications**
  - **hybrid “data handling / data processing” computers (3 year timeframe)**
  - **data handling P/F central computers (6 year timeframe)**
- **requirements specific to space applications**
  - **compatible with commercial GEO missions, ITAR-free**
- **processor architecture**
  - **based on popular COTS MPU family : SPARC, ARM, PPC, …**
  - **if multicore, should be transparent to SW developer (i.e. : parallelism of tasks or codes should be handled by RTOS or SW development chain)**
- **SW development related needs**
  - **avoid “space specific” development environment**
  - **improve observability & predictatbility/determinism of cache operation (would ease in particular schedulability analysis)**

Derived requirements (2/3)

- Performances targets
  - Mips/Mflops : one order of magnitude w.r.t. LEON, i.e. : 1 Gips / 250 Mflops
  - power consumption : < 3 mW/MHz
- availability as standard ASIC
  - required for most applications, which need either the full performance or a fully validated component with its SW validation chain
  - performances, interfaces : see perf. targets, PCI bus questionable
- availability as soft IP core
  - definitely needed for those projects needing very high CPU integration or dedicated SoC with embedded microprocessor
  - Soft IP core should be commercially supported to enable usage by SME or labs (on FPGA techno)
  - Performance : depending on target techno, interfaces : AMBA busses
- Software compatibility with previous generation
  - upward compatibility with SPARC V8 instruction set strongly desirable to enable code reusability

Derived requirements (3/3)

- **usage flexibility :**
  - **avoid the “all-in-one” syndrome of COTS microprocessor**
    - **→ COTS MPU performance in W/Mips is now decreasing with time**
  - mixing DSP with general purpose MPU in same chip might be sub-optimal for most applications
  - PCI bus I/F on chip : how many OBC with PCI as backplane bus ?

Conclusion

- **Post-LEON general purpose MPU is definitely needed in a 5 year timeframe to guarantee European independence for P/F and P/L computers**
  - **availability of this MPU, both as standard ASIC and VHDL IP core, is recommended**
  - **upward compatibility with SPARC V8 is also recommended**
- **COTS based computers with FT architecture will allow space missions to embark multi-Gops algorithms**
  - **will be an enabling factor for many missions which need sophisticated data reduction algorithm on-board**
  - **permanent techno survey should be initiated (radiations testing) to be able to select most appropriate component while on the market**