ASTRIUM

Harmonisation of European Space Technologies
ESA Workshop 2006 on
<Next Generation MicroProcessor – Round Table>

Hardware requirements for the microprocessor roadmap

<Sept.06, Astrium, Electrical Equipment>

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Microprocessor Roadmap: Definitions

- Following rough timeframes are distinguished for defining the roadmap:
  - Short term: in the next three years
  - Medium term: in four to six years
  - Long term: in seven to ten years
- Following applications for microprocessor roadmap are distinguished:
  - Platform AOCS & Data Handling
  - SSMM Control & Data Management
  - Payload Control & Data Management
  - Payload Data Processing
- Payload Control & Data Management requirements are distinguished between
  - Telecommunication missions
  - Science and E/O missions

Microprocessor Roadmap - Platform

- Platform Requirements for short – medium – long term
  - Low power, high reliability, availability of parts, especially from European sources
  - Processing Performance of 20-80 MIPS or 5-15MFLOPS
  - Driving applications for higher performance processing would be: Merge of star tracker, GNSS Receiver, Telemetry compression and encryption into the platform processor; but there are some counter-examples (RTC, Security Units, …)
- Therefore following activities are essential
  - Safeguarding of current technologies and components and to establish European sourced components rather than investment in high integration technologies. Components of great importance for investments:
    - MOSFETS, adequate FPGAs, memories, …
  - Improve qualification/certification status and availability of standard components or products
    - VHDL cores (PTME, CAN, LEON, …)
    - Standard ASICs
    - System-on-Chip
  - Consolidation of generic components, models, tools, architectures and interfaces before spending significant investment in future technologies

Microprocessor Roadmap – SSMM

- SSMM Requirements Processor Requirements
  - Driving applications for higher performance processing :
    - File Management System (FMS)
    - Compression (different and high speed algorithms)
    - Encryption (different and high speed algorithms)
    - Formatting (different and high speed standards)
- SSMM other Requirements
  - Next Generation of high capacity, high speed memory devices:
    - Flash memories
    - DDR2/3-SDRAM
  - Request for larger Mass Memory Capacities (up to10 Tbit)
  - Request for higher Data Rates (up to 10 Gbps)

Microprocessor Roadmap – Payload Control

- Payload Control Requirements for short and medium term
  - Same as platform requirements
- Payload Control Requirements for long term:
  - Increasing amount of sensor raw data in science and E/O domain and communication channels in the telecom domain lead to higher demand for data management processing
    - 1000MIPS for payload control and data management (long term need)
    - High speed interfaces and router networks
    - Data Throughput higher than today -> 64 bit architecture?
    - Required technologies: High density ASIC technology (90nm), high density packages (>600 I/Os)

Microprocessor Roadmap – Payload Data Processing

- General P/L architecture and standardization appreciated.
- Major P/L technologies identified fully in line with Astrium position; High Performance Processing must be achieved by acceleration with co-processor to the LEON. Two solutions must be maintained for the future:
  - LEON+FPGA/ASIC technologies
  - LEON+generic high performance data processor
- Bottleneck in data input and routing may be underestimated.
- Recommend to consolidate “existing” technologies for space market (e.g. ATC18, libraries, development and validation environment) and then to focus on the next-but-one technology generation.
- High rate payload data processing requires specific data processor/DSP (not subject to this workshop)
- Medium rate data processing may be a driving application for a NG Microcontroller leading to a one chip solution for certain payloads
  - Several hundreds of MFLOPS necessary (Today: 60MFLOPS)
  - High data throughput on chip level (>500MByte/s) (Today: 200MByte)
  - High speed interfaces

Microprocessor Roadmap – General

- Short term:
  - Consolidate IPs, components, ASIC technology (0.18), architectures, tools, methods, standards, HW-SW codesign
  - Establish generic architectures to improve overall system performance (LEON+co-processor)
- Medium term (if short term activities are performed successfully):
  - Establish new IPs for more complex applications (compression, decryption, formatting, …)
  - Establish new ASIC technology (0.09μm)
- Long term
  - Establish new microprocessor architecture (64 bit?) for control + data management as spin-in from commercial market -> reuse of software tools and architectural concepts
  - Provide IP data base for SOCs with new architecture
  - Proof of architecture (ASSP?)