User Requirements for Next Generation Microprocessors

ESA Round Table 2006 on Next Generation Microprocessors for Space Applications

11-13 Sept 2006, ESTEC, Noordwijk, The Netherlands

Olivier Notebaert – Astrium Satellites Central Engineering

olivier.notebaert@astrium.eads.net

LEON processor status

- Leon is a valid basis for building processor devices in the range 40-100Mips
  - Solutions with current technology:
    - Based on LEON2-FT AT697F component
    - Based on LEON2-FT Core integrated with support functions and I/F
    - Custom System On Chip with Leon2 or Leon 3 implemented in FPGA or ASIC
    - On-Chip or external Co-processing function can be associated to reach added specialised function

General trend for future missions

- New missions call for new requirements
  - Robotics, Autonomy, Security, formation flying…
  - New instruments and sensors technology
  - General increase of on-board data processing needs (performance, algorithms, data volume, communications rates)
- Need for overall budget reductions
  - Power consumption reduction
  - Mass and Volume reduction
  - Operational costs: reduction of the satellites dependence beside ground (i.e. mission autonomy)
  - Manufacturing delay reduction (parallel development, AIT)
  - Improvement of SW development techniques

Driving applications

- Science
  - Image processing, compression, navigation
    - Most demanding functions are implemented with HW
    - SW implementation of complex algorithms in powerful processor is an alternative providing more flexibility
  - On-board data and storage volume increase
- Planetary exploration
  - Autonomy (on-board intelligence for planning and decision)
  - Robotics
  - Orbital manoeuvres (capture, re-entry, landing,…)
- Telecom
  - Flexible telecoms (on-board signal decoding…)

Specific requirements driving space missions

- Radiation tolerance
- Extreme Thermal & Vacuum properties
- No dependency (any generic solution shall be ITAR free)
- Low power consumption
- Integration and mass limitations
- High reliability over long missions (especially telecom and planetary exploration,…)

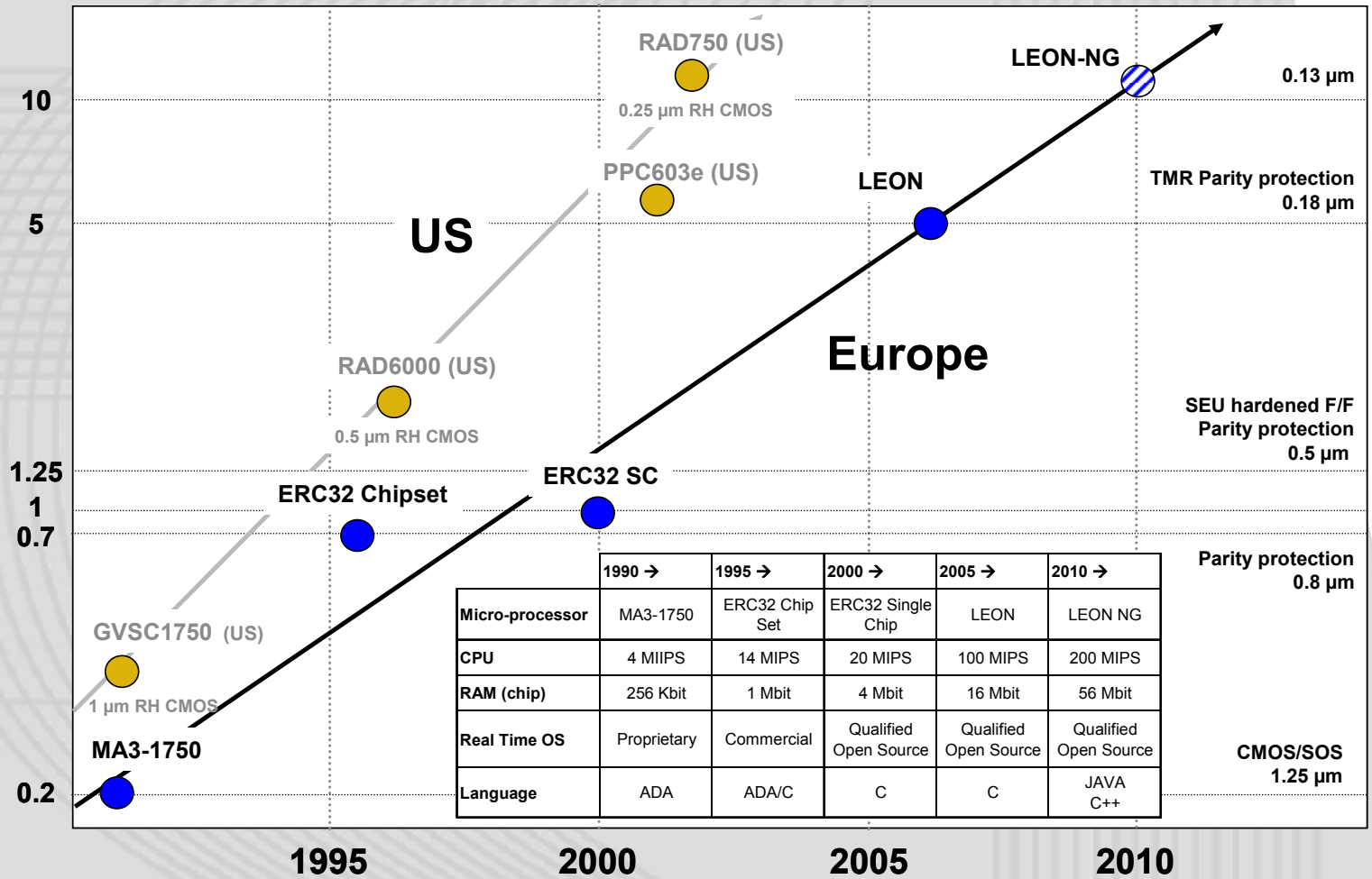
Processor Architecture

- Strategic choice
  - SPARC/Leon: Maybe not the best but it has become a legacy for European Space Industry. Experience gained and wide product and IP library are becoming strong assets
  - ARM: Widely used for SoC's. Availaibility of VHDL issue?
  - PowerPC: Widely used for avionics application. Is it also a best choice for any payload processing ?
- Shall ensure performance in SW execution high enough for many application types…
  - within a single component
  - and/or close and efficient interface to co-processing devices (preferably several)
  - and/or scalability for a "network of processing unit"

SW engineering, design and validation

- Methods and tools for design and validation
  - Efficient SW development platforms and tools
  - Modelisation capability, including caches
  - Representative HW/SW simulation
- Availability of numerical and hybrid simulator
- Testability and observability
  - Enhanced embedded debug functions
  - Efficient test interfaces (high rate, non intrusive)
  - 64 bit read-only counter
    - Simple and very precious for SW and tests

Performance target (1/3)



	1990 →	1995 →	2000 →	2005 →	2010 →
Micro-processor	MA3-1750	ERC32 Chip Set	ERC32 Single Chip	LEON	LEON NG
CPU	4 MIIPS	14 MIPS	20 MIPS	100 MIPS	200 MIPS
RAM (chip)	256 Kbit	1 Mbit	4 Mbit	16 Mbit	56 Mbit
Real Time OS	Proprietary	Commercial	Qualified Open Source	Qualified Open Source	Qualified Open Source
Language	ADA	ADA/C	C	C	JAVA C++

Performance target (2/3)

- Reasons for processing performance increase
  - Autonomy
  - Sensors evolutions (processing within central computer
  - Higher amount of data to handle
  - New on-board services (navigation, planning, tracking, security,…)
  - Evolution of SW development techniques (autocoding, languages…)
  - Harmonization and standardisation (communications, I/O's and services, ECSS, SOIS, PUS…)
  - Reusability, configurability of generic solutions

Performance Target (3/3)

- Performance target should not be driven by what's possible given the technology or the Moore's law
- An attempt should be performed to better characterize:
  - The important performance criteria and targets (Ips, Flops, latency, frequency, mips/watt, etc…)
  - The type of demanding processing from the different applications (algorithm, math functions…)
  - The most demanding applications
  - The number of applications in the various performance ranges

Performance Enhancements

- Look at implementing specific functions in the processor such as FFTs, Convolution etc.
  - Maybe implementing this as a set of extensions similar to MMX, SSE 3DNOW on current desktop processors
- DSP interface or Onchip DSP Co-processor (e.g. ARM+MAGIC in ATMEL Diopsis)
- Multiple processing cores
- Cell architecture
  - Scalable
- On chip FPGA
- On chip Semi-custom ASIC ie XPP
- Programmable network of components on chips

Low power

- Disable clocks and implement sleep modes
- Clock gating
- Dynamic clocking (the processor slows down when the load is less to save power)
- Low Voltage
- Disable options for unused differential signals
- Disable options for internal cores
- Low power modes (dynamic selection of active embedded functions)

Interfacing (1/3)

- Bus Interfaces
  - If integrated, should be compatible with ESA roadmaps for harmonisation reference architecture (SpaceWire + Milbus 1553 and optionally Can)
  - PCI interfaces require a large number of pins and require an equivalent PCI interface within the peripheral device. Not recommended
  - USB - for breadboard debugging ?
  - SIF – for breadboard debugging ?
  - PCI express ???
  - Flexray ???
  - Ethernet ??

Interfacing (2/3)

- Memory interfaces
  - Support for DDR RAM ?
  - Flash support
  - Larger memory support (64 bit addressing)
    - Support future requirements
    - Potential use within Mass Memory Controllers
- Better support for coprocessors (FPGA's or ASIC's)
  - Include support for high speed interfaces such as RocketIO
  - Options for a non-cached memory interface for IO mapping
  - External DMA channels

Interfacing (3/3)

- Local Sensor bus interface
  - SPI, I2C
  - Integrated temperature probe
  - Monitoring of internal voltage

Availability as a standard ASIC

- If it is suitable for most applications a standard qualified ASIC component provides is attractive since:
  - Lower non-recurrent costs
  - Known and trusted performance and reliability
  - Larger community of users
  - enforced reuse rate
- Therefore, selection of functions, architecture and interfaces should be defined by a user group in order to ensure that it is suitable for most applications

Availability as an IP Core

- LEON return on experience shows that this availability is very useful especially
  - On Ground for the capability to use commercial HW for prototypes and ground demonstration mock-ups, SW development models, simulation facilities with HW in the loop and real OnBoardSW.
  - For capability to build ad-hoc architecture in case of specific need (when not possible with the standard ASIC component).

SW compatibility with previous generation

- Current embedded SW have layered architecture
  - Basically: Application layer, service layer, operating systems, BSP's
  - ➢ Portability of source code is required (availability of SW development environments in C and Ada)
  - ➢ Compatibility of the Processor Instruction Set is a bonus but does not seem mandatory (processor requirements are more important drivers)
  - ➢ Adaptation of SW development environments, operating system and low level SW should be done in parallel to the µP development

Other Requirements

- Memory Management by implementing an MMU
  - This would allow memory segregation and lead to more reliability
  - Also allows for substitution of failed memory banks
  - Potential benefits for Mass memory controllers
  - Allows partitioning for running SW of different applications and criticity level on the same processor

Usage Flexibility

- Onboard Programmability
  - Utilise RMAP/SpaceWire to perform remote DMA operations in memory.
    - Enables booting without PROM/EEPROM
    - Application to Instrument and spare processors, not OBC
    - Potential application in OBC to enable register and RAM access without processor intervention

Mapping process example

	Typical Performance		RAM size	Data rates	Main Data I/F	CoProcessor		Number µP per year	Number of Independant SW
Application type	MIPS	MFLOPS			(1553, SpaceWire, Others)	Yes/no	Type		
GEO Platform Control	10								
LEO Platform Control	100								
Telecom P/L	1000								
High end P/L processsing	2000								
Multi Instrument mission	500								
Instrument processing (radar, image…)	1000								
Launchers	50								
Space Infrastructure	500								
Re-entry	500								