LEON2-FT
Evaluation and development activities

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R&D Plan for LEON Evaluation

- **Studies on LEON 2 functions and features:**
  - SW DEVELOPMENT and TEST ISSUES
    - LEON and AT697 functions (e.g. Debug, FPU, I/F…)
    - SW development environments and simulators
    - HW/SW Prototypes and benchmarking
    - Explore possibilities for debug and tests issues
    - Impact on SW development and validation process
  - EVALUATION of LEON-2 or AT697 based computer building blocks on demonstration platforms for:
    - Spacecrafts avionics control
    - Payload control and data processing

LEON Evaluation objective

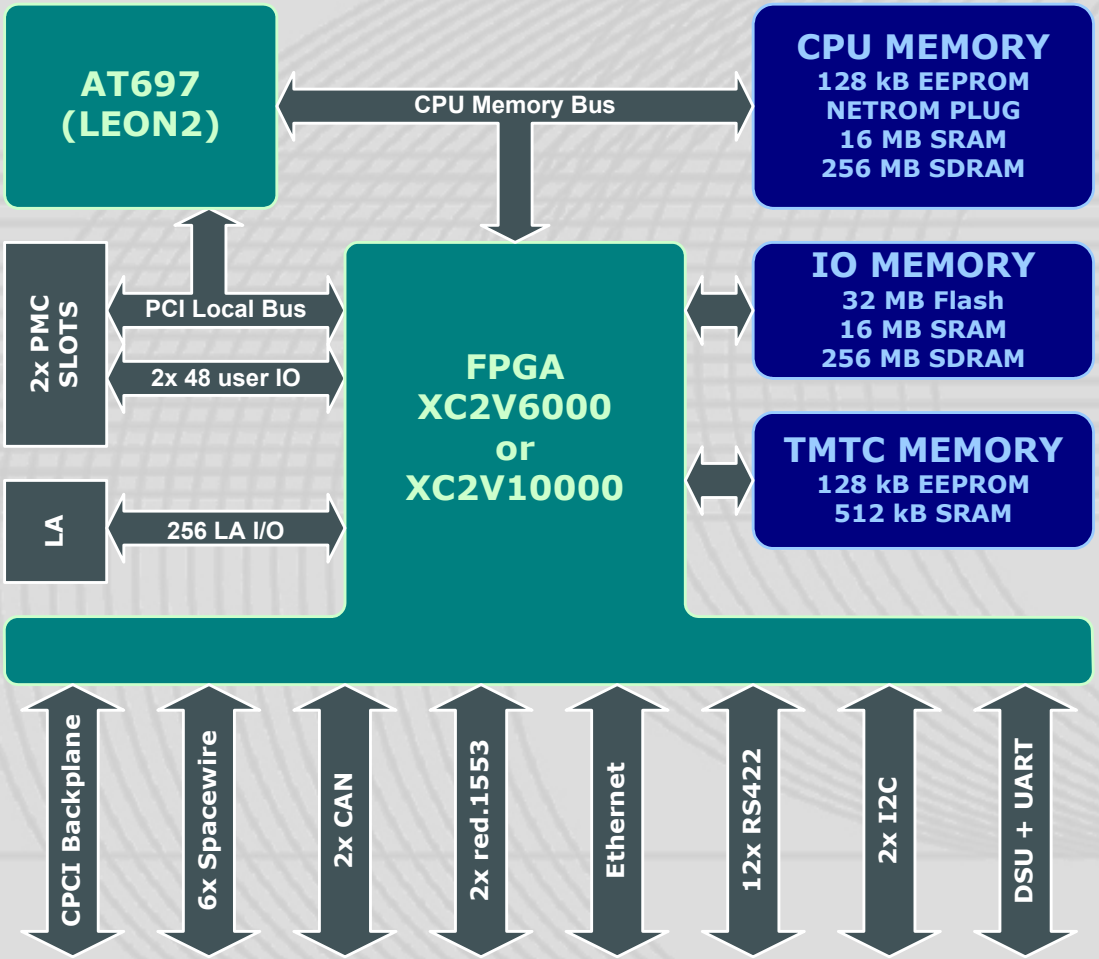
- **Check ability of LEON or AT697 based computers**
  - To allow SW development and to run SW applications developed for ERC32 target without problem
  - To achieve a performance in the expected target (benchmarking toward ERC32: x 4 expected)
  - To be tested and verified using state of the art test and validation methods and tools
  - To allow trustable simulation including through HW in the Loop solutions for Real-time verification
  - To be satisfactory observable and controlled using the Debug Support Unit
  - To allow SW traceability through dedicated test I/F (e.g SpaceWire)

Main evaluation activities performed

- **Engineering studies (based on datasheets, simulator, models or FPGA prototypes)**
- **Processor validation with AT697E on Astrium MAEVA board and application benchmark SW**
- **Tests on representative HW and SW**
  - Platform and P/L data processing and storage functions on commercial FPGA based development boards
  - Avionics control functions on breadboards with AT697E
    - MAEVA (Astrium)
    - LEOPARD (Saab Space)
    - JAGUAR (Saab Space - Ariane 5 avionics using Astrium Space Transportation requirements)

Recommendations are taken into account for processor Flight version (AT697F)

LEON and AT697 Developments: MAEVA (Astrium)



MAEVA board

Developed by Astrium Satellites in Vélizy-France

Main features

- AT697E @ 80 MHz
- Large Xilinx FPGA for SoC design or customized HW functions
- SDRAM dedicated to I/O functions
- SpaceWire, 1553, Can, I2C
- cPCI backplane

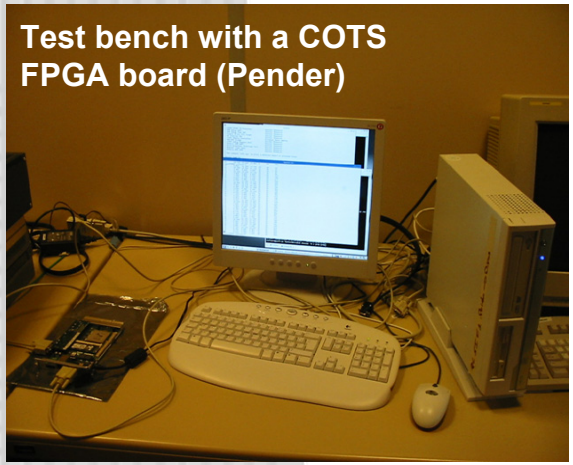
Flexible and versatile for architecture customization

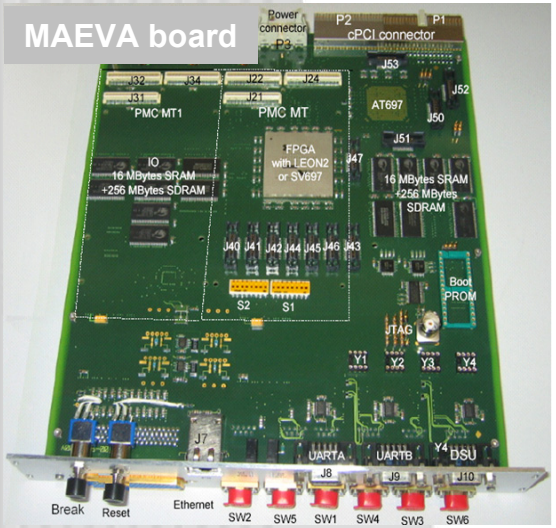
- AT697component and LEON 2 or LEON 3 IP can be alternatively used to explore different configurations, perform tests and SW benchmarks

Activities on COTS FPGA and MAEVA boards

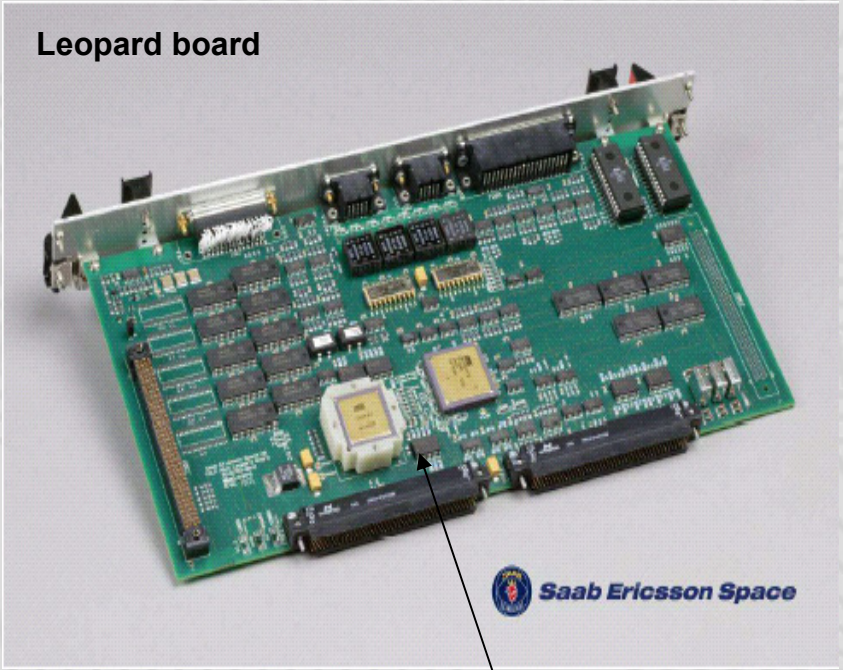
- **Engineering activities**
  - Leon based HW/SW co-design and tests on FPGA (MAEVA and COTS boards)
  - SW tests based on existing benchmarks and additional functions from Pleiades software
  - Use of SPARC V8 compiler option
  - Test with I/O functions
  - Support for the development of the in-house LEON simulator and the DSU commander

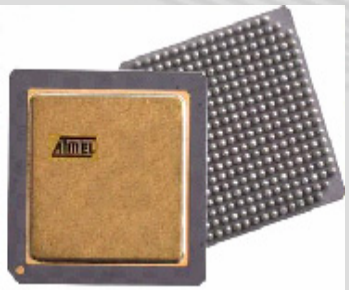
- **Validation of AT697E (with MAEVA)**


Test bench with a COTS FPGA board (Pender)



LEON and AT697 Developments: Leopard (SAAB)





Atmel AT697E
(LEON2)

Leopard board

Developed by SAAB Space in Gothenburg

Main features used

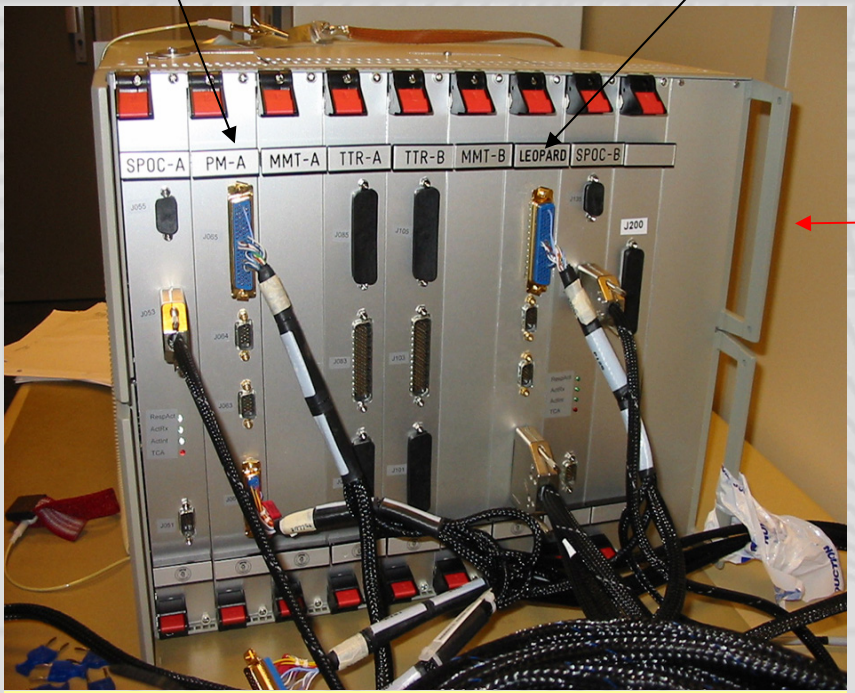
- Plug-in compatibility with Pleiades and Aeolus OBMU SDM
- AT697E @ 100MHz
- 4MB SRAM (2ws) EDAC& parity protected
- COCOS ASIC I/O controller
- 2MB SRAM exchange memory accessible via PCI
- DSU interface at 115 kBauds
- CPU UART I/F at 115 kBauds
- 1553B data bus interfaces
- Space wire interfaces
- OBT function

LEON2-FT SW portability assessment

Pleiades SW running on AT697 Board

Pleiades PM board (ERC32SC - AT695F)

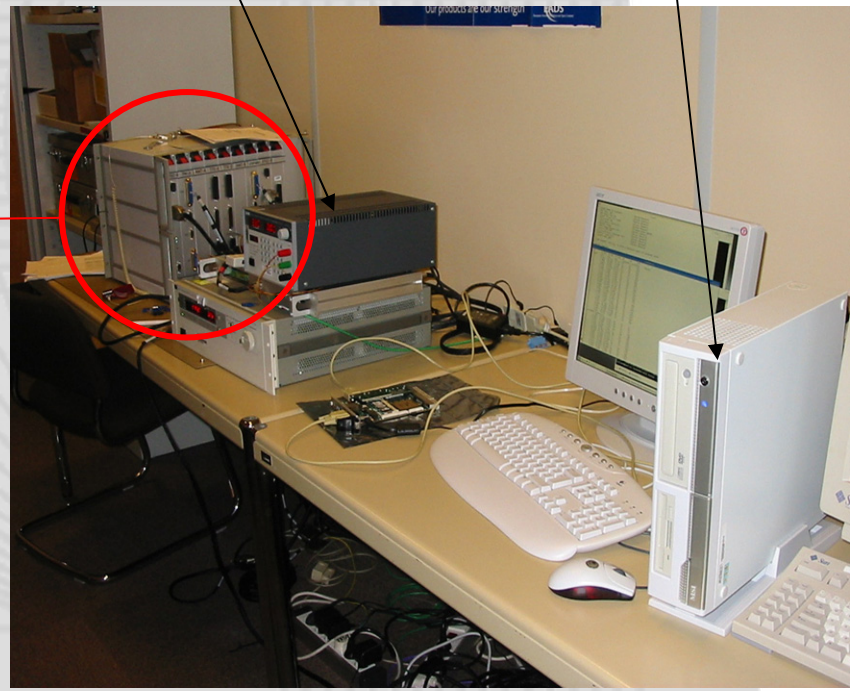
Leopard board (LEON2FT - AT697E)



The SAAB SPACE Pleiades OBMU breadboard with ERC32 and LEON2 boards

Power supplies, SpaceWire I/F and monitor equipments

LINUX PC with simulator, SIF and DSU monitor



Test bench for Pleiades SW portability assesment and benchmarking

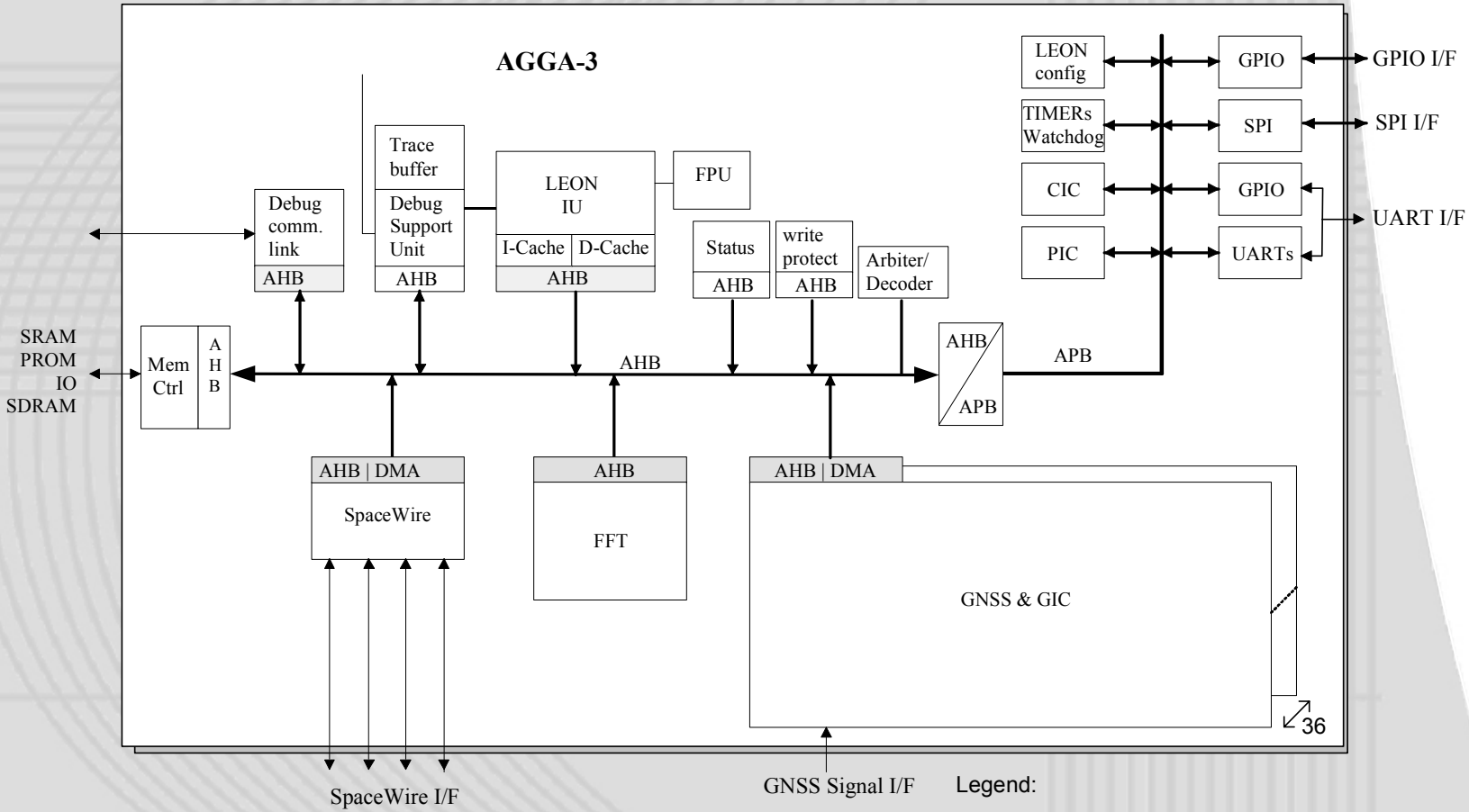
Developments in progress with LEON 2-FT

Advanced GPS/GALILEO ASIC: AGGA 3

- **AGGA-3 is under development at Astrium GmbH and Austrian Aerospace under ESA guidance.**
- **This radiation-tolerant, low power consumption new generation GNSS baseband ASIC includes:**
  - GNSS baseband processor
  - LEON2-FT fault-tolerant microprocessor
  - FPU (GRFPU)
  - FFT module, UART's
  - SpaceWire module with 4 I/F
- **The AGGA-3 chip will be manufactured by Atmel in the ATC18RHA technology and a MQFP package with 352 pins.**

Developments in progress with LEON 2-FT

Advanced GPS/GALILEO ASIC: AGGA 3



Legend:

GIC: GNSS Interrupt Controller
CIC: Communication Interrupt Controller
PIC: Primary Interrupt Controller

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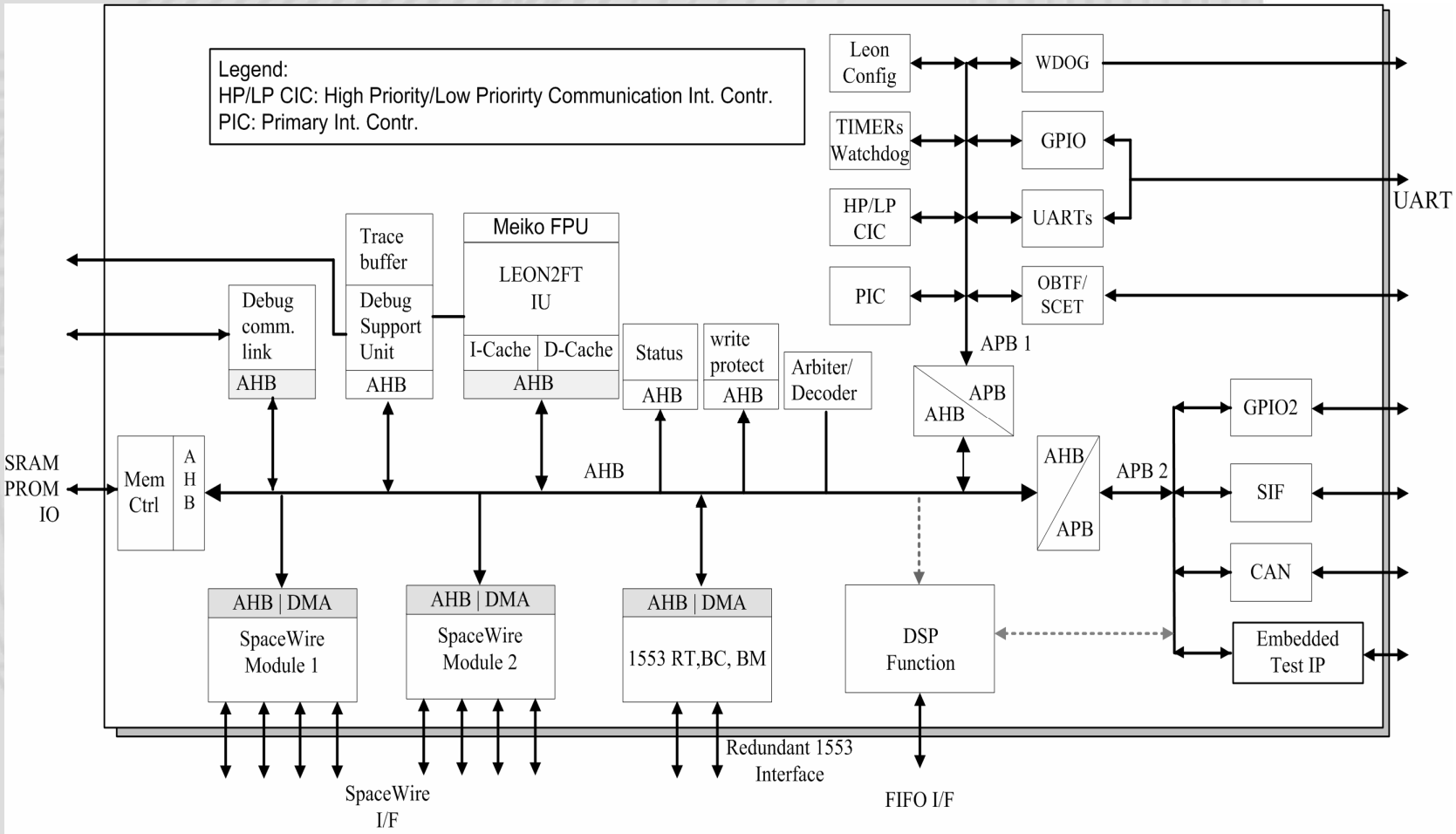
Developments in progress with LEON 2-FT

MDPA - Payload Control Processor ASIC

- **High Control Processing Performance using LEON2FT**
  - Scalable to multiprocessor system via SpaceWire with routing capability
  - MilBus interface with a S/C on-board computer
  - On-chip modem function for high speed TM/TC
  - 8 SpaceWire interfaces with the Data Path Subsystem
  - CAN bus interface for low rate data transfer between nodes and peripherals.
  - Interfaces for software debugging
    - Debug Support Unit
    - High Speed Service Interface SIF (based on SpaceWire) for Application software tests and timing/sizing
  - Test module for advanced JTAG boundary scan testing

Developments in progress with LEON 2-FT

MDPA - Payload Control Processor ASIC



Software Development environment

- **Astrium is working on an integrated development environment for all Sparc based developments**
  - Eclipse IDE environment
  - Gnu C software development environment
  - PC Cigwin host computer
  - RTEMS 4.6 cross compilation environment
  - GRMON tool for no real time debug and test procedure
  - SIF tool for real time and application debug
  - SIMERC32 and SIMLEON Astrium simulators

Outcomes from evaluation and developments (1/2)

- **One of the main advantage of the LEON processor is the availability of VHDL**
  - It allows the System On Chip approach to get compact and powerful processing devices
  - Prototyping becomes easier, faster and with lower cost thanks to commercial FPGA boards
  - Hardware and software can be co-designed rather early and in an incremental way
- **Software development on LEON targets is OK**
  - SW development tools are either identical to ERC32 (compiler) or natural evolution (simulator, RTEMS BSP).
  - LEON DSU is a new mean, easy to use and powerful

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Outcomes from evaluation and developments (2/2)

- **Performance increase versus ERC32 is between x2 and x5.**
  - Performance gain is difficult to predict since it depends a lot on the processing type and on cache effects
  - Parallel FPU can improve application performance when necessary (as for instance in the AGGA3)
- **Some concerns (with solutions)**
  - Observability (solutions: simulation, enhancement of on board debug support and high speed test interface)
  - Determination of WCET (solutions: estimation methods, cache control…)
  - Support of memory partitioning (solutions: improved memory protection scheme with AT697F, MMU)

Conclusion

- **Leon 2FT is a solid basis for building computers in the range 40-100Mips**
  - Development and test facilities are available and functional
  - Evaluation activities are successful (it works!)
  - Upgrade from ERC32 without major impact
  - Several implementation solutions based on current technologies (on FPGA or ASIC):
    - Using the LEON2-FT AT697 component
    - Systems on Chip using LEON2-FT Core with specialised functions and I/F in ASIC or FPGA
    - Other Systems On Chip with Leon 2 or 3 for FPGA or ASIC implementation.