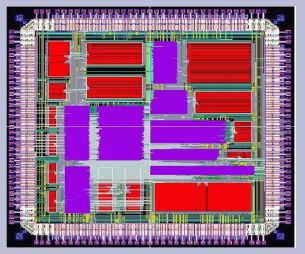
Gaisler Research



LEON2FT Modification

Memory interface

- **Asynchronous sampling of BRDYN**
  - Will advance BRDYN sampling one clock
  - New function selectable through bit in MCFG1
  - Back-wards compatible default setting
- **BRDYN can also extend PROM cycles**
  - To allow more that 30 waitstates (EEPROM write)
  - New function selectable through bit in MCFG1
  - Back-wards compatible default setting
- **Removal of 16-bit interface**
  - 16-bit PROM/SRAM/IO will no longer be supported
  - Only a configuration setting, no code-modifications
- **New RAM write protection scheme (TBD)**

On-chip peripherals

- **Counters extended to 32-bit**
  - Affects timer1, timer2 and watchdog
  - Down counting should make change transparent
  - Scaler remains 16-bit
- **Four additional interrupts**
  - Allows generation of irq 10, 12, 13 & 15 from IO port
  - Any I/O port input can be used
  - Back-wards compatible irq 4, 5, 6, 7 generation
- **AHB trace buffer can be frozen in debug mode**
  - Extra control bit in DSU ctrl reg to freeze AHB trace buf
  - Back-wards compatible default mode

Additional changes

- **Merging of ESA provided patches**
  - Improvements to PCI TMR registers and reset
- **Fixing of all bugs in current AT697E bug list**
  - Done.
- **New test benches**
  - New features will be covered by basic test bench

Not implemented modifications

- **Asyncronous sampling of BEXCN**
  - Not needed
- **Additional hardware breakpoints**
  - Not feasible (timing)
- **Cache locking**
  - Not possible to protect lock bit (FT)
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- **Reed-Solomon SDRAM ECC**
  - Pin-out compatibility could not be retained
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- **Reduction of ICC branch delay**
  - Not possible due to timing