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Introduction to the Evolution from the AT697E prototype to the AT697F flight (update of the LEON2-FT)

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LEON2-FT Update Objectives

The two main objectives of the update of the model of the LEON2-FT:

- Correct the design deficiencies that have been identified since the design of the LEON2-FT prototype
- Improve the functionalities of the AT697 at the request from the European space user community

I will not present to you all the details of the above, that will be done in the next presentation of Gaisler Research.

I should like only to shortly describe the following two items:

- Improvement of the PCI model (ESA)
- Addition of a new Write Memory Block Protection (ERC32 compatible)

PCI Changes AT697E → AT697F

#	Problem/Feature	AT697E	AT697F
1	PCI CLASS CODE field (bit 31:8 @0x08)	Meaningless value 0xB	0xB4000, which stands for processor/co-processor device1
2	Internal readability of the external bootstrap pin SYSENN allowing boot SW and OS to distinguish between host and satellite mode and to load the respective drivers	Not implemented	readable in bit 12 of the Master Status register (@0x54)
3	Internal readability of the PCI configuration registers (@0x00 - @0x40) which (in satellite mode) can only be programmed from outside, through the PCI bus.	Not accessible at all from inside the processor (reading only returns the reset value)	can be read from inside, thus allowing the SW to know e.g. which PCI address it has been mapped on
4	Handling of 64 bit transactions (load/store double) either as 2-word burst or as 2 successive single words	configurable by bits 1 and 2 in the master set register (@0x58)	Choice decommitted (config bits read-only = 0), and the PCI interface always executes 2-word PCI bursts
5	Problem with certain combinations of PCI target transactions (write after delayed read), in combination with long AHB wait states (e.g. when accessing slow PROM or I/O devices).	May cause a deadlock because the write wipes out the earlier read request which will then never be satisfied	Fixed by forcing a retry until it comes to a correct repetition of the read transaction. This force-retry can be observed or stimulated with bit 8 of the target status/command register (@0x60)

Note: the expression @0xAB means "at address 0xAB of the PCI configuration space"

New Write Memory Block Protection for the AT697F: the problem

- Presently the AT697E is using a TAG (start address) and a MSK (mask) fields in the WPR1 and WPR2 registers to control two MBP units allowing to define two memory areas that can be write protected or write allowed
- The use of mask is a choice going back to the early phase of the design of the LEON1-FT and it was motivated by time constraints of the target technology envisaged at that time
- The drawback of that approach is the poor granularity of the block size choices (32 KB, 64 KB, 128 KB, …) and the associated start address alignment constraint
- In addition a bug has recently been found in one of the four possible combinations of operation that make that configuration impossible to use

New Write Memory Block Protection for the AT697F: the solution

- The bug in the present MBP units will be corrected
- Two additional new MBP units will be added that are compatible with the ERC32 memory protection scheme that offers much more flexibility and word granularity and will ease the software portability from the ERC32 to the AT697F

Next Presentation

That is the end of my presentation

The next presentation by Gaisler Research will detail the update of the model and the validation of the updated model