Microprocessor to Microcontroller
When, Which and Why

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Context

- MESA Context: microprocessor ⇨microcontroller
- Applications
- Top Level Requirements
- Microcontrollers at Astrium
- Trade-off
- Preferred Characteristics
- Conclusions

Introduction

- Microprocessors are providing increasing performance and are attractive for complex control and processing tasks such as that required for the on-board Avionics.
- but Microprocessors come at a “price”:
  - Resource hungry requiring large (fast) memories and busses
  - High pin count packages (sometimes CGA) requiring a sophisticated mounting process
  - Provide many features and interfaces which are not required for simpler applications
  - Consume power and board area (or gate count if IP block)
  - Sometimes restrictions on IP versions if the user wants to create his own “System On Chip”
  - Formal verification and validation process for software can be costly
- Microcontrollers are an attractive alternative.

MESA Context

- A Microcontroller is a component for data acquisition and simple controlling applications.
- A single component (physical and IP block) able to fulfil requirements coming from all space embedded applications:
  but low price, low pin count (easy to assemble package), low power consumption ⇨ is this a contradiction?
- A new physical development should consider the feasibility to include in a single chip additional functions and interfaces to lever advantages of miniaturisation and thereby to simplify the design of the surrounding electronic circuitry ⇨ business case!
- The availability of Software Development Tools is a key point in the selection of the best solutions
  ⇨ spin-in of a successful commercial product.

Microcontrollers enable flexibility

- A standard VHDL approach using anti-fuse FPGA or ASIC technology dictates that the requirements and the implementation are frozen early in the development cycle.
- A microcontroller adds flexibility:
  - During design if customer specification is not stable enough
  - After design because:
    - It allows correction of errors without re-design of ASIC/FPGA
    - Microcode may be downloaded when Flight Unit is already delivered to adapt the design to a new customer requirement or to fix an equipment bug (e.g. in the IEU project where it was possible to adapt the equipment thanks to use of the PIC microcontroller)

Microcontroller for Astrium: Applications

- Small ICU / large RTU
- Mechanism Control
  - Cooler
  - Motor
- Nand Flash Controller (low level)
- Compression Controller (low level)
- Active Antenna Controller
- Power Control

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Microcontroller for Astrium

- Real-time application support
- Limited (but expandable) address range: 64k data + 64k program
- IP version mandatory: < 10kgates, ideally ~ 2kgates (so that use in SX FPGA's feasible); not clear whether need for hard or soft IP
- Standard Development Tools:
  - C support + assembler
  - Emulator / Debug I/F
  - Simulator
- IP formally validated with justification file (⇨ mature technology)
- Low cost IP and preferably no royalties
- Low cost physical implementation (0.18µ or DSM?)
- Only integer (no floating-point)
- Alternative IP suppliers (open source?)
- Capability to handle various data types (16-bit ➔ 32-bit)
- Availability of I/F block to Amba Bus

Candidate Microcontrollers

- RISC 51 family, e.g. 8051
- PIC
- ARM Cortex, e.g. M1
- LEON (probably downsized)
- ATMega128/AT90CAN128

RISC 51 Family

- Atmel 80C32 used in many instances at Astrium including
  - Atmel 80C32 for Helios 2 MCM (mechanisms control)
  - Atmel 80C32 for Spainsat & Isdesat IRMA antenna control
  - Atmel 80C32 for NASA MSL instrument

  but component is now obsolete.
- Additional Experience
  - Dallas 80C320 for ISS (AMS-02 cryomagnet avionics)
  - Evatronics R8051 IP core for Coolers (ESA GSTP)
- Key Advantages:
  - Good SDE and emulator support. SW reuse.
  - Simple system & inexpensive solution (8 bits buses).
  - Low cost IP core for System On Chip.

PIC

- Astrium has applied an 8 bits PIC microcontroller: the **SLC1657** (Silicore IP from Microchip Microcontroller)

→ Successful Experienced on WICOM, COMS IEU, COME and CORECI.

Consequences of using PIC IP (µcontroller)

- Program download and program dump functions are needed to load, modify or verify the firmware
- Design is seen as a set of registers by the microcontroller, some of them being reserved for microcontroller calculations
- SRAM may be needed (with an SRAM management function)
- The SLC1657 PIC can manage “only” 2K instructions, therefore microcode shall be optimized to fit into a 2K program memory, or shall implement a page management to be able to virtually have access to more than 2K
- Hardware simplified but Software is needed

Impacts of using PIC IP (µcontroller)

Design flow impacts :

- SoftWare and HardWare developments are parallel processes that meet together during VHDL simulations
- Microcode is Firmware, not Software… especially because the PIC IP does not manage interrupts

  → microprograms can be seen as “deterministic” and linear (no interrupts)

Planning impact :

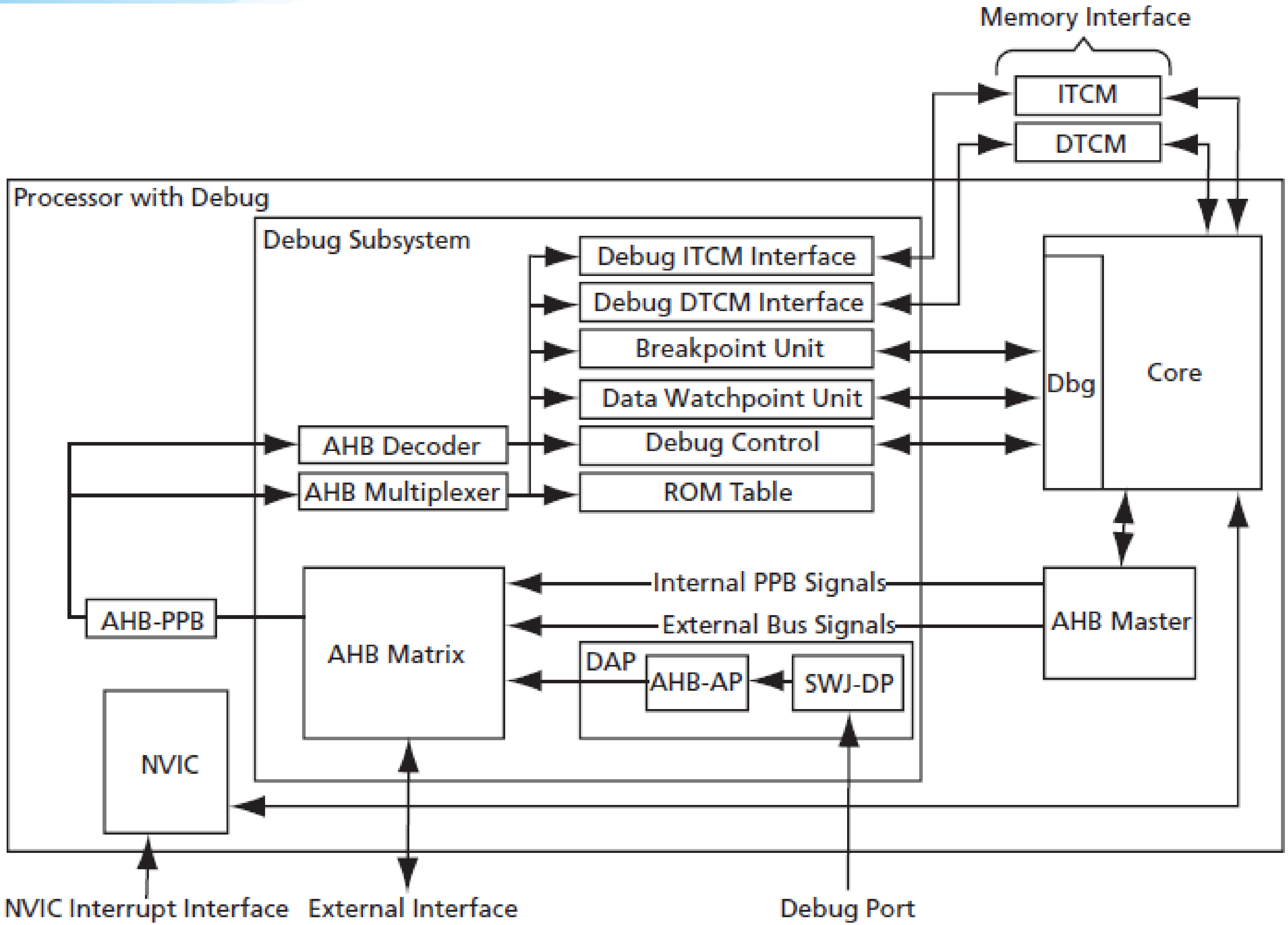
- Around 4 months for a microcode of 2 K words (IEU experience)
- But … a lot of time saved due to hardware easier validation and flexibility

ARM Cortex M1 Experience

- Modern use of ARM Cortex M1 for on board antenna control (‘Paz’ satellite) and cooler control applications
- Antenna Control Electronics for ‘Paz’ satellite
  - Spanish EO Radar system.
  - In charge of calculations of the antenna phase & gain parameters for every radio-frequency unit and synchronous transmission of the parameters to the antenna elements.
  - Communication with the data handling subsystem
  - Implementation into 1 RTAX2000 FPGA
  - System currently running in BB and EM models (ProASIC FPGA version).
  - Project Status: PDR preparation
- Cooler Drive Electronics
  - Proposed for CSO (post-Helios mission)
  - And intended to use for MTG.

Why ARM Cortex M1 microcontroller?

- Performance
  - 32-Bit RISC Architecture (ARMv6-M). 32-Bit Memory Addressing Range
  - 32-Bit AHB-Lite Bus Interface
  - 3-Stage Pipeline
  - 32-Bit ALU
  - Embedded ICE-RT Real-Time Debug Unit & JTAG Interface Unit
  - Up to 60MHz operation (typically). 1 instruction per clock cycle.
  - Specific version oriented to FPGA implementations
  - Fully predictable (no cache)
- Development & dev. Environment
  - Proven in millions of applications
  - Consolidated development environment (software and tools): Keil microVision
- Size
  - 30% of RTAX2000 resources (just 24% if debugger not included)
- Inexpensive licence for FPGA


Memory Interface
ITCM
DTCM
Processor with Debug
Debug Subsystem
Debug ITCM Interface
Debug DTCM Interface
Breakpoint Unit
Data Watchpoint Unit
Debug Control
ROM Table
AHB Decoder
AHB Multiplexer
Dbg
Core
Internal PPB Signals
External Bus Signals
AHB Master
AHB-PPB
AHB Matrix
DAP
AHB-AP
SWJ-DP
NVIC
NVIC Interrupt Interface
External Interface
Debug Port

ATMega128/AT90CAN128

- high performance low power 8-bit microcontroller
- advanced RISC architecture up to 16 MIPS @ 16 MHz
- 128 kBytes in-system programmable flash memory
- SPI Interface for In-System Programming
- Data retention: 20 years at 85°C/100 years at 25°C
- 4 kBytes EEPROM
- 4 kBytes internal SRAM
- further built-in features are:
  - Master/slave TWI serial interface (I²C bus interface)
  - An 8-channel, 10-bit AD converter with programmable gain set used for the inputs of primary current and temperature signals
  - 53 digital I/O lines.
- CAN bus interface (AT90CAN128 only)
- used in EML-ECE Power Supply Unit on ISS for input current and temperature measurements as well as commanding

Micro-controller for Astrium: trade-off

Parameter	**Risc51**	**PIC**	**Cortex**	**Leon**	**ATmega**	**Comment**
Address Range	-	- -	+	+	--	
Bus Width (⇨ memory)	+	+	++	++	+	
IP available	+ +	+	+	+	+	
IP Price/Licensing	+ +	+ +	++	-	-	ESA will not licence LEON2 FT IP for FPGA
Gates	**8k**	**2k**	**~15k**	**~20k**		
Tools	+ + +	+ +	+ + +	+ +	+++	
Formal IP Validation	**(+)**	**O**	**(+)**	+	-	@ ESA/CNES
Alternative Suppliers	+ +	-	-	-	--	
Data Type Support	-	-	+	+ +	++	
I/F Block to Amba	-	-	+ + +	+ +	--	
Astrium Experience	+ +	+	+	+ +	++	
Code Density	+ +	-	+ +	+	--	
Usable in FPGA	+ +	+ +	+ +	-	--	

Astrium Preferences I

- Preferred architectures and instruction sets
  - Downsized LEON if FPGA IP licence
  - Cortex if price ok; 8051 as backup
  - ITAR free technology
- Necessary processing performances
  - Few MIPS, deterministic execution time
- Power consumption requirements
  - Low as possible (< 200mW)
- Which and how many peripherals/interfaces are needed
  - On chip 8-channel multiplexed ADC (12bit, 100ksamples/sec)
  - UART with standard serial interface (RS232, RS422)
  - CAN bus (tbc)
  - SpW (tbc)
  - SPI (tbc)
  - PWM 3 channels minimum
  - GPIO
  - Internal memory and memory extension

Astrium Preferences II

- Specific needs (internal memory, power down modes, analog blocks etc)
  - 128kbytes internal memory, internal EEPROM (tbc)
  - Power down mode
  - ADC and PWM
- Package and quality grade requirements (DIL, QFP etc., pin count)
  - QFP, < 250 pins, easy to mount/assemble on PCB
- Temperature range and radiation requirements (TID and SEE)
  - Military temp, 100krad, SEE free
- Preferred programming languages and operating systems
  - C, assembler, scheduler rather than OS
- Requirements for software development & debugging tools
  - JTAG Emulator, simulator

Conclusions

- Astrium primary need for a microcontroller as IP for FPGA (and maybe ASIC) implementations; but also some applications require a component.
- Microcontroller should support deterministic software thereby minimising the effort for validation.
- Downsized LEON could be an attractive approach but availability as an IP for FPGA (ASIC) implementations to be assured and tools adapted accordingly.
- The ARM Cortex M1 is a modern inexpensive (FPGA licensing) product with good interfacing and excellent tools.
- The RISC 51 (8051), although dated & with some deficiencies regarding address range, data types and interfaces, is a low cost solution with continuing potential for some applications.