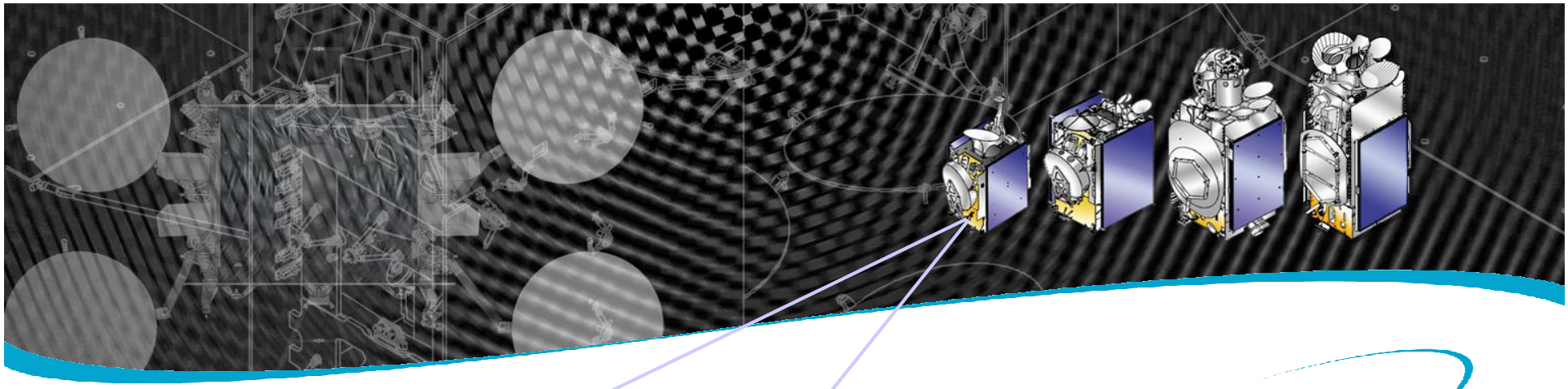
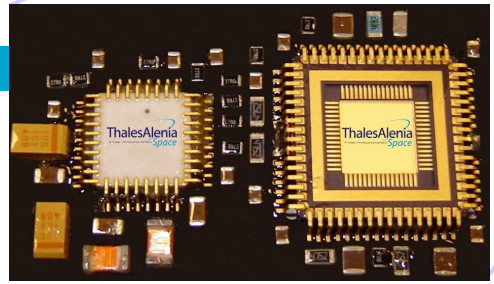




Digital Control for Space Power Management Devices

Work conducted under ESA Contract nr.21826/08/NL/LVH

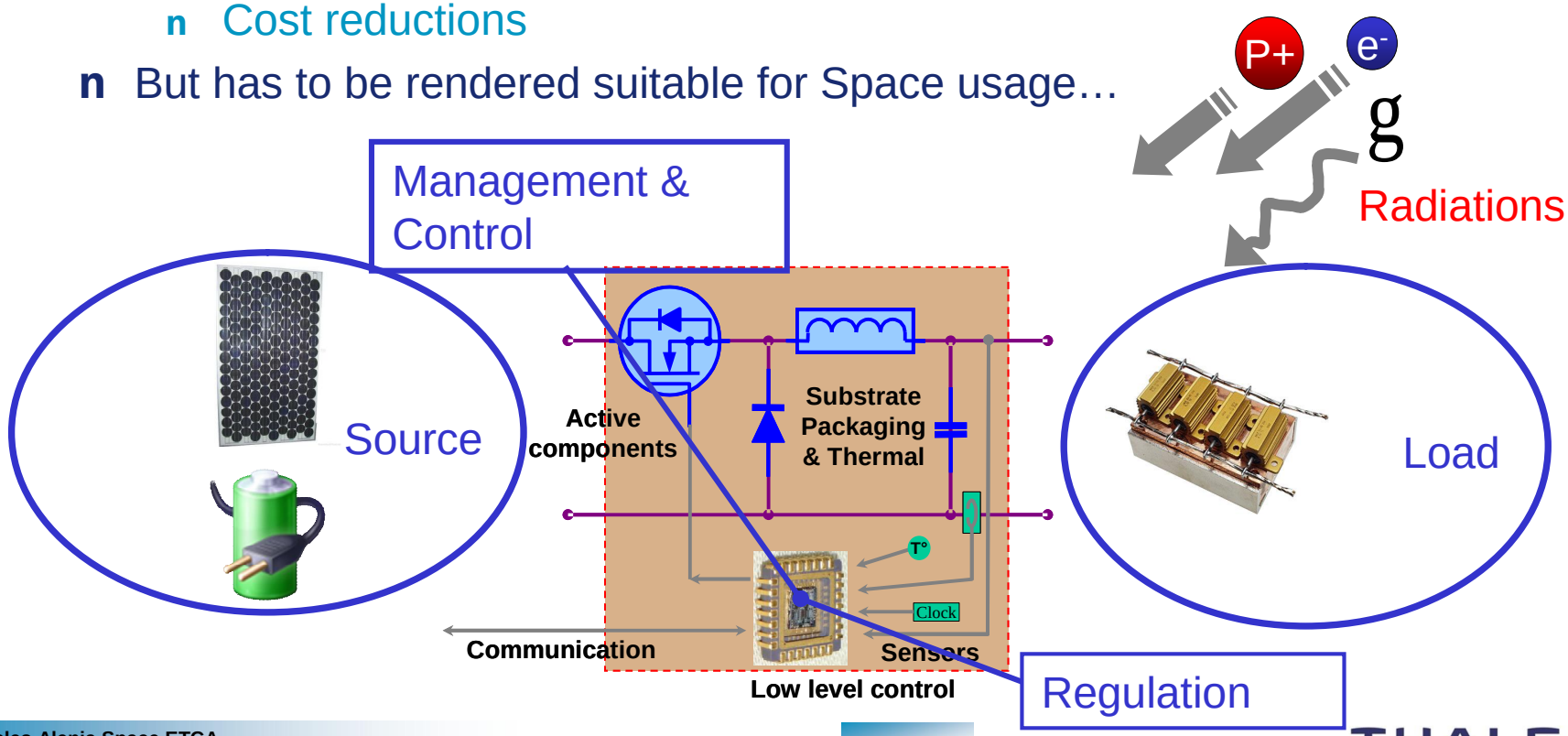
Thales Alenia Space ETCA

Ref : HMCU-ETCA-TN-0448
Date : 4/11/2010 M. Fossion

Template reference : 100182079N-EN

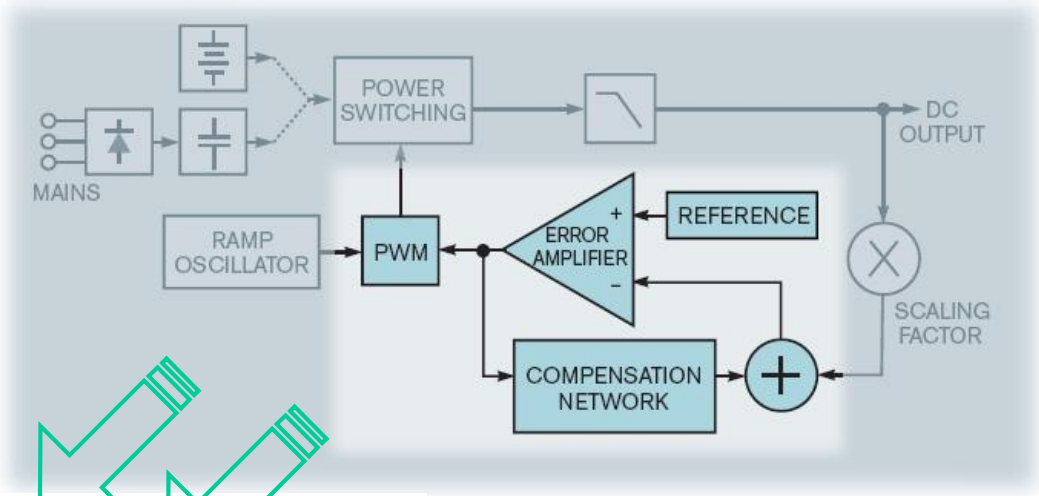
DIGITAL POWER CONTROL

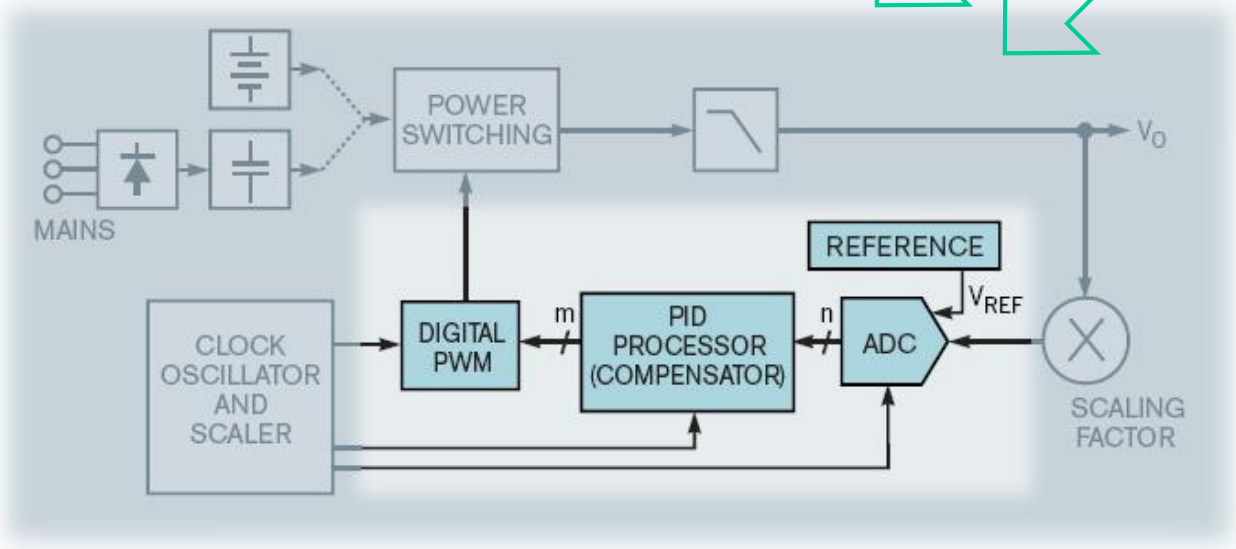
- Management of power devices via digital rather than analog techniques
- A high-growth domain for the past five years on ground
  - 45% growth predicted by 2013 (Darnell – Feb. 2009)
- Brings about
  - ‘Flexibility’
  - Cost reductions
- But has to be rendered suitable for Space usage…



DIGITAL Vs. ANALOG CONTROL

An analog SMPS control loop compares a scaled sample of the output voltage with a fixed reference and controls the PWM timing to force the two quantities to match.



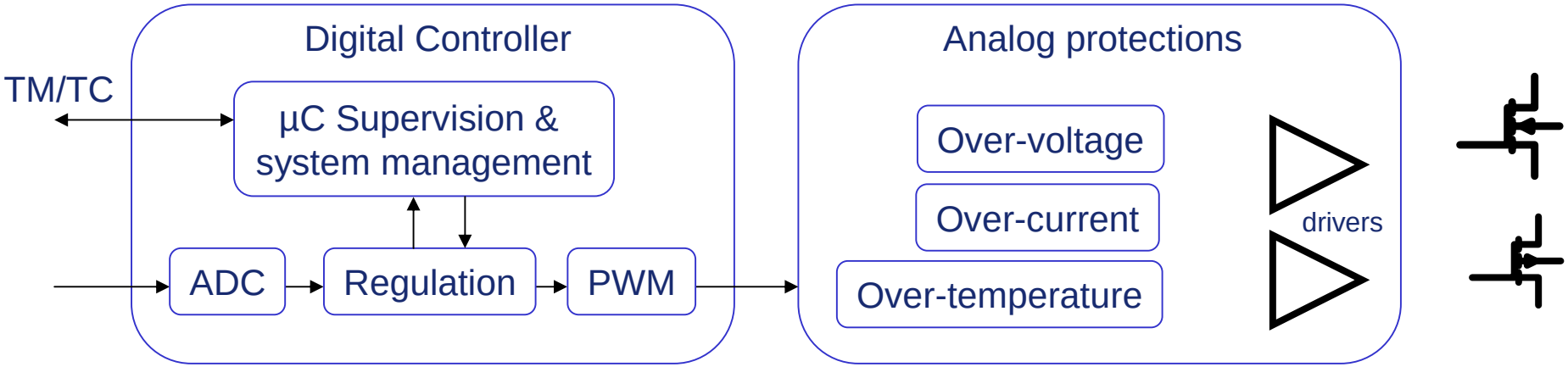


A digital SMPS control loop replaces the error amplifier with an ADC. The digital PWM requires a high-speed clock to provide the necessary edge-timing resolution.

A BIT OF POWER digitally controlled power conversion
JULY 21, 2005 | **EDN** 59-66
BY JOSHUA ISRAELSOHN • TECHNICAL EDITOR

ECSS E-20: “Any protection function of a power converter or regulator preventing failure propagation shall:

1. not be implemented in the same hybrid cavity or integrated circuit, and
2. not utilize common references.”



- A FULL-CUSTOM ASIC CHIPSET
  - MIXED-MODE REGULATION AND CONTROL UNIT
  - ANALOG PROTECTION CHIP
- FOR INTELLIGENT POWER MANAGEMENT

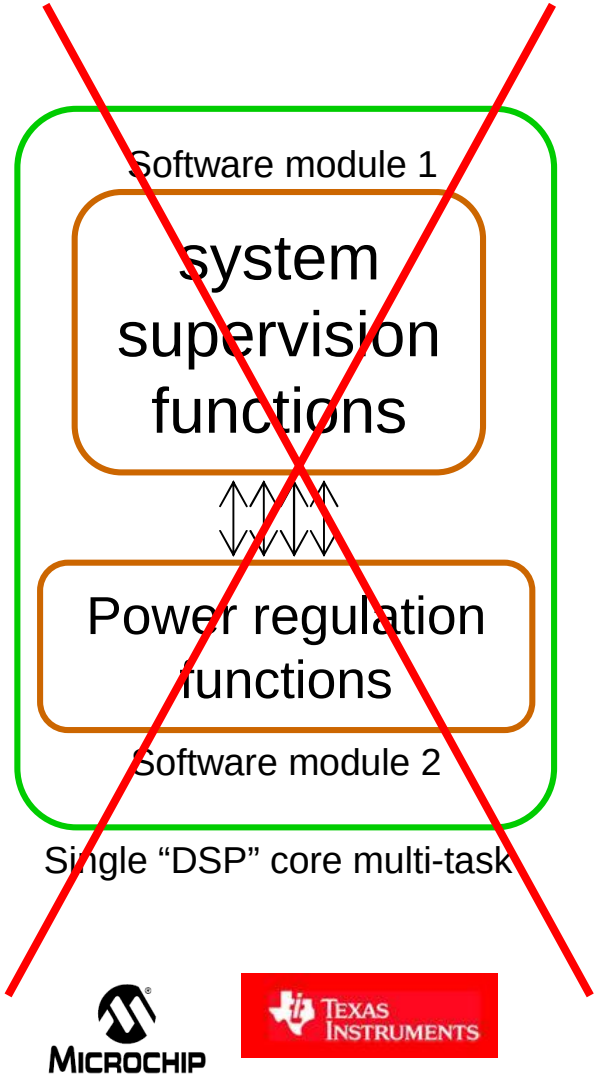
Layered approach

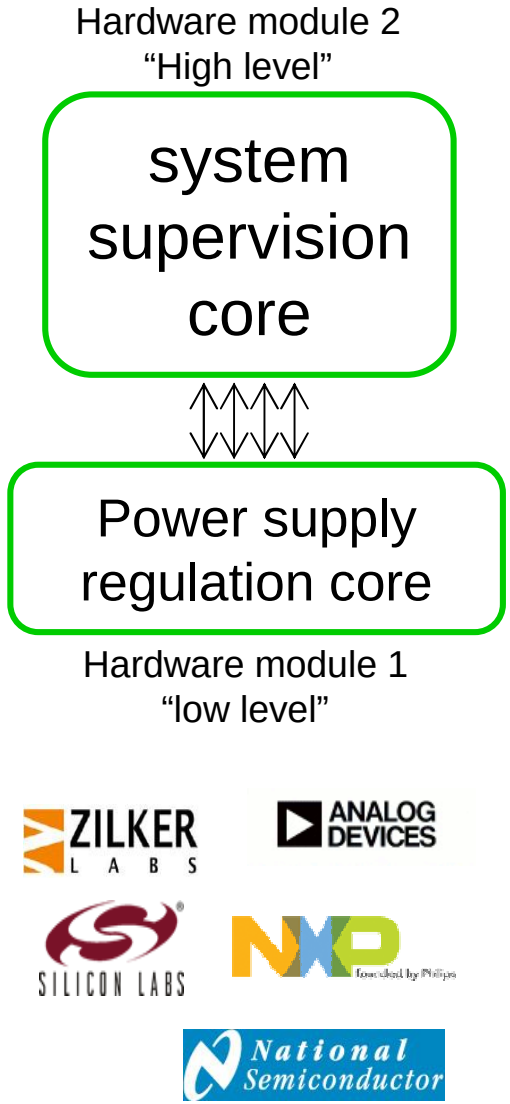
There are 2 main tasks to perform:

1) the main regulation

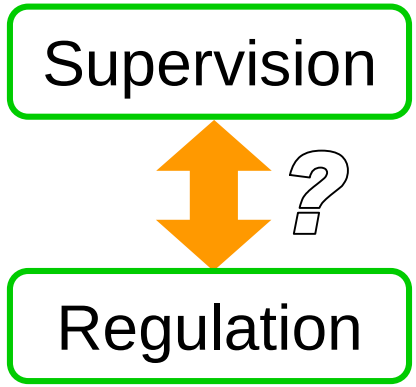
2) the supervision & control of this regulation

There 2 implementation options …





Implementation trade-off



Single DSP core performing multi-tasking.

- The 2 tasks are 2 software modules

Two optimized independent hardware modules

- Talking to each other via a dedicated interface

Trade-off analysis:

- Independency of the main action & the supervision of it is much better for reliability.
- Formal method used to demonstrate “bug free” are much easier if there is only 1 process without interrupts & multi-tasking.
- Return of industrial applications show that an optimized “hardware” engine for the power regulation consumes less energy: the complexity of the regulation functions is so much simpler that running a power-full DSP is a waste of resources

Features

On chip …

- **non-volatile memory**
- **6 high speed ADC with differential inputs**
- **3 DAC**
- **Configurable glue logic**

Serial data communication module

- **þ 1553, OBDH, UART, SPI, I2C**
- **¨ CAN, SpaceWire**

Digital fast regulation engine: math sequencer

Digital PWM generator with 6 complementary (6x2) outputs.

Low pin count … 68pin CQFP

Supervision & system management µC

Low end CPU

- Manipulating integer 16 bits / float data
- 10..15 MIPS

Code size is small ~12 kbytes

Timers, watchdog …

Debug functions (step by step, breakpoints …)

Role1 = System state machine

- Startup, shutdown sequencing features of a power supply function
- Alarms management and reporting
- Time keeper

Role2 = Optimize equipment level performance

- Dynamic updates on the regulation (floating point)

Other possible chip usages

Client Bus / remote IO

- OBDH, 1553 … I2C, SPI, UART serial interface
- Hot / Cold redundancy (connection to both/either nominal/redundant bus)
- General purpose analog & digital IO controller

Gateway

- Protocol translation
- Eg. 1553 satellite OBC ↔ equipment specific protocol

Remote intelligent sensor

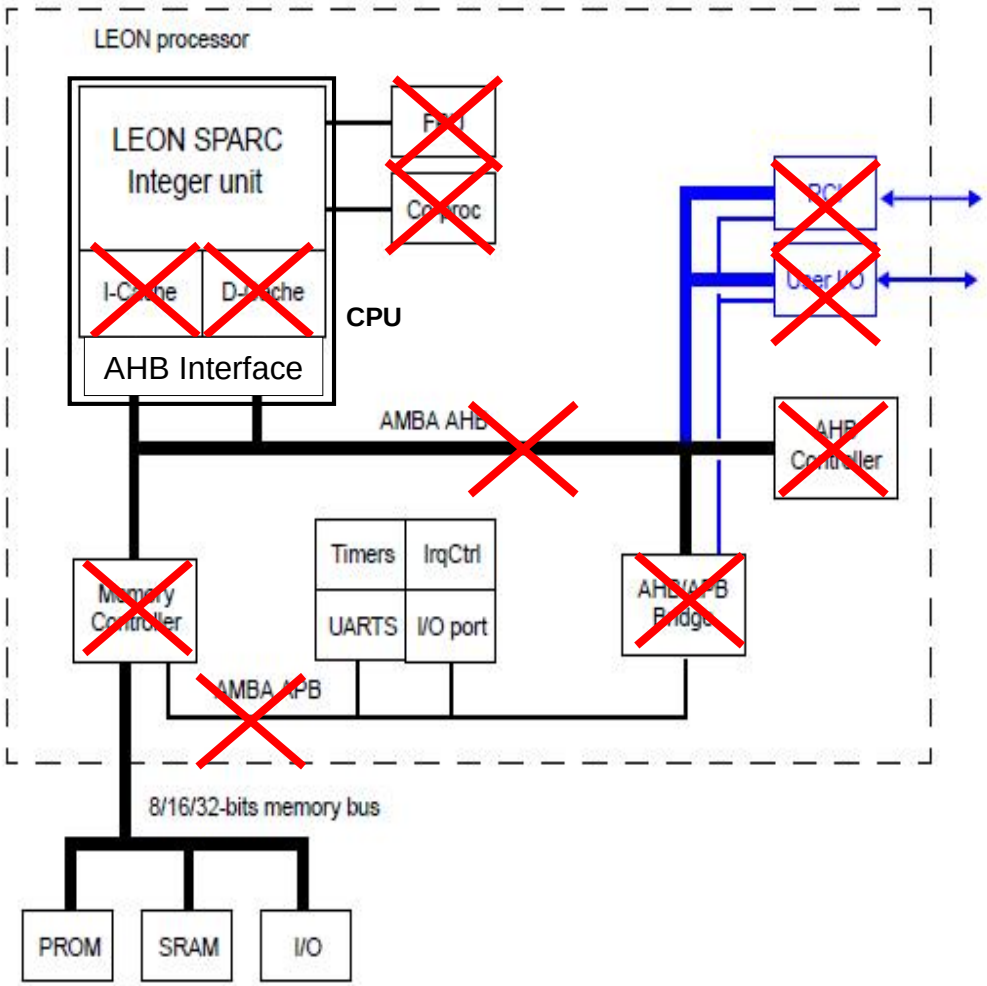
- with I2C, SPI, UART serial interface
- Eg. LVDT / resolver
  - Generate stimuli, measure response, preprocess data
  - Accept commands & report value

General purpose µC

- With PLL, ADC, DAC, PWM generator, NVM, watchdog, GPIO …

Digital DPC – Light LEON 2

q Useless functions (to deactivate, to remove) :



q PxcoBlaze

- **PicoBlaze** is a proprietary 8-bit RISC architecture and a CPU soft core developed by Xilinx. Although available free of charge, the core is tied to a Xilinx FPGA architecture, was designed to operate in low-density FPGAs and occupy about 100 Spartan/Virtex slices.

- **PacoBlaze** is an open-source clone (released under the modified BSD license) of the **PicoBlaze** soft core. **PacoBlaze** is a device-independent CPU core binary-compatible with the original **PicoBlaze** and written in Verilog-2001 since Aug 2004.

Summary

	Light LEON2-FT	8051	Modified PacoBlaze
CPU power	Oversized	OK	OK
Bus width	32bits K future safe	8bits K (code size!)	16bits J OK
License	Exclusivity	OK	No issue
Effort for Tooling C code & Debug support	None	Light / medium	heavy
Heritage & sales support	J J (space community)	J (well known)	L (whole doc & support from ETCA only)
Community support	Medium	Large	Little
Float	J	L (code size!)	L (library adaptation)
Timing predictibility	L Pipeline !	Instruction dependent	Simple
Risk	IP bugs (Large Complexity)	IP bugs (Med. Complexity)	IP bugs (Low. Complexity)

SW dev. Tools

Our applications are mostly « Mission critical » (DAL-B ref. DO-178B)
This class of SW is expensive to develop.

Besides “regular” tools such as

- Compiler
- Debugger (step by step & breakpoints)
- Emulator
- Simulation environment.

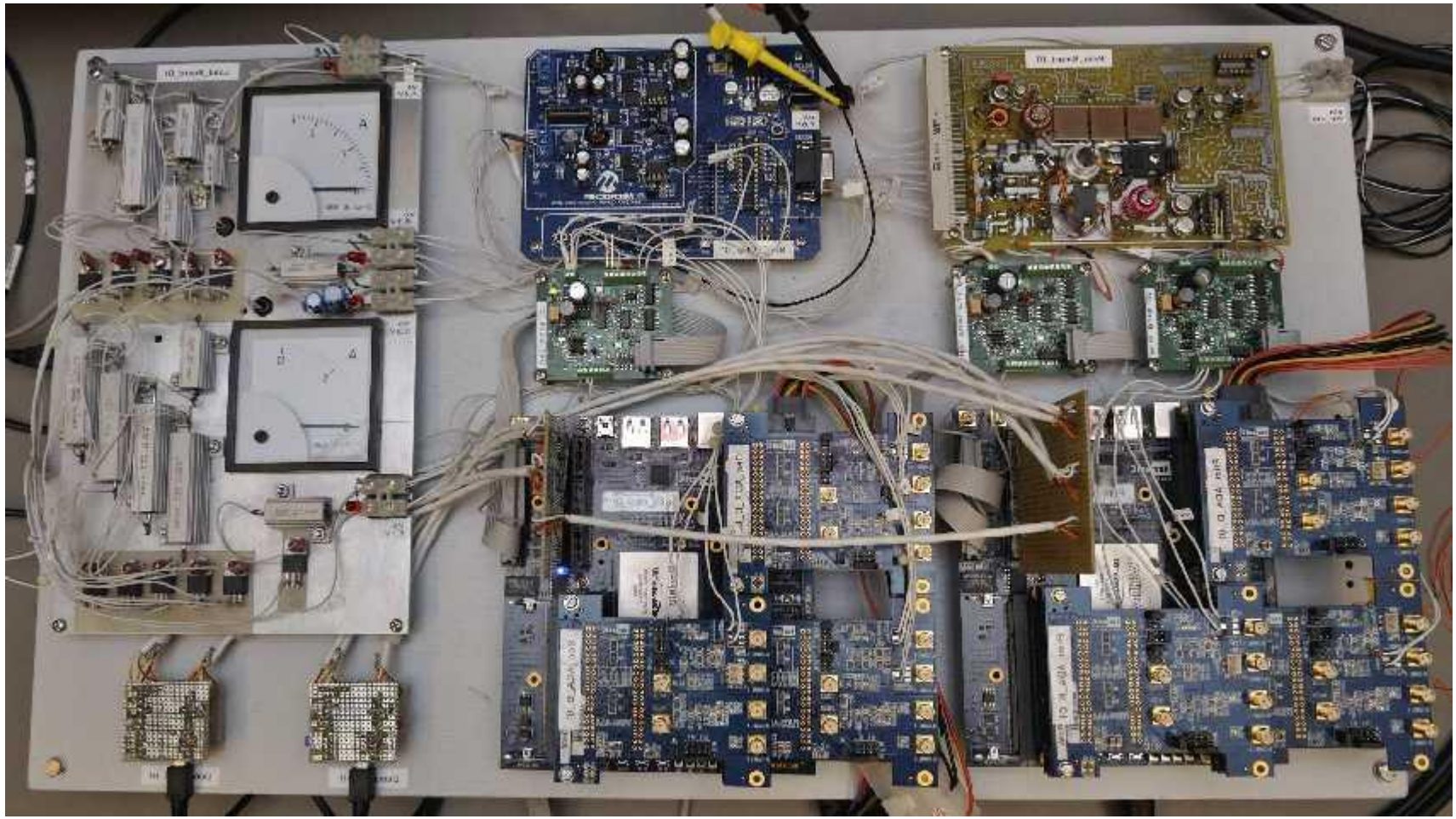
Some tools are useful to make life easier such as

- C code verification « Polyspace »
- Traceability tools « Doors »
- Automatic test pattern generator & Code coverage analysis tools

Esterel Scade tool suite

- From a high level modeling quite a lot of task can be automated
- Has large references in aeronautics (DO-178), recently ECSS !
- Under investigation if not a too large tool for small code sizes

Photo of our breadboard



Conclusions

Thales Alenia Space ETCA

- Is developing a digital power control chipset to offer more flexible power conditioning products.
- Feasibility has been assessed & demonstrated for space product

This is nothing but a general purpose µC with

- A large set of peripherals dedicated to analog & digital interfacing
- Regular communication capabilities
- A dedicated core supporting time critical regulation functions.

The embedded on-chip non-volatile memory & analog functions are key drivers to reach very low cost targets.

Light LEON core would be a nice candidate for the “supervision & system management core” of this chipset