V8uC: Sparc V8 micro-controller derived from LEON2-FT

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Introduction

V8uC is an ESA project to realize a 32 bit micro-controller from LEON2-FT core data-base

From CPU to micro-controller a new simplified memory data path had to be designed

Design approach of reuse of large parts of the LEON2-FT core:

→ to reduce design timing and risk

→ to inherit its SW tools and libraries

Changes minimized to not reintroduce errors in debugged components

Topics

- Target application
- Architecture
- New Features
- SW development tools
- First numbers
- Conclusion

Target applications

Embedded sub-systems where LEON features/costs exceed, but not cover effective requirements.

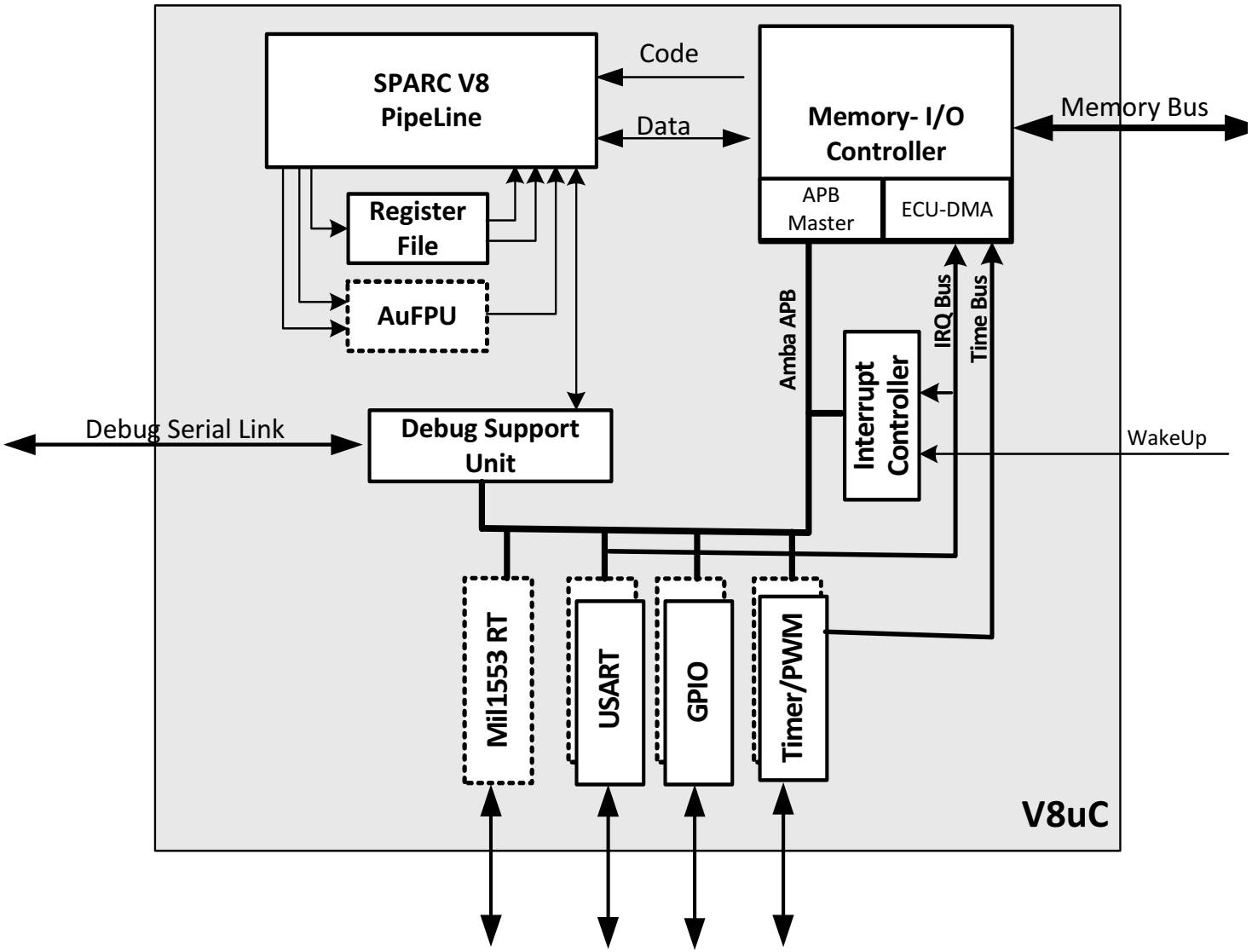
- Closed control loop applications
- Acquisition and serialization of multiple discrete or analogue signals
- In-line data elaboration

→ No real Operative System but only scheduler loop
→ Memory data path simplified with on chip local memory (64/128 Kbyte) sufficient to keep entire application
→ Option for Remote boot via serial link
→ Several I/O lines and serial peripheral interfaces

The objective is to cover I/O or control boards requirements without need of additional FPGA design

Architecture : Block diagram

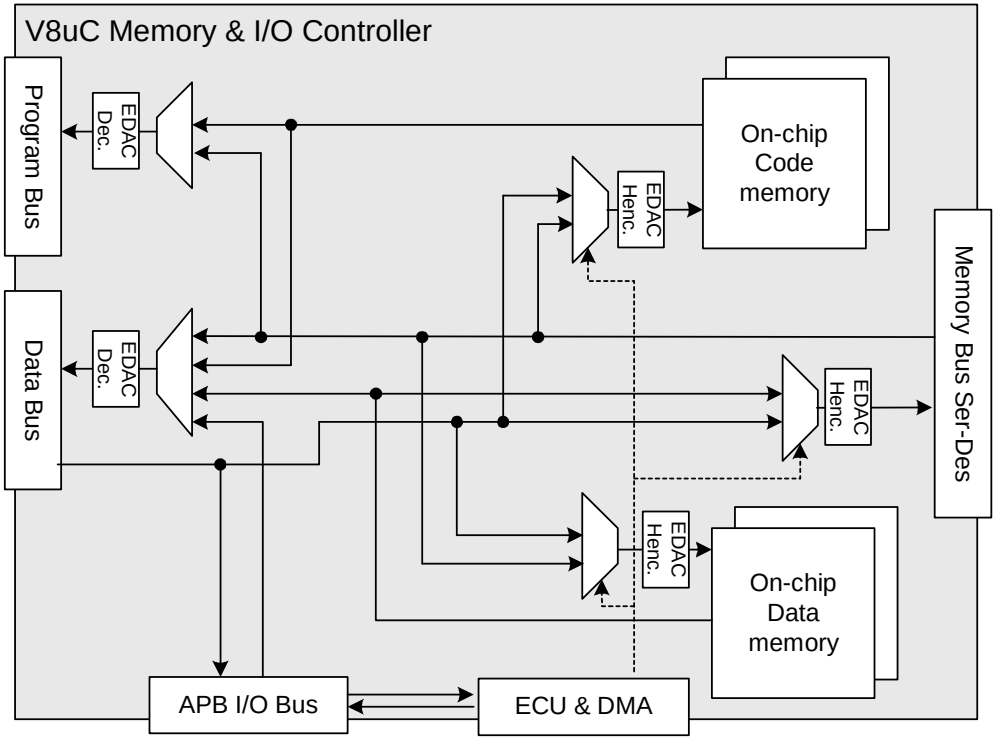
- No Caches
- No AHB Bus
- New Memory Controller with DMA engine
- Programmable number of USARTs, GPIOs and TIMERs
- AuFPU and MIL1553 are optional plug-ins



Architecture : the new memory controller

The memory controller is the only module redesigned from scratch.

- Directly connected on the PipeLine to manage concurrently Data and Program buses
- It resolves conflicts between program and data memory accesses
- New memory controller includes:
  - Addressable local RAM
  - Event Controller & DMA unit
  - APB master for the peripherals bus



External memory interface can work at 8,16 or 32 bit

All on/off –chip memories are EDAC protected

Architecture: From cache to addressable local RAM

Cache tries to keep frequently accessed information close to the processor for low latency accesses

Cache is an expansive mechanism that may be not effective in specific embedded application:

- Data are not always reused, or have limited reuse
- Data are loaded only when requested the first time
- Cache line may be not a good match for data size
- In Real-Time applications, Cache makes the system behavior not easily predictable

In micro-controller the complexity is moved from HW to SW.

Micro-controller is expected to execute few programs heavily optimized by hand

The programmer is in charge to move information close to the processor when it is needed

New Features: Event Controller and DMA unit

- DMA engine capable to manage multiple channels between any combination of on/off-chip memories and peripherals

Three possible triggers for DMA channel activation:

- Program controlled activation (for example for data pre-fetch before elaboration and data store after elaboration)
- Asynchronous request from an external port (for example incoming message or end of transmission)
- Synchronous Schedule (for example: analogue acquisition with a defined sampling rate)

The Event Controller and DMA unit manages in parallel to the processing pipeline all “interrupts” that can be served with a memory transfer operation.

New Features: Peripherals

New functionalities are added to the LEON2 peripherals to address the largest range of devices without need of external logic (FPGA)

Timers

- New option to chain up to 4 x 16 bit timers into a 64 bit resulting timer (RTC)
- PWM output added

USART

- New master/slave SPI function
- New control signals for Map and PacketWire support
- Up to 4 ports

GPIO

- Line size enlarged to 24 bit bitwise programmable
- “S&H” buffer added to interface parallel ADC/DAC devices (AD774/AD667/..)
- Up to 4 lines
- GPIO pins shared with all others peripherals and memory controller

New Features: Interrupts and Sleep controller

IRQ controller changed in **Interrupts and Sleep Controller**

Each peripheral and the processor pipeline itself have an 'Enable' that in HW (ASIC) may be implemented as stretch control for the clock line. Disabled blocks go into low-power mode with no switching activity

- The programmer can disable any peripheral units (not all of them !) and put to sleep also the processor pipeline.
- Any Interrupt request wakes up the processor. Examples of wake up may be interrupt for timer expiration, incoming message on serial or trigger on external wake-up port.
- At reset processor pipeline and all peripherals re-start enabled

Optional Plug-in: AuFPU, MIL1553

- AuFPU is a pipelined floating point unit implementing sub-set of SPARC V8 FP instructions.
- The effective precision is a configurable parameter from the IEEE 754 standard single precision down to custom solutions with reduced mantissa sizes to save resource occupation.

SPARC V8 Instruction	Latency (1)	Sub-module
FADDS	3	FPadder
FSUBS	3	
FCOMPS	3	
FDIVS	8	FPdiv
FSQRT	NA	NA
FMULS	2	Fpmul
FITOS	2	Fpunary
FNEGS	2	
FABS	2	

(1) Latency applies for 20 MHz clock frequency on an Actel ProAsic3 device

- A MIL1553 Remote Terminal (or CAN/CANOpen Slave) will be made available as communication module

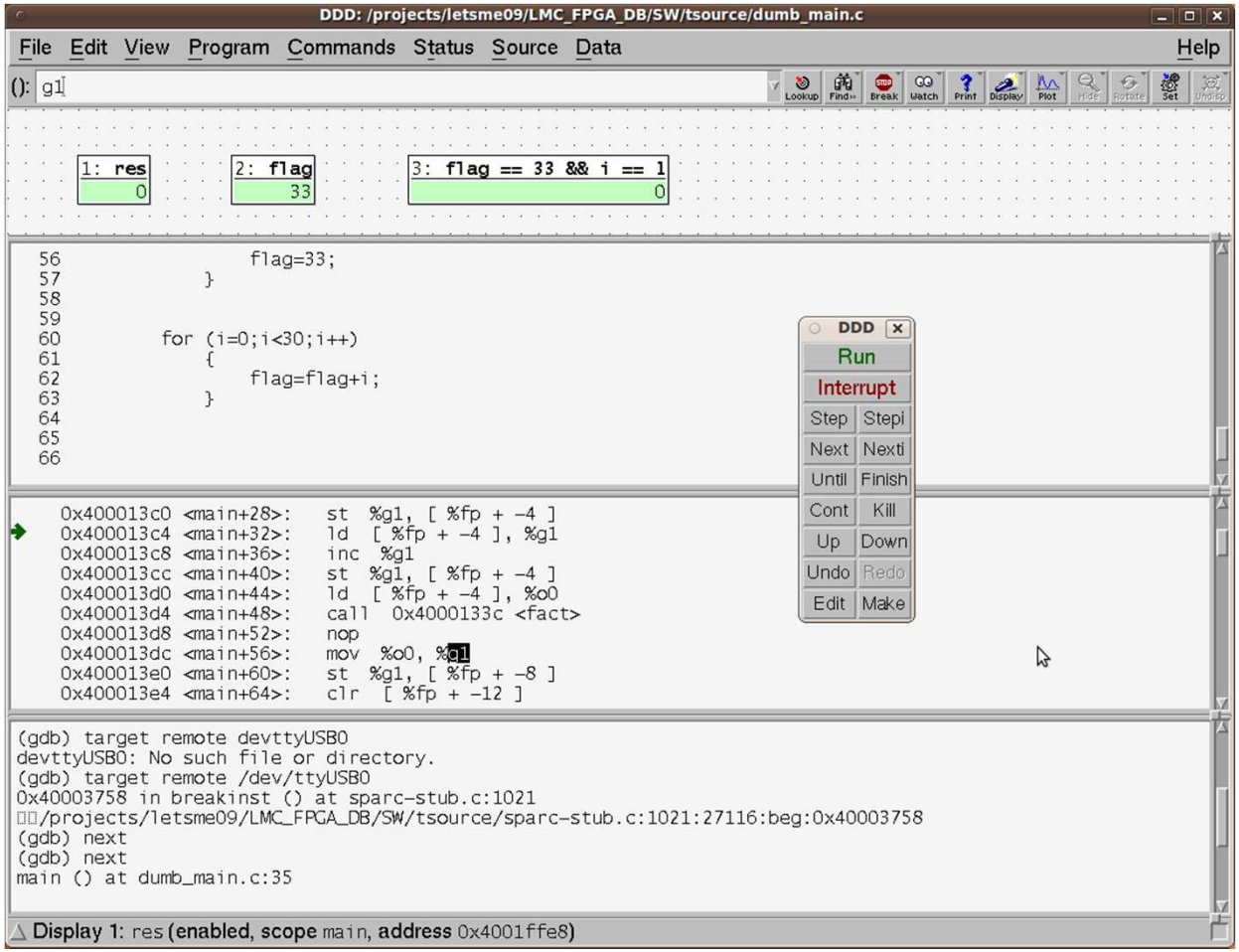
SW tools : compiler and debugger

V8uC is a SparcV8 processor compliant with **sparc-elf-gcc** cross compilers.

The debugging of programs on V8uC can be done using **sparc-elf-gdb** on a standard serial port. A V8uc-GDB stub file and a first V8uC boot code have been developed.

The **DSU** module has been maintained for compatibility with LEON2-FT Tools.

Except for memory controller and cache settings V8uC executes LEON2-FT codes without changes.

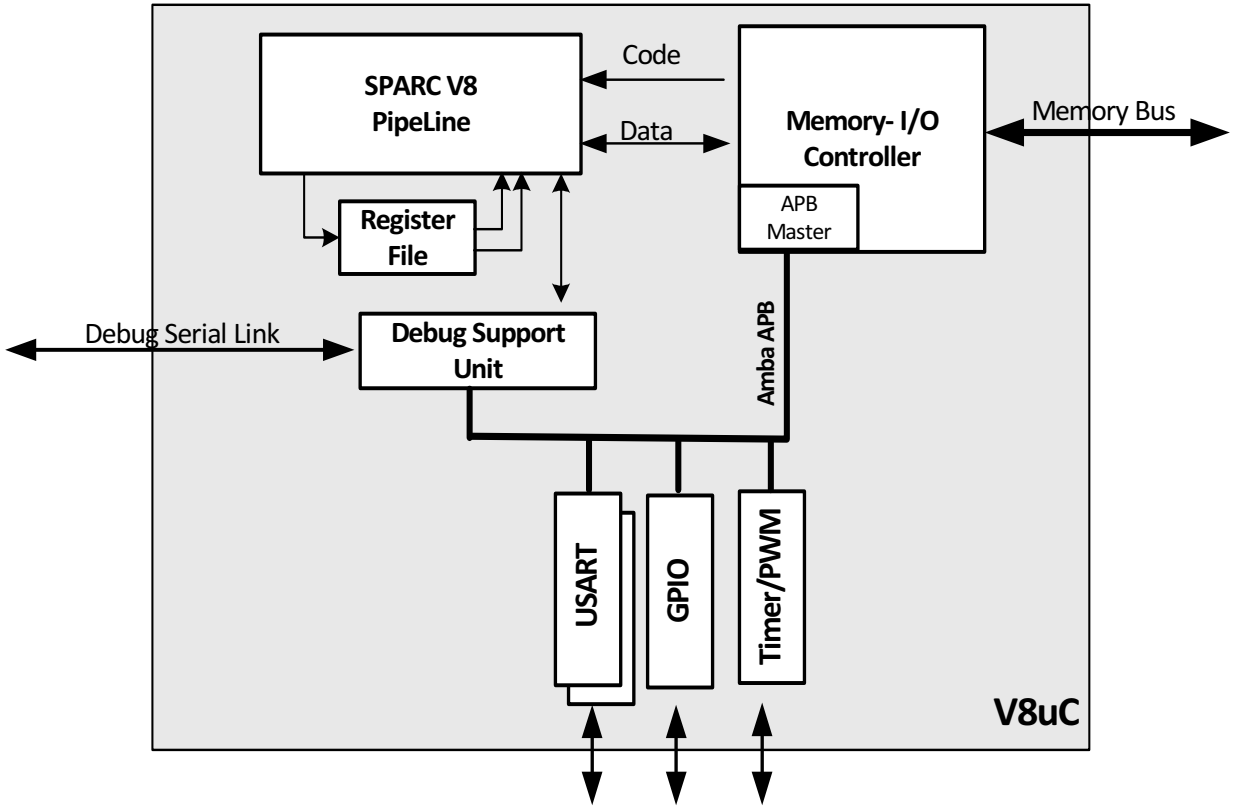


Some Numbers: resource budget (1)

Preliminary synthesis on ACTEL ProASIC3 technology to compare V8uC, LEON2-FT and M8051

Comparison limited to Processor Pipeline + Memory Controller + DSU Vs the equivalent LEON2 modules

TMR not enabled



Some Numbers: resources budget (2)

Unit is the ACTEL ProASIC3 VersaTile cell (the A3PE3000 devices claims 75264 VersaTiles corresponding to 3000000 system gates)

LEON2 is around 40% greater than V8uC that is around 100% greater than M8051

Module	V8uc	LEON2	M8051
IU (with Mul M16x16)	10314	9817	
DSU_Box (V8uc)	1526		
DSU		930	
DCOM		1170	
MemCtrl (V8uc)	935		
CACHE		5278	
MCTRL		1710	
AHB Arb		315	
AHB Master		579	
AHB Slave		122	
Total	12775	19921	6300

Some Numbers: first benchmark

The Dhrystone benchmark for integer computation and strings manipulation has been executed on a V8uC, LEON2-FT and M8051

V8uC: 8 Register windows; 64Kbyte program + 64Kbyte data memories on chip.

LEON2: Instruction Cache = 4 x 8Kbyte x 8byte ; Data Cache = 2 x 8Kbyte x 4byte

	V8uC	*LEON2*	*M8051*
Clock Frequency	32 MHz	32 MHz	16 MHz
Dhrystone/s	49230	44076	595
MIPS/Mhz	0.876	0.780	0.021

V8uC is 10% faster than LEON (Local Memory Vs Caches advantage) and 40 times faster than M8051 (8 bit too few to manage Dhrystone bench !?)

Conclusions

- First tests confirm that V8uC can be an effective substitute for the phasing out M8051
- Reuse of LEON2-FT already debugged modules allowed a fast prototyping: first sub-system is already running

Next step is PDR in 2 weeks

- First architectural design is completed according to inputs received from ESA regarding memories and peripherals management.
- The Soft nature of the IP Core still allows receiving suggestions for enhancements
- Please send questions/comments/suggestions to:
  - Me : w.errico@sitaelspace.com
  - Technical officer: claudio.monteleone@esa.int
- Full VHDL core is planned in 6 months