Control Loop Processor

Towards European Programmable Solution for Dedicated Hard Real Time Applications

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ADCSS 2010 - MESA

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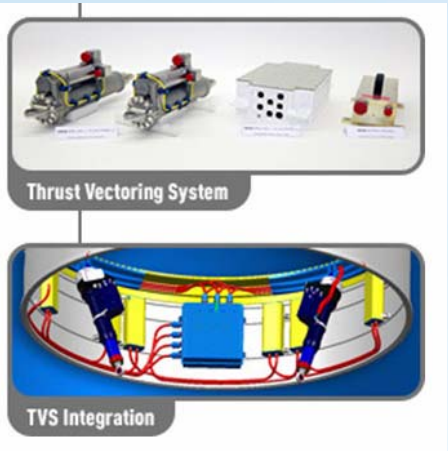
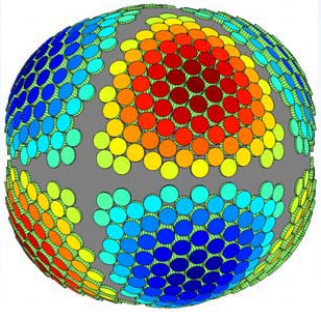
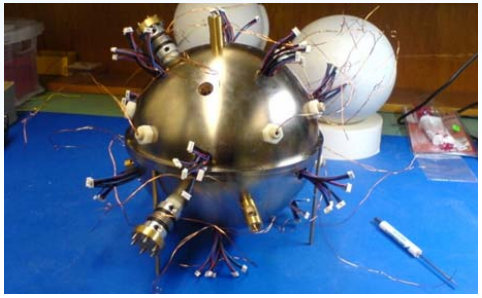
TECHNICAL PERIMETER (1/2)

- **Increasing demand in:**
  - More complex control strategies
    - VEGA launcher: TVC Electrical Subsystems
    - IXV: Flap Control Systems
    - Ariane 5 MidLife: TVAS, Fault Tolerant drive electrical actuation
  - New actuators/mechanisms topologies, harder to control
    - Reaction Sphere for attitude control: equivalent to 3D electrical motor







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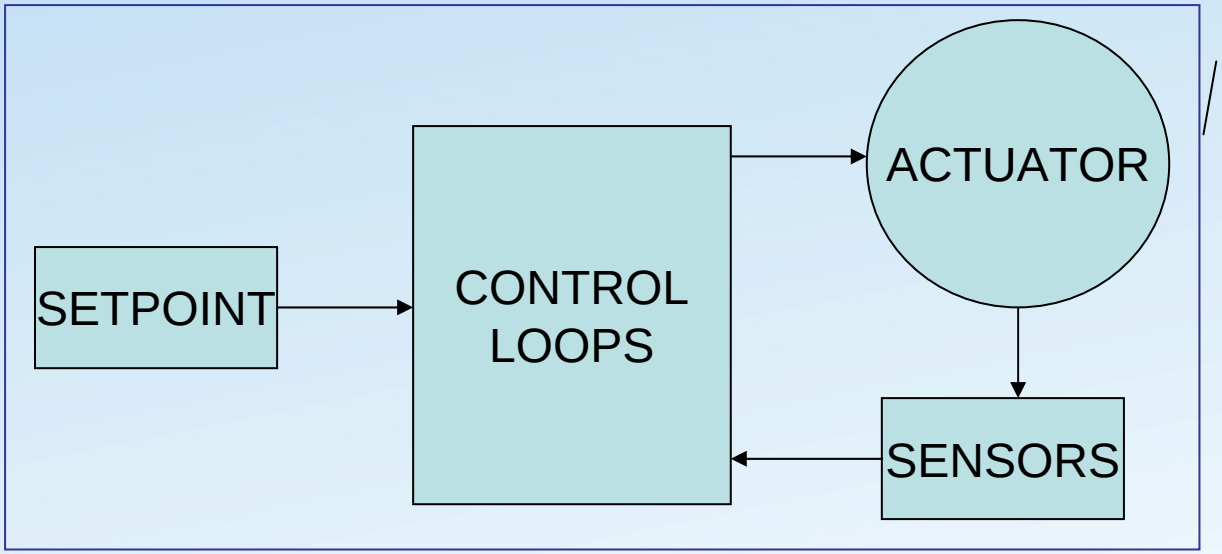
TECHNICAL PERIMETER (2/2)



Example:

BW Loop #1 (outer loop) @ 10Hz

BW Loop #2 (middle loop) @ 100Hz

BW Loop #3 (inner loop) @ 1KHz

If sampling rate = 10xBW, execution @ 10 KHz

- **Key characteristics**
  - One to several nested control loops with tight processing constraints
    - Most complex loop is often the smallest (matrix, mathematical functions, high order filters…)
  - Poor implementation options
    - Analog solution unfeasible
    - Digital alternative has a limited space-grade processors range
    - Classical SW approach leads to real time issues

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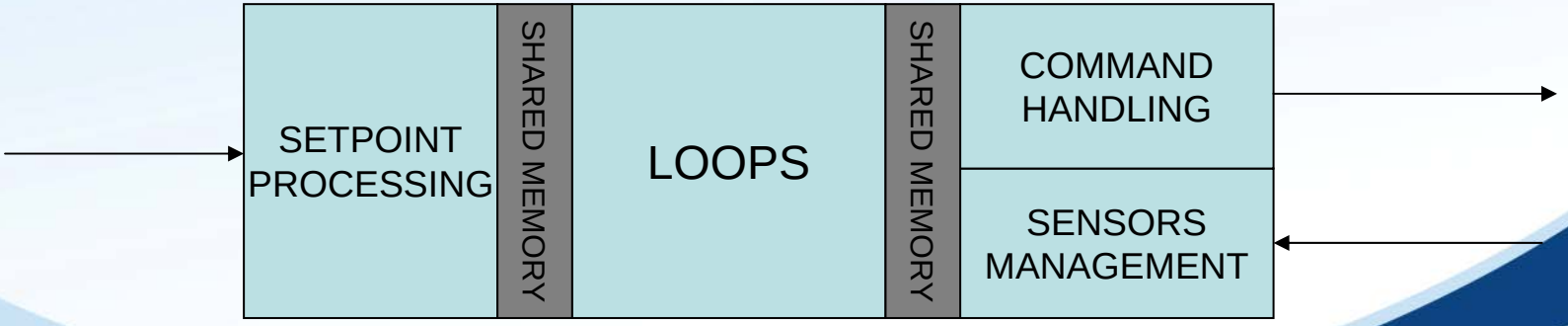
TECHNICAL BASELINE (1/2)

- **Dedicated SW/HW architecture**
  - Loops execution made in <u>software</u> via CLP *core*
    - Dedicated time slicing (cfr next slide)
    - Uninterruptible execution
  - Interface with real world (sensors management, setpoint processing,…) made in <u>hardware</u> units via CLP *peripherals*
    - Stand-alone capability
    - Configured during initialization via software
  - "Core ⇔Peripherals" communication via dual port <u>shared-memory</u>
    - Core has the highest priority
    - Avoids interruption mechanism penalizing loop execution



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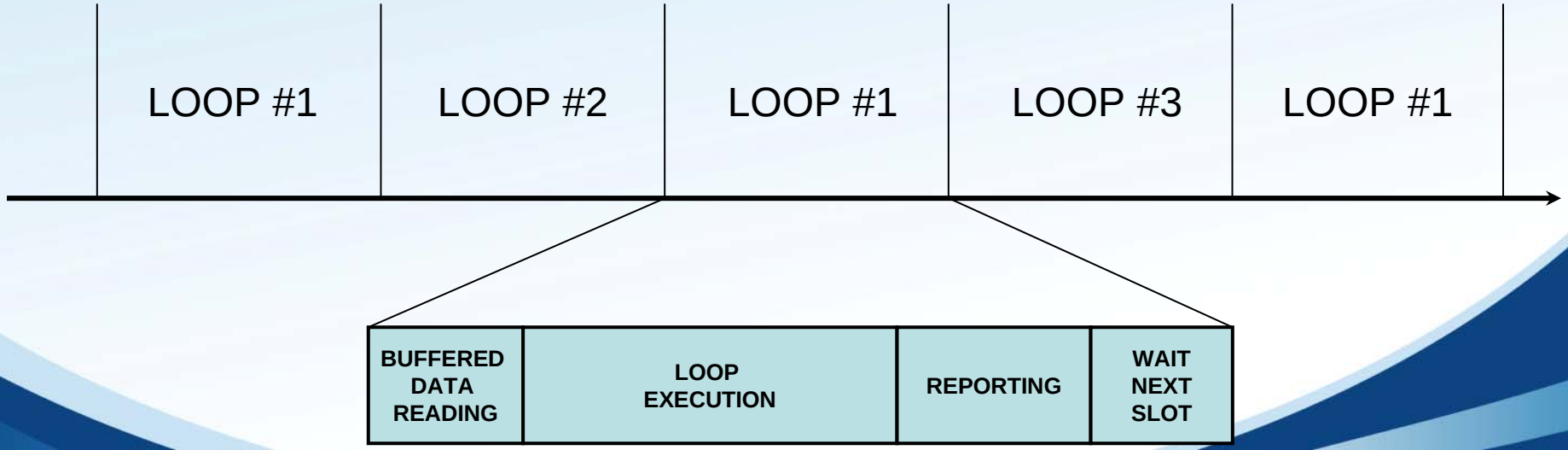
TECHNICAL BASELINE (2/2)

- CLP software architecture
  - One global loop made of fixed length time slots
    - Arranged to have each loop working at right frequency
  - Sequential execution, only forward branching allowed
  - Start of timing slot triggers loop execution and peripherals (ADC start of conversion and so on…)
  - Takes advantage of the controller features



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CONTROLLER CHARACTERITICS (1/3)

- Deterministic execution
  - Cache-free
  - RISC machine
  - Uninterruptible architecture

- Computation power, compatible with targeted high dynamic data
  - Dual Floating-Point units
  - Data format: IEEE-754 single-precision format
  - On-chip 10-kbit memory data, fast access, double data fetch, organised in banks (small data size)

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CONTROLLER CHARACTERITICS (2/3)

- Safe behavior
  - Exception-free arithmetic (as per ADSP 21020)
  - Saturating arithmetic
  - Floating-point format avoids typical fixed-point issues (rescaling, overflow and so on)
- Efficient time slot management
  - Real-time counter
  - Autonomous functions to support application interfaces (PWM, sensors excitation, ADC interface,…)
- Non-intrusive real-time reporting

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CONTROLLER CHARACTERITICS (3/3)

- Hardened for space applications
  - On-chip EDAC for memories
  - Hardened technology for other

- Targeted performance
  - 50 MIPS
  - 100 MFLOPS
  - 300-500 mW (@fmax)

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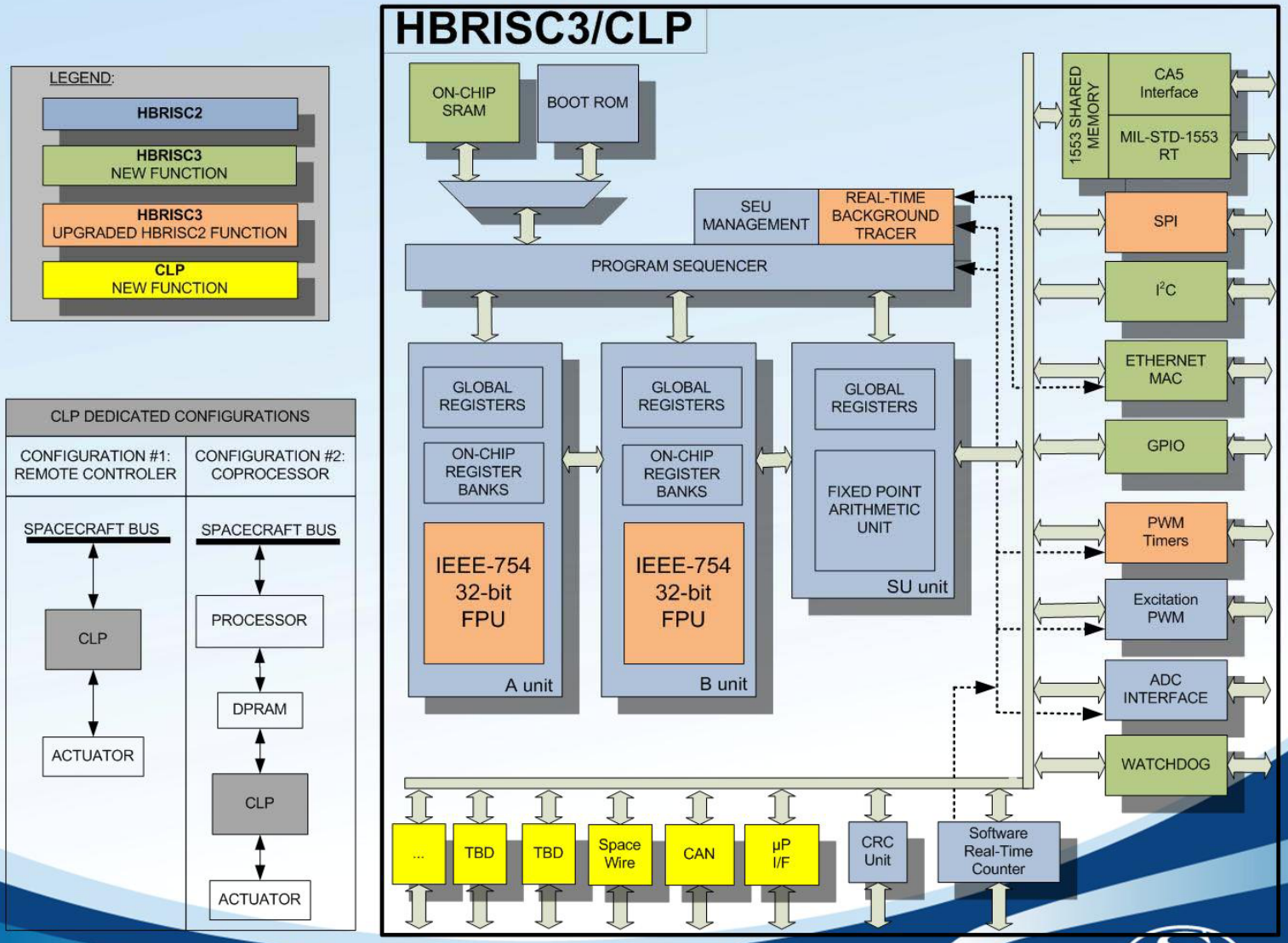
CONTROLLER FUNCTIONAL DIAGRAM



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SOFTWARE TOOLS (1/2)

- Control loops design is Matlab/Simulink-based
  - Standard development tool for most system and control engineers
  - Synthesizable model (i.e. used for code generation) can be simulated and uses a dedicated library

- Then uses automated code generator
  - Simple conversion of Simulink model into macro calls
  - Static register allocation, exclusively using on-chip data memory
  - Fully deterministic and sequential execution
  - OS-free and highly efficient code
  - Equivalence between one Simulink variable and associated CLP register

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SOFTWARE TOOLS (2/2)

- Other key considerations
  - SW tools are easy to develop and maintain
    - Code generator is more a translator than a compiler/optimizer
    - Assembler is simple thanks to CLP straightforward features
  - Generated SW is easy to validate

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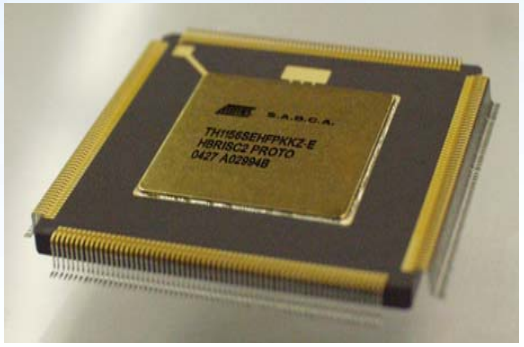
CONCLUSION

- Heritage of proprietary design (HBRISC2) – cfr MPSA ADCSS 2009
- Fully predictable, uninterruptible and vectorial architecture to deal with targeted applications
  - Control loops running @ 1 kHz or higher
  - Complex control algorithms
- Accessibility to general users
- Programmable, tailoring made with simple and OS-free SW
- ITAR free



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