ATMEL microprocessor family

ATMEL works on processors for space for more than 15 years

- Existing processors for space
  - 80C32E
  - TSC21020 DSP
  - TSC695F and TSC695FL Sparc V7
  - AT7913E LEON2-FT Sparc V8
  - AT697E/F LEON2-FT Sparc V8
  - Reconfigurable Processor

- Microprocessors products family roadmap
  - B_ LEON2-FT Sparc V8
  - S_ LEON2-FT Sparc V8
  - DSP_ LEON2-FT Sparc V8
  - MultiCore Sparc
80C32E 8-Bit Architecture

• 80C32: 8-bit ROMless microcontroller rad.tolerant
  • Side Brazed 40-pin, MQFPJ 44-pin
  • Total Ionizing dose: 30 krads (Si) according to MIL STD 883
  • No Single Event Latch up below 80 MeV/mg/cm²
  • QML Q and V with SMD 5962-00518
• 0.8μm RT CMOS technology
• End of life announcement 2010/11
• No new design based on this product
TSC21020F DSP

- Standard 32/40-bit Floating Point from Analog Devices
  - Radiation tolerant version of ADSP-21020
  - Superscalar IEEE Floating Point Processor
  - 20 MHz max; 5V ± 0.5V
  - 40 MFlops sustained performance, 60 MFlops peak
  - Space qualified MQFPF-256 for flight models
  - Total Ionizing dose : 100 Krad
  - No Single Event Latch up below 80 MeV/mg/cm2
- 0.6µm RTP CMOS technology
- End of life announcement 2011/12
- No new design based on this product
## TSC695F/FL SPARC 32bit Space Processor

**Flight heritage more than 1600 flight model**

<table>
<thead>
<tr>
<th>TSC695F</th>
<th>TSC695FL Low Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>25 MHz, 20Mips, 5Mflops @ 5V+/-0.5V</td>
<td>15 MHz, 12Mips, 3Mflops @ 3.3V+/-0.15V</td>
</tr>
<tr>
<td>SEU Rate Better than 1.6E-8E/d/d on GEO</td>
<td>SEU Rate Better than 1.2E-7E/d/d on GEO</td>
</tr>
<tr>
<td>SEU Rate Better than 8E-10E/d/d on LEO</td>
<td>SEU Rate Better than 4E-5E/d/d on LEO</td>
</tr>
<tr>
<td>41 mA power down current @ 25 MHz</td>
<td>10 mA power down current @ 15 MHz</td>
</tr>
<tr>
<td>230 mA operating current @ 25 MHz</td>
<td>100 mA operating current @ 15 MHz</td>
</tr>
<tr>
<td>ESCC &amp; QML V (5962-005401)</td>
<td>ESCC &amp; QML V (5962-03246)</td>
</tr>
</tbody>
</table>

- 0.5µm RTP CMOS Technology
- Latch up immune
- Total Ionizing dose : 300Krads (RHA=R)
- **End of life announcement 2013/14**
AT7913E – LEON2FT - SpaceWire RTC 1/2

Design performed by Saab Space under ESA contract, and manufactured by ATMEL

- Sparc V8 Leon2 FT with Floating Point Unit
- AT7913E RTC (Remote Terminal Controller)
  - Two CAN interface
  - FIFO interface (parity check)
  - ADC/DAC interface
  - 2 UART interfaces
  - 2 bidirectional SPW link 200Mbit/s on chip LVDS
  - 64kB x 32 on chip memory with EDAC
  - ...
- SW can be uploaded via SpW link (RMAP compatible)
- Direct Memory and IO Access via SpW RMAP
- CMOS Technology: ATC18RHA (0,18 µm)
- Processor performance (@ 50MHz)
  - Dhrystone 2.1 benchmark = 34,4 MIPS
  - GNC benchmark = 2,4 MFLOPS
- 1.8V core, 3.3V I/O
- Power consumption: ~0.7W@50MHz
- LGA 349 and MQFPF 352 to be introduce
- SMD
  - 5962-10A0301QYC, 5962-10A0301VYC for LGA
AT7913E – LEON2FT - SpaceWire RTC 2/2

Design performed by Saab Space under ESA contract, and manufactured by ATMEL

24 GP I/Os
8 Pulse Generation lines

8/16 bit ADC/DAC
Parity bits

4 Kbyte I&D Cache
16 x 16 multiplier
8 register windows
Radix 2 divider
5 Stage I-pipeline

EDAC functionality

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AT697 E/F Sparc V8 32-bit Architecture 1/2

• SPARC V8 LEON2-FT with Integer and Floating Point Unit
• ATC18RHA CMOS 0.18 micron; 1.8 V core; 3.3V I/Os
  • Fault tolerance by design
  • On chip Amba Bus
  • Embedded Instruction and Data caches
    • 16Kbytes multi-sets Data cache
    • 32Kbytes multi-sets Instruction Cache
• Memories Interface for PROM, SRAM and SDRAM
• PCI 2.2 interface (33 MHz)
• Two Timers, two 8-bit Uarts and interrupt Controller
• Debug Support Unit
  • Trace buffer 512 lines of 16 bytes

• Available package
  • LGA 349
  • MQFPF 256

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AT697 E/F Sparc V8 32-bit Architecture  2/2

AT697F development tasks

• **Electrical characterisation and validation**
  • Full bias voltages and military temperature ranges

• **Application Tests**
  • Update of the evaluation board

• **ESCC evaluation**
  • ESCC screening on going

• **Space Qualification QML Q, QML V**
  • AT697F-KG-E MQFPF 256 Engineering Samples
  • 5962-0722402QYC MQFPF 256 QMLQ
  • 5962-0722402VYC MQFPF 256 QMLV
  • 5962R0722402VYC MQFPF 256 QMLV-RHA

• **Radiation characterisation**
  • Total dose : tested up to 300Krad(si) successfully
  • SEE heavy ions and protons first run done @ UCL
    • Analysis on going
    • Next Run @ UCL end November 2010
Reconfigurable Processor  1/2

- Processor
  - AT697F SPARC V8 LEON2-FT
- Reconfigurable unit
  - ATF280F SRAM based FPGA
- Total dose up to 300Krad(si)
- Available package
  - MQPFP 352
- Functionalities
  - AT697F predominance, to allow speed performance
  - LEON can boot using ATF280
  - PCI internal only
  - PCI Bus can be used to communicate with the FPGA using DMA
  - Separate reset
  - Separate Power supply: each component can be powered separately
- First application based on CNES space application

The development of the Reconfigurable Processor is funded by CNES the French space agency
Reconfigurable Processor  2/2

• **ATF280F FPGA**
  - 151 I/O including Clocks
  - 2 LVDS Transceivers Space Wire compliant

• **AT697F Processor**
  - SDRAM control
  - Control (reset, Watchdog, DSU, Clock, skew)
  - 8 PIO [15:8] bits (including UART)

• **SHARED**
  - Bus (32 data + 8 CB + 28 address)
  - Memory control
  - 8 PIO [7:0] bits
  - JTAG

The development of the Reconfigurable Processor is funded by CNES the French space agency
Some products on the market

- Need of a small and a mid range processor for equipments (Sensors, CCD, Star trackers ...)

- Missing Space Interface in AT697 (SpaceWire, 1553, CAN ...)

- Need Computing power At low power consumption

- To be completed any idea?
Microprocessors products family roadmap

Legend
- SPARC V7
- SPARC V8
- MCP Processor
- Next G µP
- Embedded FPGA
- MultiCore Sparc + DSP
- DSP_Leon2FT
- B_Leon2FT
- 150MIPS µP
- S_Leon2FT
- 20MIPS µC

AT697E/F
AT697F+ATF2
AT697F+ATFS4
AT7913 (SpW)
TSC695
80C32

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ATMEL strengths

• Background ERC32, AT697E and AT697F (SparcV7, V8)
• 90nm technology retargeting
• Power consumption vs Speed Performance
  • Use of both Standard and Low leakage
• Software compatibility with Leon2FT (AT697E/F)
• Development tools and on chip debug facilities.
• Already Hardened by Design
• Flight heritage
• QML-V & ESCC QML procurements
**B_ LEON2-FT Sparc V8 1/2**

- **SPARC V8 High Performance Low-power 32-bit Architecture**
- **90nm Target technology**
  - Voltages: 3.3V +/- 0.30V for I/O and 1.0V +/- 0.15V for Core
- **Frequency from 120MHz up to 200MHz**
  - Leon2FT core with Limited improvement to be added
  - Same interfaces as AT697 (Timers, Uarts, I2C, ...)
  - Same package LGA349 and QFP256
    - According to the Ips pins requirement
- **Add new features**
  - Memory Management Unit: MMU(?)
  - Increase Cache size
  - Internal SRAM (HRAM Hardened) and ROM (HROM) with Default Boot
  - SpaceWire, PCI interface and AHB External Bus
  - CAN interface, 1553 interface and Ethernet(?)
  - Boot capability to external serial Prom
  - Interface to external ADC/DAC
- **Fault Tolerance by Design**
B_ LEON2-FT Sparc V8  2/2
LEON2FT SPARC V8 High Performance Low-power 32-bit Architecture

- 90nm Target technology
  - Voltages: 3.3V +/- 0.30V for I/O and 1.0V +/- 0.15V for Core

- Low processing power (few 10Mips)
  - Low power single chip
  - Low end space application (Sensors,...)
  - No cache memories
  - 4 Register Windows
  - No internal Sram
  - 8 bits external memories interface
  - Limited addressing range (few Mbytes)
  - No FPU

- Add new features
  - SpaceWire (LVDS and Digital outputs)
  - ROM (HROM) with Default Boot (?)
  - Boot capability to external serial Prom (?)
  - Interface to external ADC/DAC (?)

- QFP 100 (ideally QFP64)
- Fault Tolerance by Design
DSP_ LEON2-FT Sparc V8

- C programmable VLIW DSP
- Floating point 32 / 40 bit
- Up to 10 floating point operations per cycle
  - 1.5 GFLOPS @ 150MHz in 90nm (target for DSP_Leon2FT)
- 2 address generation units, 4 memory accesses per cycle
- 6 port memory system allowing concurrent computation and data move
- Float – vector – complex native data type support
- Program Memory Management Unit (PMU). PM cache
- DMA engine supporting stridden memory accesses
- AMBA AHB master and slave bus interface

- C callable optimized functions, written in C
  - Functions can be modified and adapted if needed
- More than 200 functions available, covering all the basics of DSP
- All the functions works on array
DSP_ LEON2-FT Sparc V8

mAgic DSP Architecture
Product development Plan

Step 1
B_Leon2FT Sparc V8
On-chip Amba Bus
U to 150Mips
Numerous Features and interfaces

Step 2
Leon2FT Sparc V8 + DSP
1.5Gflops @150MHz

Step 3
S_Leon2FT Sparc V8
Low power few Mips
SpaceWire Link

Step 4
Dualcore Sparc V9
Multicore Sparc V9 + DSP
Thank You