Processor and Peripheral IP Cores for Microcontrollers in Embedded Space Applications

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Presentation outline

- Microcontroller requirements
- Requirements vs. available technology
- What can be provided today
  - Why a SPARC based microcontroller
  - Available peripherals
  - Proposed architecture
  - Single-event hardening
  - Existing architectures
- Availability
- Conclusions/Summary
Microcontroller requirements

• Requirements
  – Single chip
  – Single processor core
  – Medium speed interfaces such as CAN, PWM
  – On-chip memories (RAM/EEPROM)
  – Analogue function such as ADC/DAC
  – Power management functions / low power consumption
  – Low price
  – Low pin count, package easy to assemble
Requirements vs. available technology (1)

• No problem to specify an architecture that meets all requirements. More interesting is perhaps:
  – What can actually be manufactured?
  – What technology is available in Europe?

• Processor and peripheral IP cores
  – Several processor alternatives exist
  – Peripheral IP available from several sources
  – IP core availability is not a major issue

• On-chip RAM
  – Consumes significant area
    • Does not fit well with simple package requirement
Requirements vs. available technology (2)

• Target process must support digital system combined with on-chip rad-hard EEPROM.
• Should this not be available an alternative is external rad-hard EEPROM
  – Existing devices have parallel interfaces
  – Does not fit well with low pint count package
  – Limited size ~128 KiB (may be enough for \( \mu \)C)
  – Workaround: Larger package

• Rad-hard process must support digital system combined with on-chip ADC/DAC and building blocks need to be available.
  – Appears not to be currently available in Europe
  – Alternative: Use Ramon Chips 130 nm which has ADC/DAC
Requirements vs. available technology (3)

- Requirement: Low pin count
  - Requires on-chip RAM and EEPROM
  - But on-chip RAM requires large area
  - Off-chip EEPROM requires ~30 pins
- Requirement: Easy assembly
  - Requires simple package
  - See above
- Reducing area by moving RAM off-chip → higher pin count
- Low pin count and/or easy assembly is not easily attainable with currently available technologies

- Requirement: Low cost - Producing a µC is not necessarily cheaper compared to building a more advanced SoC
• Competence for developing the building blocks required for ADC/DAC and EEPROM combined with digital system targeted for space use is available in Europe
  – All building blocks not available on the same process

• A microcontroller can still be implemented, not fulfilling all requirements:
  – Processor/peripheral IP: Available
  – On-chip RAM: Available, results in large area
  – On-chip EEPROM, ADC/DAC: Not available on same process
  – Low pin count, easy assembly: Hard to achieve
Why a SPARC based microcontroller?

• Open standard → No licensing issues
• Certified instruction set
• Code compatibility: ERC32 → LEON2FT → LEON3FT (→ LEON4)
• Potential drawbacks
  – No 16-bit instruction set
    • Alternative: Code compression
      – No major obstacles on hardware side
      – Work on software side is major
        » Requires external funding
  – Objections to 32-bit - “not a μC”
    • Many applications work with 32-bit data
    • SW developers used to OS support
      – More powerful μC may be necessary
LEON3FT SPARC V8 processor core

- Fault-tolerant and SEU-proof
- Already used in a number of space applications
- SPARC V8 instruction set with V8e extensions
- 7-stage pipeline
- Hardware multiply, divide and MAC units
- IEEE-754 FPU options available
- Configurable caches: 1-4 ways, 1-256 KiB/way
- On-chip debug support with instruction and data trace buffer
- Power-down mode and clock gating
- Robust and synchronous single-edge clock design
- Extensively configurable
- Large range of software tools: compilers, kernels, simulators and debug monitors
- High performance: 1.4 DMIPS/MHz, 1.8 CoreMark/MHz (gcc-4.1.2)
Selection of peripheral IP cores in GRLIB

• Memory controllers
  – SRAM/PROM/IO controller with EDAC (FTMCTRL, FTSRCTRL)
  – SPI memory controller (SPIMCTRL, requires external FT devices)

• Communication interfaces:
  – SPI master/slave controller with 3-wire mode (SPICTRL)
  – I2C master and slave controllers (I2CMST / I2CSLV)
  – PWM controller (GRPWM)
  – General Purpose I/O port (GRGPIO)
  – CAN controllers (OC_CAN / GRCAN)
  – USB device and host controllers (GRUSBDC / GRUSBHC)
  – SpaceWire controllers (GRSPW1 / GRSPW2)
  – MIL-STD-1553B (GR1553B)
  – ADC/DAC controller (GRADCDAC)
  – Pulse controller (GRPULSE)

• Other:
  – Timer units (GPTIMER, GRTIMER)
  – Time distribution cores
Proposed architecture

- Processor core: LEON3FT, no MMU, 4+4 KiB I/D cache, GRFPU-light
- RAM: On-chip 256 or 512 KiB
- EEPROM: Off-chip, parallel (~27 pins)
- Peripherals: Timer unit, interrupt controller, UART (4 pins), 2x SPI (8 pins), 2x I²C (4 pins), 1553 BRM (A/B) (12 pins), CAN 2.0b with redundant port (4 pins), SpaceWire codec with RMAP target (4 pins), GPIO (16 pins)
- Pin count: 27 memory, 52 I/O, 2 clocks, total: 81 + power
- Debug connection: UART
- Pin count: ~50 + power (requires pin sharing)
- Proposed package: CQFP68
- Example implementation Ramon Chips 130 nm:
  - Area: 5.5 mm² core area including routing
    - + 10 mm² for 256 KiB on-chip RAM
    - + 20 mm² for 512 KiB on-chip RAM
  - Power: 1mW / MHz with clock gating
  - Frequency: 0 – 200 MHz
Fault tolerance in proposed system is aimed at detecting and correcting SEU errors in on-chip RAM.

- L1 cache and register file in LEON3FT is protected using parity and BCH.
- RAM blocks in on-chip IP cores can be protected using BCH or TMR, smaller buffers can be synthesized as flip-flops.
- Flip-flops should be protected using SEU-hardened library cells or TMR.
- Technique proven (used for existing LEON2FT and LEON3FT devices).
Architecture 2

- Processor core: LEON2-FT with Meiko FPU
- RAM: On-chip 64 KiB SRAM and external SRAM
- EEPROM: Off-chip, parallel
- Peripherals: UARTs, FIFO I/F with DMA, ADC/DAC interface, 24 GPIO with pulses, CAN, 2x SpaceWire links
- Implementation on Atmel ATC18RT:
  - Frequency: 50 MHz
  - Package: MCGA 349
- Currently available as AT7913 from Atmel
Architecture 3 (1)

- Processor core: 2x LEON3FT with MMU and GRFPU
- RAM: 192 KiB on-chip, external SRAM/SDRAM
- EEPROM: Off-chip, parallel.
- Peripherals: 6x SpaceWire links, redundant 1553 BRM, CCSDS Telemetry Generator, CCSDS TC Decoder Front-end, 2x CAN 2.0B, 6x UARTs, 10/100 Mbit Ethernet MAC, I²C master, SPI master, 64 General Purpose I/O
- Debug link: JTAG
- I/O matrix offering five configurations, power save via clock gating
Architecture 3 (2)

- Implementation on Ramon Chips/Tower 180 nm, CQFP-240 package
- Performance
  - 100 MIPS/100 MFLOPS peak @ 100 MHz (per processor core)
  - 140 DMIPS/core in on-chip SRAM
  - 55 MFLOPS/core Whetstone
- Soon available as GR712RC component from Aeroflex Gaisler
Availability

- All IP cores are available as part of a highly portable IP library
- Library has already been used to target DARE 0.18, Atmel 0.18, Ramon chips 180 nm, and several other ASIC targets.
- All IP cores can be licensed for use in projects
- Design services are also available
- Component availability: Actel RTAX/FT ProASIC 3
  - Perhaps not low power enough
  - Typically not a small chip with few pins
- Architecture 2 is already available as an ASIC
  - AT7913 (SPW-RTC) from Atmel
- Architecture 3 soon to be available as an ASIC
  - GR712RC from Aeroflex Gaisler
• Microcontroller requirements need to be formulated
  – What does the industry think about 8- vs. 32-bit
  – What interfaces are most important?
• Based on the requirements given in this presentation: A “real” microcontroller for space use requires ASIC technology which may not be available in Europe today
• To build microcontroller with on-chip EEPROM and ADC/DAC, focus should be on developing ASIC technologies
• Aeroflex Gaisler can provide microcontroller systems for space use on Actel RTAX/FT ProASIC 3.
• IP cores for microcontroller development are available, both for licensing as standalone cores and as part of a highly portable IP library.
• There are components available, or soon available, for instance AT7913 from Atmel and GR712RC from AG
Thank you for listening