Cambridge Consultants

Using XAP Processors in Space Applications

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XAP®

Cambridge Consultants – a multi-disciplinary engineering and design consultancy.

XAP®

- Established out of Cambridge University in 1960.
- 300 staff in Cambridge UK, 40 in Boston MA
- We design and develop innovative products, processes and systems using multi-skilled teams supported with in-house services, labs and prototyping capabilities
- Our work is typically on strategic projects that require deep technical and market knowledge
- We serve a worldwide client base ranging from funded start-ups to blue chips working in:
  - Semiconductors, processors
  - Aerospace, transport, defence
  - Energy, metering, security
  - Healthcare, industrial, manufacturing, retail
  - Communications, wireless, consumer

What are the problems with using a processor in space?

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- Low power
- Long lifetimes
- Low area to permit redundancy
- High reliability
- Radiation environment
  - Need protection from Single Event Upset (SEU) and other damage
  - Particularly in the memory, as this is often the larger area
- Ability to safely perform (large) software upgrades and (small) patches while in orbit
- Large audience with a big range of technical requirements
  - Both high level and low level software should be supported
- Use cases in FPGA, custom ASIC or standard microcontroller

XAP®

XAPs are a family of 16 bit processors optimised for low power, small silicon area and easy verification

XAP®

- XAPs have been sold since 1995 - there are now over 1 billion XAPs in silicon
- There is probably a XAP in your pocket already!
  - XAP is used in most Bluetooth chips for mobile phones and headsets
  - XAP and xIDE (Bluelab) are recognised success factors for CSR's business
- Ember Communications has XAP in the EM250 and EM260 ZigBee chips
- 3M uses XAP in its range of touch screen controllers
- Other licensees used XAP in their ASICs or ASSPs
- Including high-reliability applications such as in-body medical products

Green Peak

3M

Chipcon

SiGe Semiconductor

GN ReSound

Combitech Systems

ember

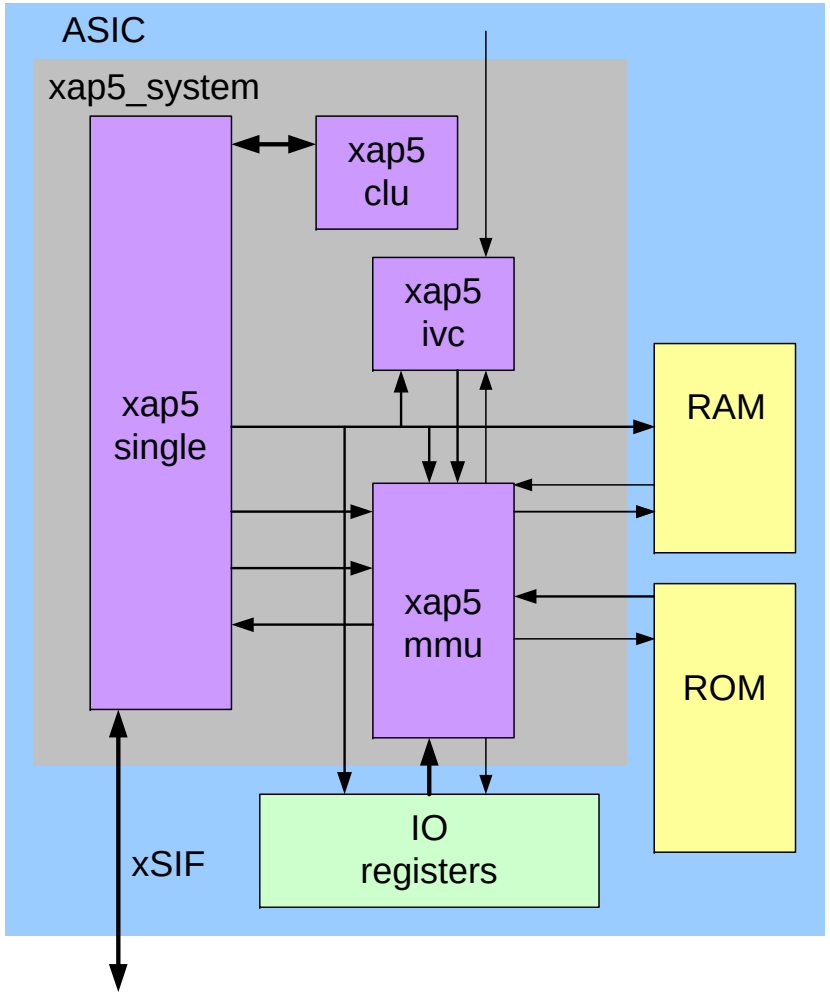
cyan

csr

Latest XAP 16-bit processors – XAP4 and XAP5

XAP®

- XAP4
  - 12k gates
  - Up to 64kB memory
- XAP5
  - 18k gates
  - Up to 16MB memory
- Modern RISC Von Neumann processors
- Non-invasive debug:
  - xSIF (external serial)
  - iSIF (internal parallel)
- GNU compile chain (GCC and Binutils)
  - C, Ada, (C++ soon).
- User and privileged modes enable code separation
- Nested Interrupts and Exceptions (error-handling)
- 2 Stack Pointers. Typical usage :
  - SP0 for a single persistent system stack
  - SP1 for multiple task stacks



XAP5 hardware

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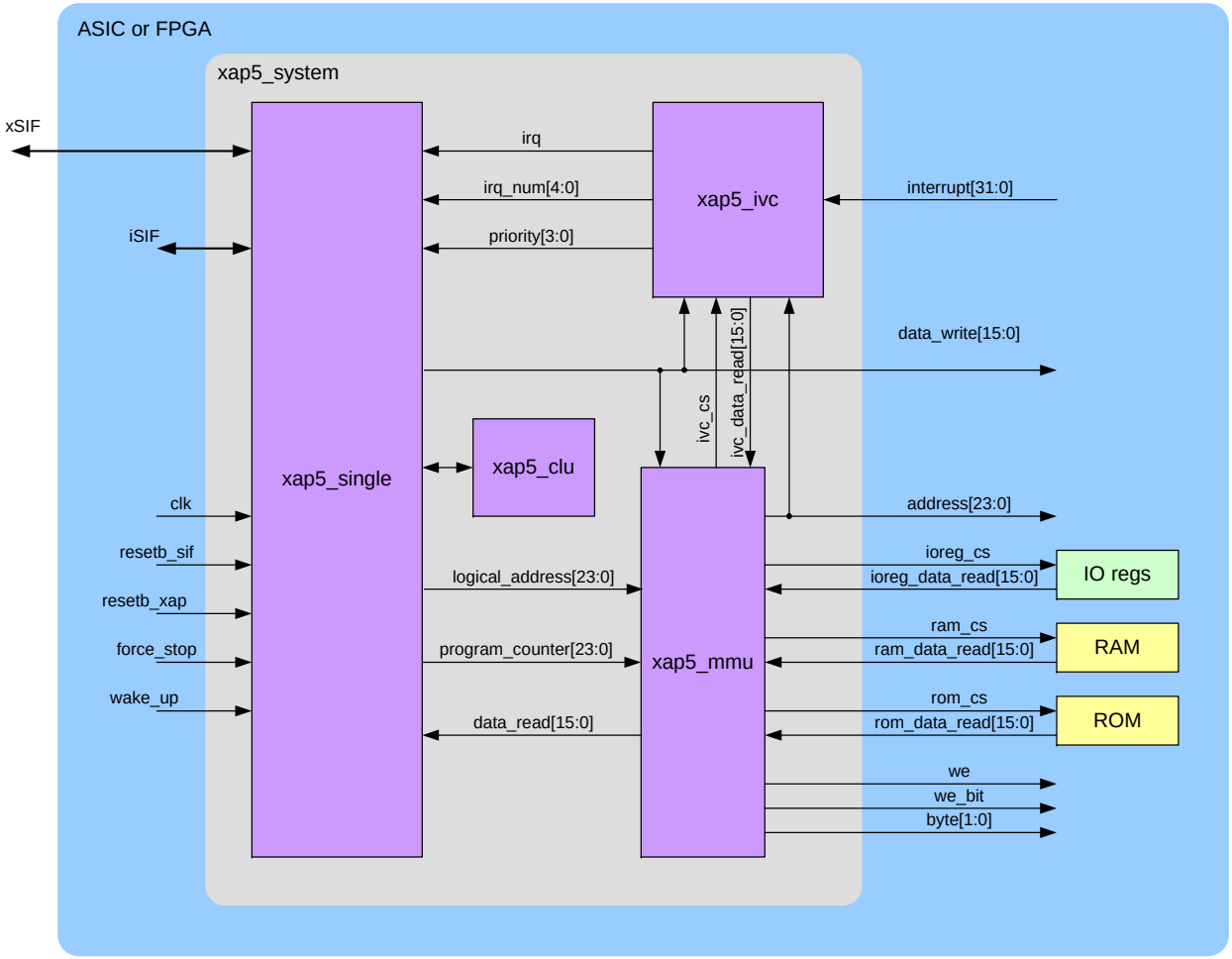
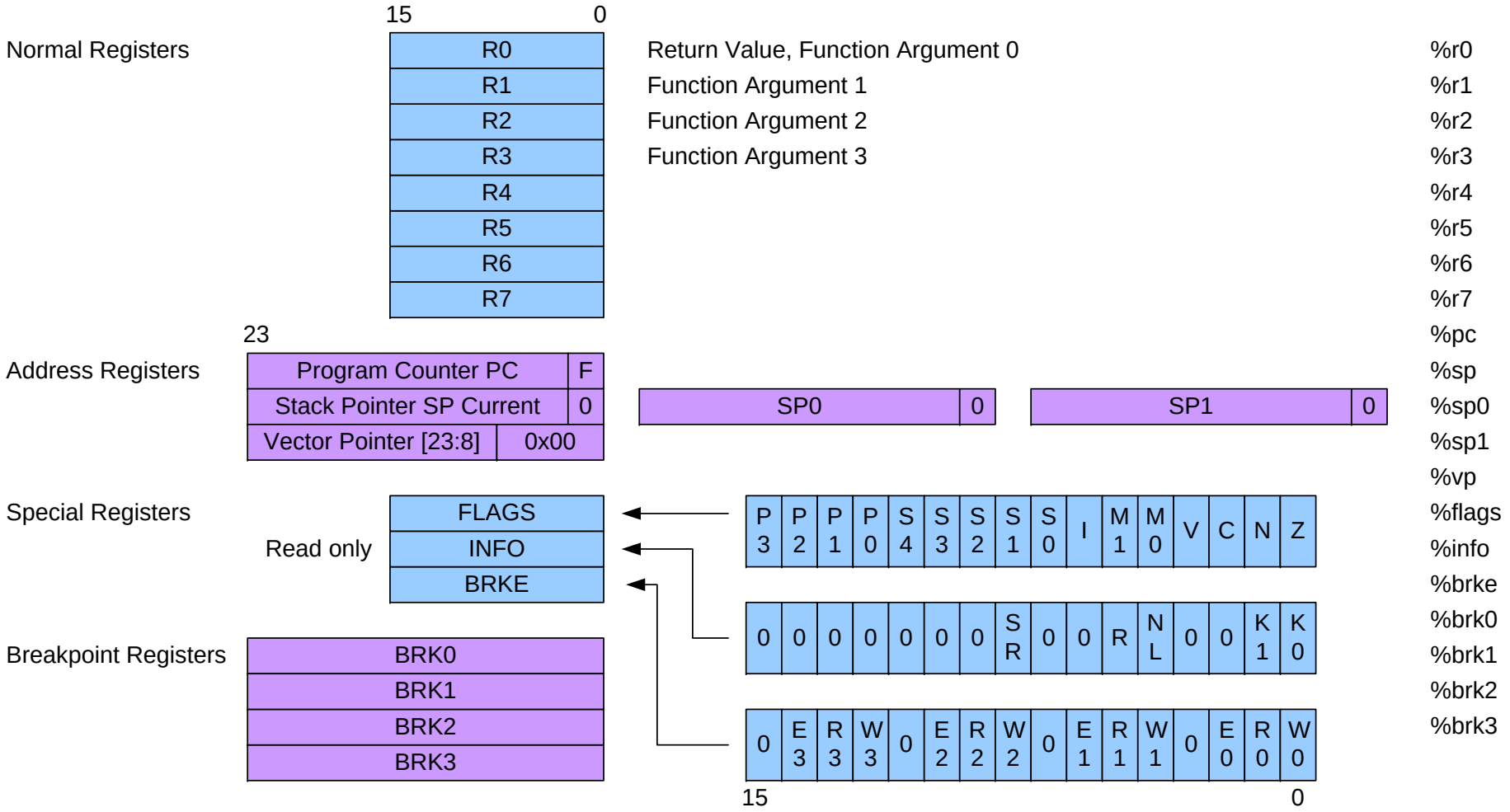
- Example shown is XAP5
- Delivered to licensees as Verilog RTL
  - Fully static design supports clock stopping or frequency changes
  - With test benches, synthesis scripts, documents and tools
- xap5_single is fixed
- xap5_ivc and xap5_mmu are customised per application
- Both minimal and fully featured templates for the IVC and MMU are provided
- xap5_clu is added to execute Custom Logic Unit instructions if needed. No change to tool chain needed
- XAP5 supports 32 interrupts (4 NMI and 28 maskable) and 32 exceptions
- Unified data and address bus
  - Von Neumann design



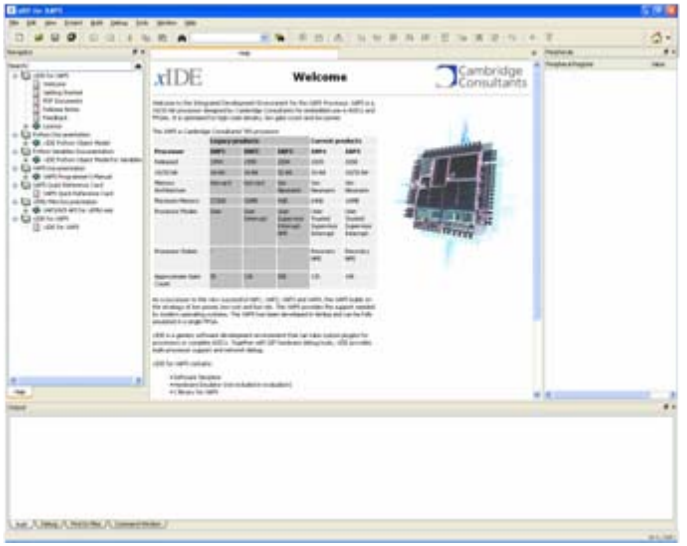
XAP5 programmer's model



XAP tools – xIDE and GCC / binutils

XAP®

- Download from www.cambridgeconsultants.com/xap
- Leverages investment in GNU compilers and tool chain
  - Compilers for C and ADA (C++ soon)
  - Achieves very high code density
  - World class verification and debug tools
- xIDE provides:
  - an extensible instruction set software simulator
  - Real time hardware interface to target device



- Tools use the published xSIF API for non-invasive debug
  - xIDE
  - SIF Explorer
  - Python scripts
  - Custom applications (e.g. LabView, Matlab, C, C++, python)

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Three example applications of XAP within a space environment

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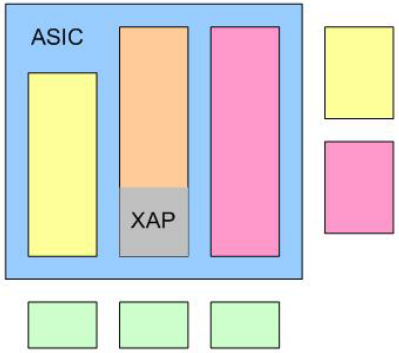
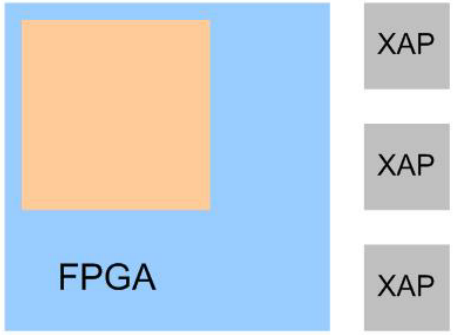
- Some examples of how XAP could be used within a space mission
- Not exhaustive or particularly detailed!
- First application shows XAP as a master processor within a mixed signal ASIC
- Second application shows XAP as a slave processor to a larger FPGA
- Third application is XAP as an always-on house-keeper on a ASIC which also includes a larger processor which is powered up and down as required.

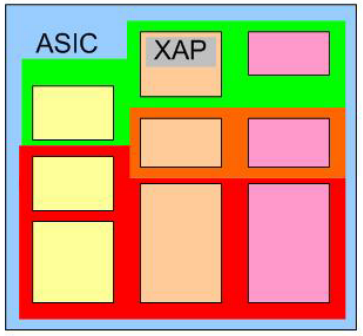
1) XAP as Master



2) XAP as Slave



3) XAP as housekeeper



1) XAP as Master – here the XAP is the main or only processor in the system

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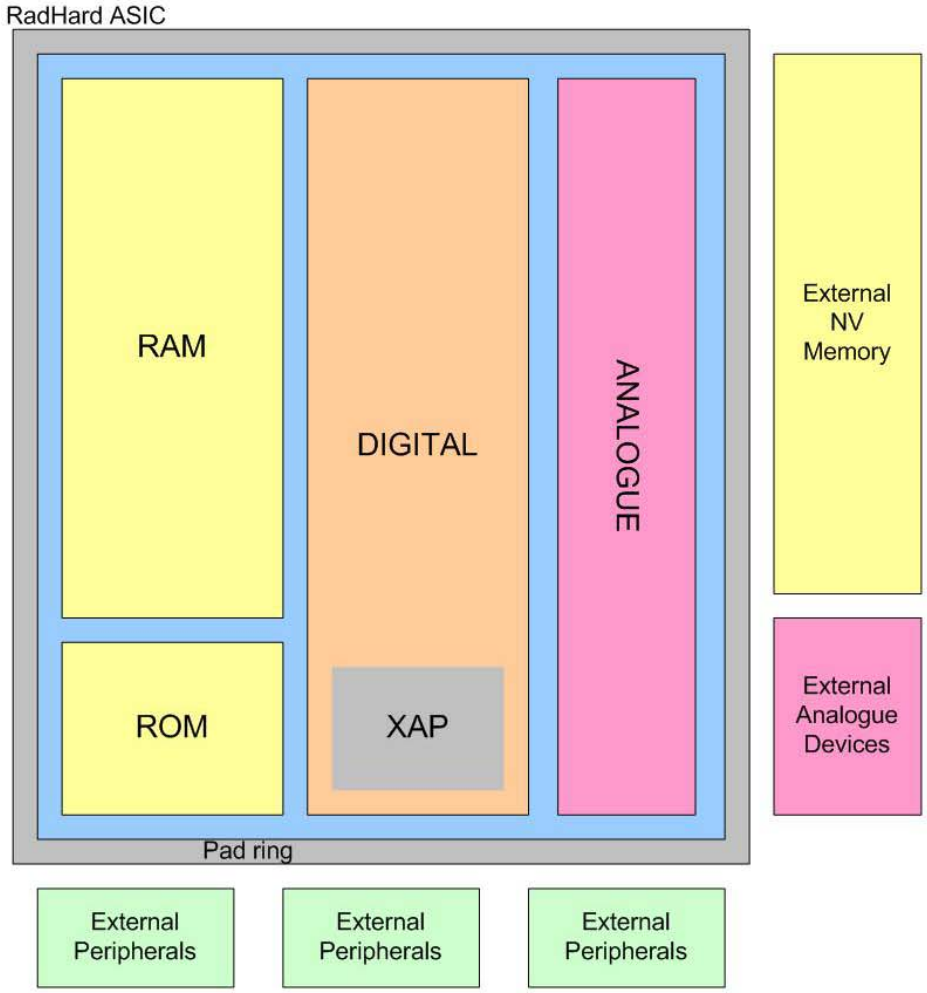
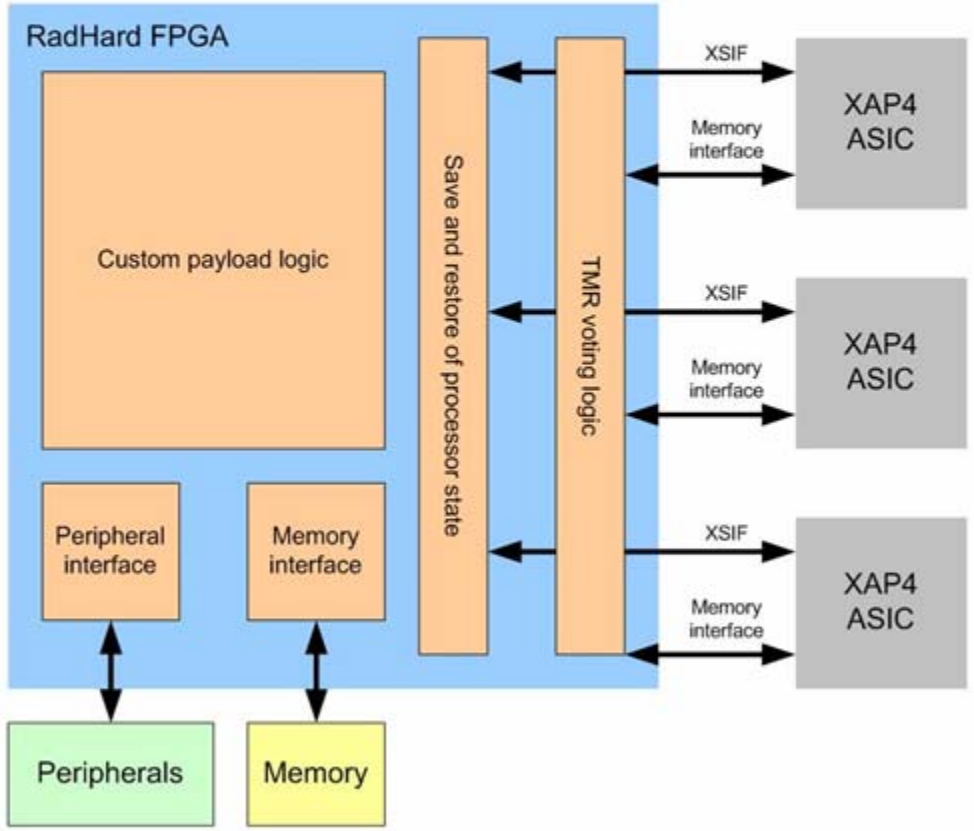
- Customised memory manager with error detection and correction (EDAC) on both on and off chip memory
- Both corrected and uncorrected memory errors can cause interrupt or exceptions as required
- Software counts memory errors and scrubs memory when some threshold is reached
- Memory scrub and DSP functions are activated by custom assembler instructions in CLU
- Connects to a few peripherals and some custom logic (e.g. DSP) in the FPGA.



2) XAP as Slave – here XAP performs processing under the control of another device

XAP®

- XAPs used in Triple Majority Redundancy (TMR) at ASIC level to provide fault tolerance
- XAP controls peripherals such as solar panel pointing etc
- TMR and other custom logic happens on a RadHard controller FPGA
- If errors are detected, state of XAP is saved and restored by FPGA



3) XAP as housekeeper – saving power by turning off bigger blocks

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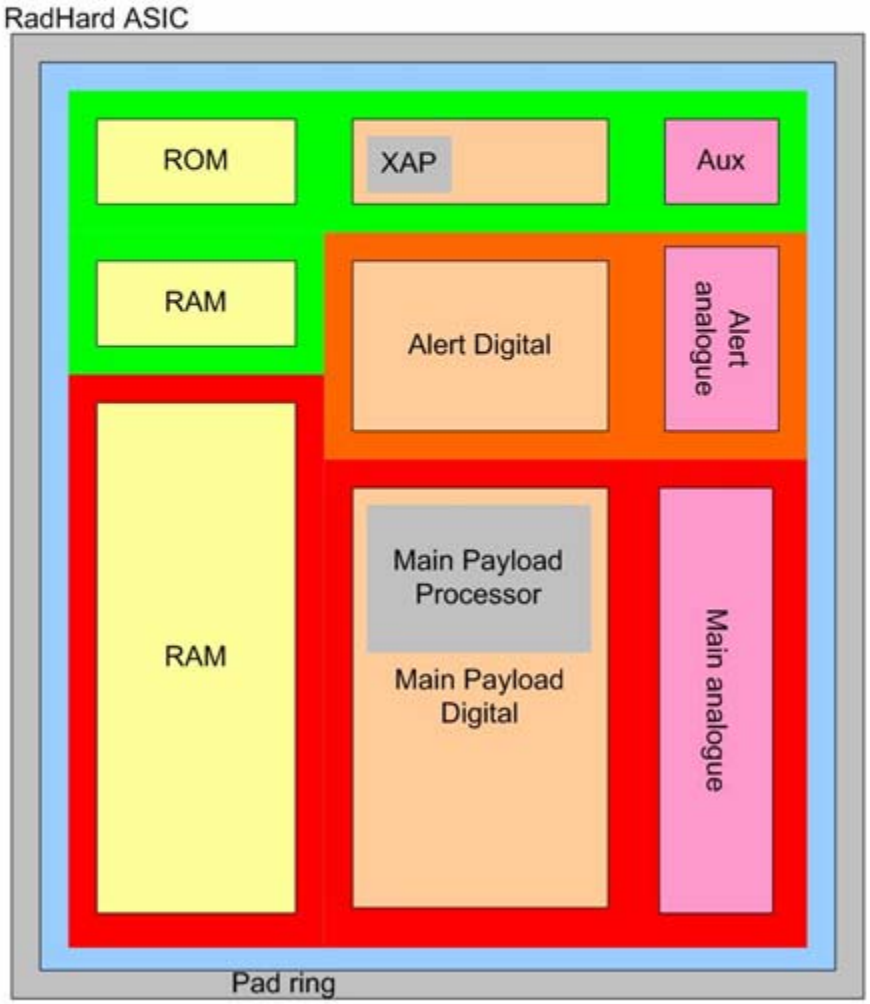
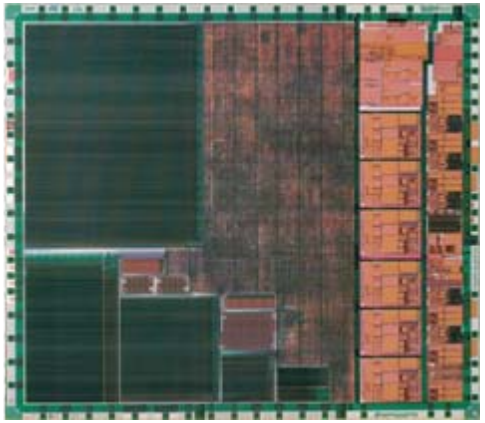
- Different parts of the ASIC can be powered as required, under control of the XAP
- XAP, some memory and some auxillary analogue are always on
- Periodically, the XAP wakes some alert logic to check for "interesting" events
- When an event is detected, the main payload processor is powered up and restored by the XAP
- XAP can monitor output of the main logic for SEU type errors



What features of XAP are most useful for space applications?

XAP®

- Low power
- Few gates
- Small memories because of high code densities
- Flexible memory interface
- Customisable interrupts, exceptions and instructions
- Easy restore of state
- Non-invasive debug
- State of the art tools
- Rich, dense, regular instruction set
- Can be used in ASICs and FPGAs



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