New On-board Microprocessors

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R o l a n d W e i g a n d

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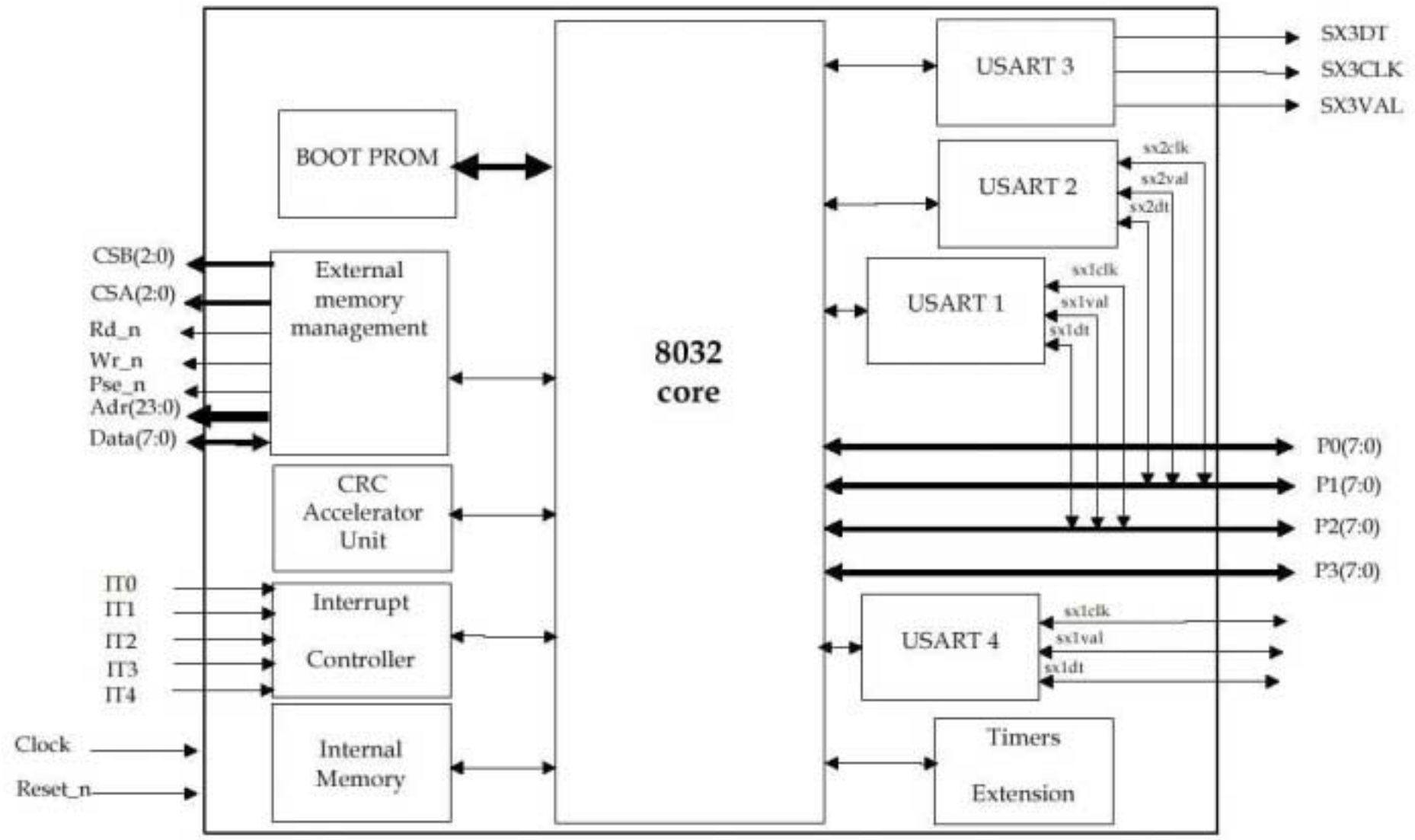
The Microelectronics Section

- ***Part of the Control and Data Division (TOS-ES) of ESTEC***
- ***Microelectronics design, technology and methodology needed by control, data and signal processing systems for spacecraft platforms and payloads***
- ***Specialist support in its domain of competence to ESA projects, to other sections/divisions in the department and to the European space industry***
- ***Research in the area of microsystems and microelectronics with the particular goal of promoting the miniaturisation of spacecraft electronics***
- ***Promoting techniques and methodologies for microelectronic design and development, in concert with the quality assurance department.***
- ***Promoting the development and distribution of building blocks (IP-cores) for system-on-chip devices for the use in European space projects***
- ***Promoting the development of standard components (ASIC, processors) for the use in European space projects***
  - 8-bit microcontroller: ADV80S32
  - 32-bit SPARC V8: LEON1

80S32 Microcontroller Overview

- ***Fully compliant to the Intel 80x1 (8051…) architecture***
  - 8051 + additional standard peripherals = 8052
  - 8052 without program ROM = 8032
  - 8032 for space usage = 80S32
- ***512 bytes on-chip RAM***
- ***Bootstrap PROM for SW download via CCSDS TM/TC packets***
- ***Memory interface for up to 16 Mbyte data and 8 Mbyte program***
- ***3 counters with extended time count duration (16 bit @ CLK/12)***
- ***4 USART supporting RS232, PacketWire and TTC-B-01***
- ***5 external interrupts***
- ***Hardware acceleration for CRC calculation***
- ***Radiation tolerant technology***
  - 0.5 µm ATMEL MG2RT: latchup and total dose (100 kRAD) immunity
  - SEU hardened flip-flops used for critical registers
  - Built-in 8+8-bit EDAC protection for internal and external memories

80S32 Architecture



80S32 Peripherals

- ***1 Standard 80C52 UART (RS232)***
- ***3 additional USART configurable in 3 operating modes:***
  - RS232 asynchronous (full duplex 8 bit words)
  - PacketWire synchronous (half duplex byte packets)
  - TTC-B-01 synchronous (half duplex 8 or 16 bit words)
  - Two 64 x 8-bit FIFO's for USART data buffering available
- ***Interrupt controller for 15 interrupts, polled at each clock cycle***
  - 5 external interrupts
  - 3 timer interrupts
  - 5 USART interrupts
  - 2 interrupts for external and internal memory error
- ***CRC accelerator unit for CCSDS Telecommand/Telemetry***
  - 16-bit CRC Calculation mapped to Special Function Registers
- ***4 x 8-bit PIO (parallel input/output) ports***
  - Pins shared with alternate functions (RAM expansion, USART's, timers)

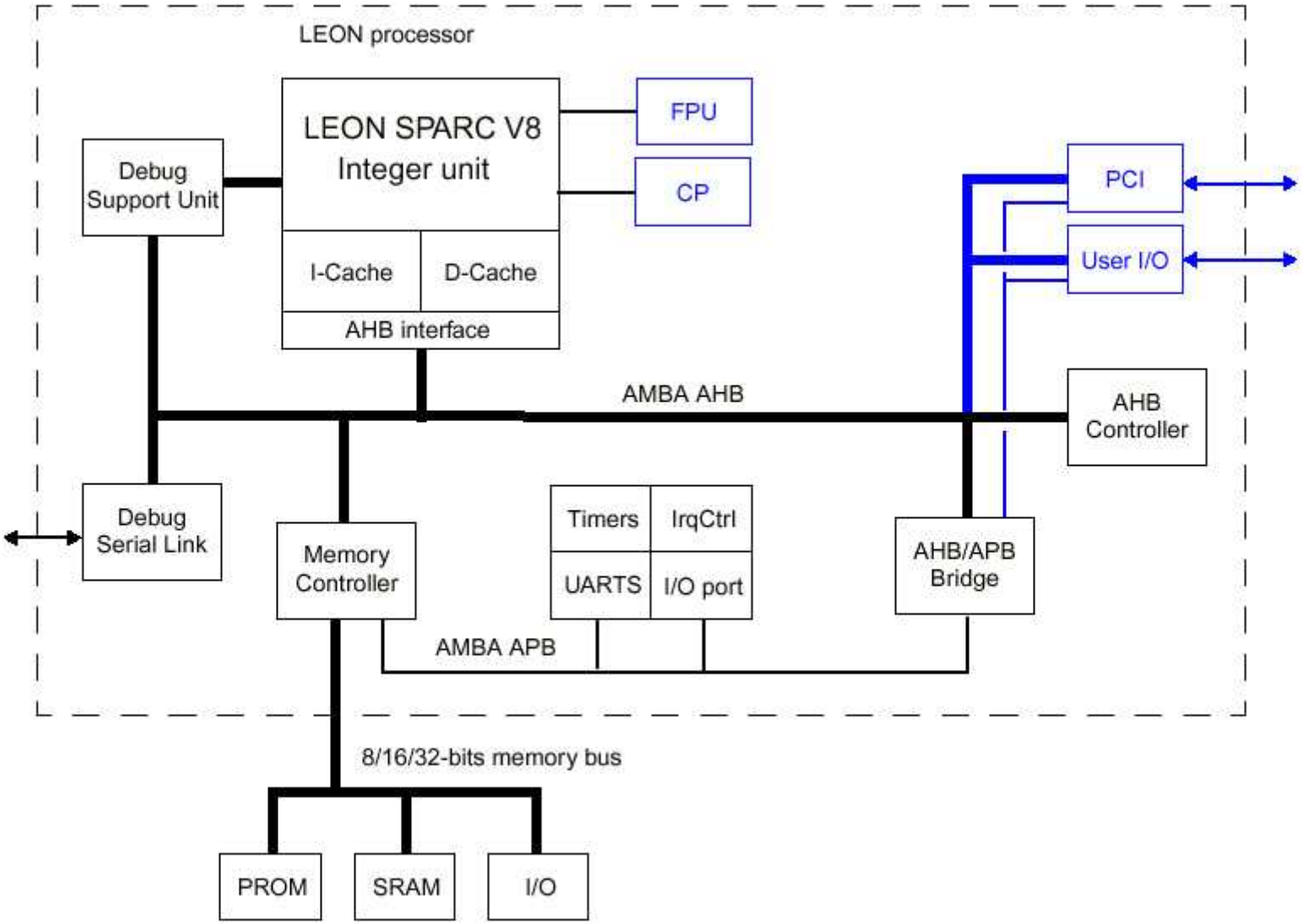
80S32 Summary

- ***Package: MQFP 100 (100 pin, 20x20 mm)***
- ***Supply Voltage 5V***
- ***Max. clock frequency 20 MHz (estimate)***
- ***Performance 3 MIPS @ 20 MHz***
- ***Power consumption 235 mW @ 20 MHz***
- ***Development Tools***
  - Keil
  - Dolphin
- ***Availability***
  - Prototypes produced and tested in 2001
  - Datasheet available at ESA Microelectronics web site
  - Validation and production release outstanding
  - Distribution by Atmel and support by Transwitch (ADV)
- ***Applications***
  - Controlling in instruments, antennae and sub-systems
  - Main processor on small satellites

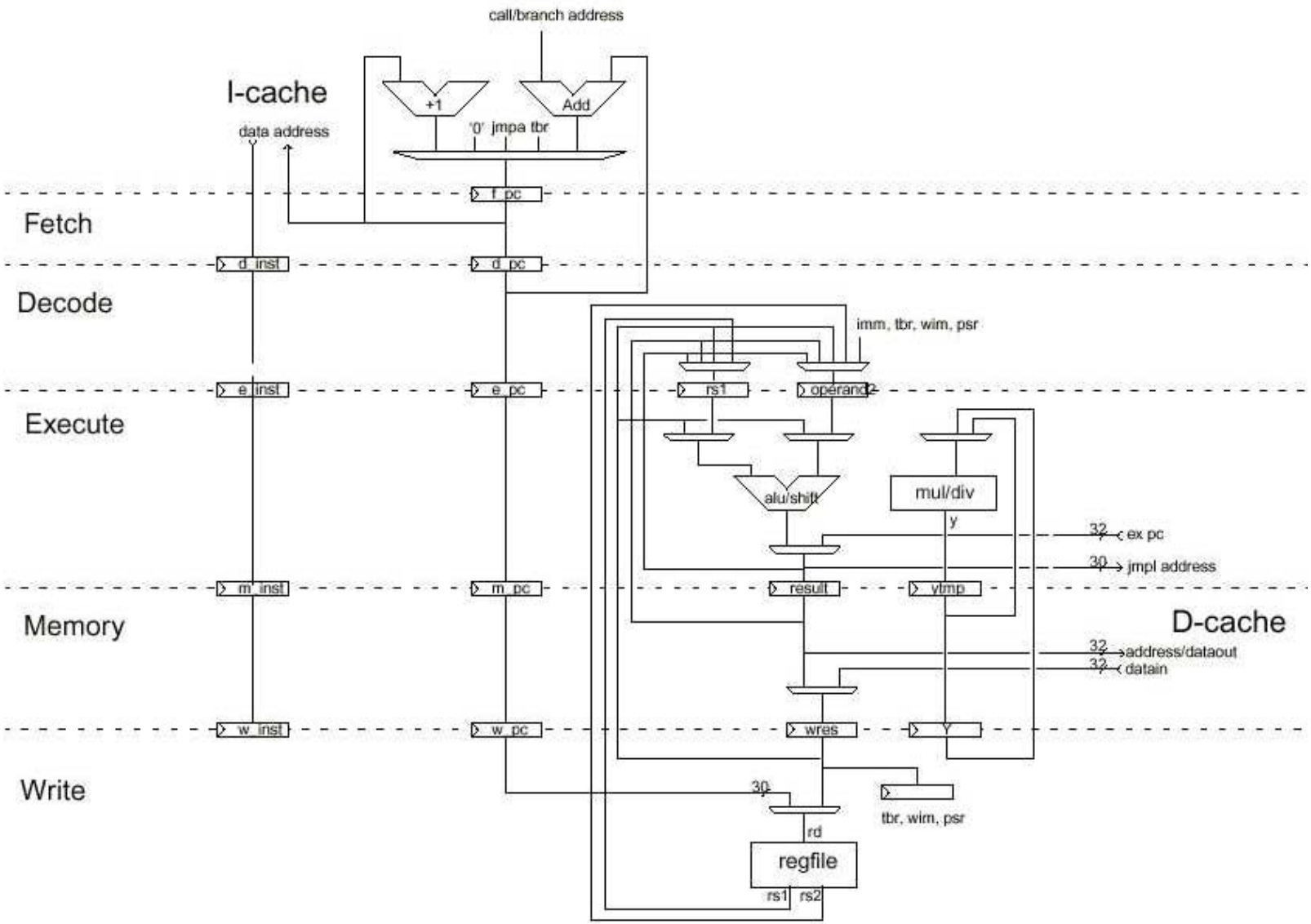
LEON Processor Overview

- *LEON is a highly configurable VHDL model → System-On-Chip*
- *32-bit SPARC V8 Integer Unit, 5 pipeline stages, HW mul/div/mac*
- *Register Files supporting 2 – 32 register windows*
- *Harvard architecture: separate instruction/data caches (1-64 kByte)*
- *8/16/32 bit wide external SRAM (SDRAM planned)*
- *Hook-ups for coprocessor and/or FPU*
- *Standard peripherals: PIO, UART, Watchdog, Timers, Interrupts*
- *Hook-ups for other peripherals via the ARM - AMBA busses*
  - AHB for high speed, APB for low speed
- *Peripherals exist or are under development in form of IP-cores*
  - http://www.estec.esa.int/microelectronics/core/corepage.html
- *Debug support unit for on-chip debugging via a RS232 link*
  - Debugging after various HW and SW breakpoints and –conditions
  - Access to processor registers and instruction or AMBA bus transaction trace
- *Fault tolerance through EDAC and TMR flip-flops*
- *Performance ~ 1 dhrystone MIPS/MHz*

LEON Architecture



LEON Integer Unit

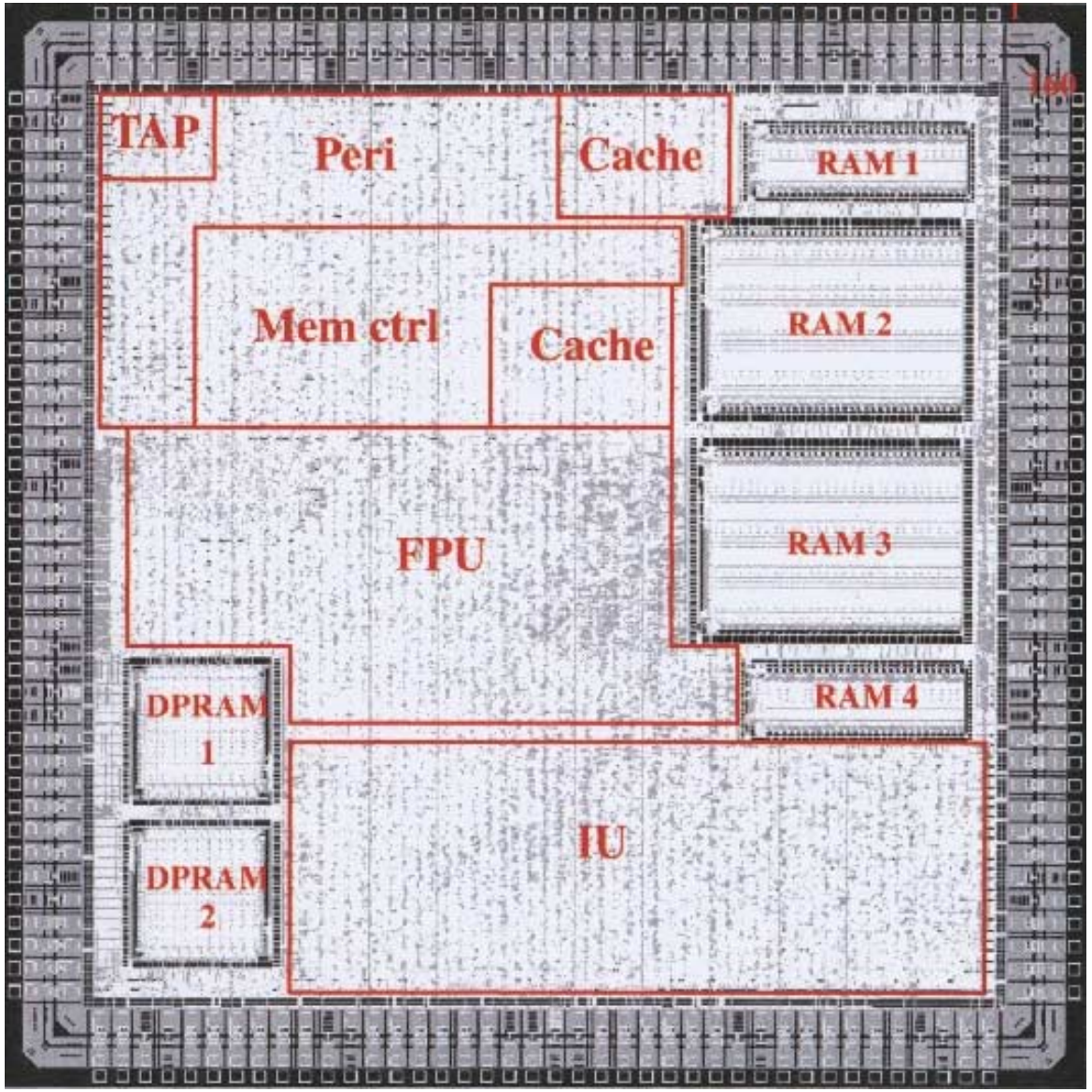


LEON Implementations and Schedule

- ***LEON1 Express: ES produced/tested on Atmel 0.35 µm (2000/2001)***
- ***Several FPGA implementations (Xilinx, Altera), ~ 25 MHz***
- ***Commercial/University implementations on TSMC/UMC 0.18 µm***
- ***LEON2 configuration:***
  - Advanced fault-tolerance achieved with EDAC and TMR
  - 2x8kByte data/instruction cache, 8 register windows
  - Meiko FPU (Sun Microsystems Communitysource)
  - 16x16 bit HW multiplier, HW divider (radix2)
  - MAC (16x16 bit to 40 bit accumulator)
  - 33 MHz 32 bit PCI master/target
  - Debug Support Unit (DSU)
- ***LEON2 prototypes***
  - UMC 0.18 µm commercial technology, 120 MHz (Q3/2002)
  - Atmel 0.25 µm radiation hard process, 80-100 MHz (Mid/2003)
- ***LEON2 production release in Atmel 0.25 µm (Mid 2004)***
- ***SW tools available from Gaisler Research:***
  - Simulator TSIM, LECCS: LEON/ERC32 cross-compiler system (GNU)

LEON1 Express

- *Fault-tolerant version 2.1*
- *EDAC for memories*
- *TMR flip-flops*
- *Meiko FPU*
- *2*4Kbyte caches*
- *Atmel ATC35 0.35 µm*
- *Latchup-free,*
- *Total-dose 300 Krad*
- *Total Area: 40 mm2*
- *Core 30 mm2, 70 kGates*
- *RAM blocks 10 mm2*
- *Pads 10 mm2*
- *Clock frequency 40 MHz*



Links

- ESA Microelectronics: http://www.estec.esa.int/microelectronics
- Transwitch: http://www.transwitch.com
- Keil Software: http://www.keil.com
- Dolphin Integration: http://www.dolphin.fr
- Gaisler Research: http://www.gaisler.com
- Atmel Wireless: http://www.atmel-wm.com
- LEON mailing lists:

  http://www.yahoogroups.com/group/leon_sparc

  http://www.yahoogroups.com/group/leon_announce

  http://www.yahoogroups.com/group/leon_dev