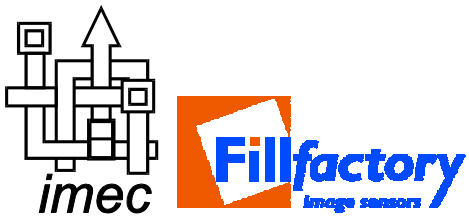

STARS-3: Fully Integrated Communication Terminal and Equipment: Image Compression Camera

Work Package 2300

IRIS-3 Datasheet

Specification	:	Deliverable D25
Authors	:	W. Ogiers (FillFactory n.v.)
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issue	Date	description of change
0.1	11/07/2002	Created from P50314-IM-DL-003 Imager Specification
0.2	18/02/2003	Added final pin lists. Added logic IO DC electrical specification. Added bug list (section 2.8)
0.3	20/03/2003	Added electro-optical specifications after device characterisation. Added to package drawings.
0.4	30/4/2003	Modified data alignment when used with 8 bit SDRAM: new section 2.4.7 and updated pin list.
1.0	02/09/2003	Added total dose radiation data, including despecification above 30 krad. Cleaned up sections 1.1 and 1.2. Redefined document as deliverable D25.
1.1	28/10/2003	Added heavy ion SEU/LU data. Dropped ‘confidential’ label.

Table of contents

Purpose

This document is the datasheet for the IRIS-3 image sensor chip, detailing its operation and performance.

Scope

This is deliverable D25 in the STARS-3 activity Image Compression Camera, ESA contract number 13716/99/NL/FB. It is an evolution of D12.

Applicable documents

[AD11] P50314-IM-DL-0001, *"Image Compression Camera Requirements Specification"*, deliverable D1 in STARS-3 activity Image Compression Camera

[AD21] ABB HAFO, "*VCA HAF_12399 Virtual Channel Assembler: Preliminary Datasheet*", January 1994

[AD22] GEC Plessey DS3839-4.2, "*MA28140 Packet Telecommand Decoder: Preliminary Information*", March 1995

[AD23] Dornier XM-IF-DOR-0001, "*XMM Electrical Interface Requirement, issue 5"*, 26/08/1997

[AD24] ESA PSS-04-106, "*Packet Telemetry Standard, issue 1*", January 1988

[AD25] ESA PSS-04-107, "*Packet Telecommand Standard, issue 2*", April 1992

[AD26] CCSDS 102.0-B-4, "*Packet Telemetry*", November 1995

[AD34] P50292-IM-RP-003, "*Minutes of Progress Meeting Nr. 1"*, Apr. 22-23, 1996

[AD41] RE-VMC-017-OIP/99, "*Visual Monitoring Camera: Design Description for the VMC IRIS Cameras, issue 3*", DSS-OIP, 5 May 1999

Reference documents

[RD1] Datasheet: Hitachi HM5225805B 256 Megabit SDRAM

[RD2] Datasheet: NEC mPD45256841 256 Megabit SDRAM

[RD3] Datasheet: Micron MT48LC32M8A2 256 Megabit SDRAM

[RD4] Datasheet: Samsung K4S560832A 256 Megabit SDRAM, Oct. 1999

[RD5] ABB HAFO, “VCA HAF-12399 Virtual Channel Assembler, Preliminary Data Sheet”, January 1994

Abbreviations and acronyms

e-	Electron(s), used for expressing signal levels at a pixel site
APS	Active Pixel Sensor
ASIC	Application-Specific Integrated Circuit
BGA	Ball Grid Array, surface mount IC package type
CCSDS	Consultative Committee for Space Data Systems
DS	Double Sampling
EDAC	Error Detection And Correction
FF	Fill Factor
FW	FlexWave, internal name for ICA
FPA	Focal Plane Array
FPN	Fixed Pattern Noise
FSM	Finite State Machine
ICA	Image Compression ASIC: wavelet-based compression engine (IMEC, 2000)
ICC	Image Compression Camera: compact camera combining the ICA and the IRIS-3 into one unit.
IRIS	Integrated Radiation-tolerant Imaging System: series of image sensors
Mps	Megapixels per second
PGA	Pin Grid Array, through-board IC package type
QE	Quantum Efficiency

RTU	Remote Terminal Unit, spacecraft's data receiver.
S/C	SpaceCraft
SDRAM	Synchronous Dynamic RAM
SNR	Signal to noise ratio
TBA	To Be Assessed
TBC	To Be Confirmed
TBD	To Be Determined

1 IRIS-3 overview

The Integrated Radiation-tolerant Imaging System 3 (IRIS-3) is a CMOS camera-on-a-chip with full digital interfaces that comply with spacecraft telemetry standards. It is profiled as a general purpose high-quality greyscale imaging component, to be used as a core block for miniature cameras for a wide range of spaceborne applications. These applications include robotics, low-to-medium quality earth and planetary imaging, compact lander and rover cameras, and visual telemetry.

The IRIS-3 offers enhanced functionality such as:
- A choice of on-chip digital I/O interfaces
- Control of a local industry-standard SDRAM buffer for image storage
- Direct interfacing with the ICA wavelet compression engine

The IRIS ASIC comprises a full custom mixed analogue-digital part: the actual pixel array along with its lowest-level timing and control circuitry and an ADC. In addition, there is a cell-based purely digital part: the local controller that drives the pixel array, captures the data from the ADC and interfaces with the outside world.

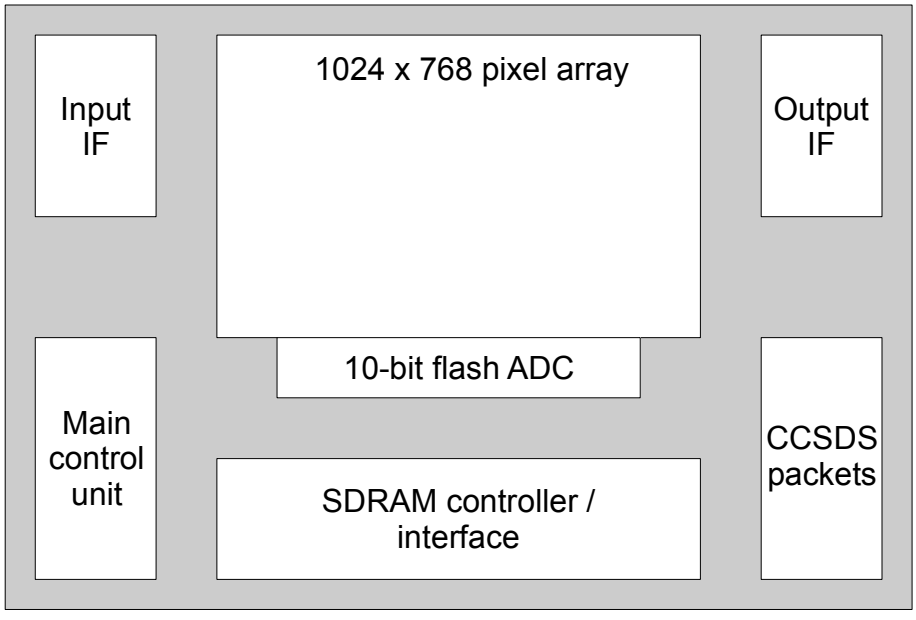


Figure 1.1 : IRIS-3 image sensor block diagram

1.1 Radiation tolerance

IRIS3 consists of a radiation-hardened pixel array and ADC, combined with control and interfacing logic made of commercial/industrial standard cells.

The total dose (gamma) radiation tolerance is 30 krad (Si) for operation withing specification. Doses up to 80 krad can be tolerated with reduced eletro-optical performance with with strongly increased supply current for the chip's logic.

The device is free of latch-up up to LET=55.9 MeV/mg/cm² and 11000 ions/s/ cm².

At a beam flux of 10 ions/s/cm² no SEUs were observed. At a beam flux of 100 ions/s/cm², no SEUs were recorded at a fluence of less than 2300 ions/cm²

1.2 Electro-optical characteristics

	value	remarks
pixel architecture	integrating APS	3 transistor photodiode pixel
format	1024x768 pixels	
pitch	15 μm	
die size	19x19mm	
blooming tolerance	High	
fill factor (FF) x Quantum Efficiency (QE)	>26 %	480-650nm band
optical bandwidth	400-900nm	FF x QE > 5%
MTF	> 0.26	-
voltage conversion factor	10.4μv/e-	
noise	53 e-	

saturation level	247500 e-	
saturation level for 1% linearity	170000 e-	
optical dynamic range	64 dB	

dual slope mode		selectable, expands dynamic range through non-linear pixel transfer function
remaining non-uniformity	0.57%	in the dark
dark current generation (21°C)	2200 e-/s	
readout method	on-chip Double Sampling	
electronic shutter	yes	non-synchronous 'rolling blade' type
nominal exposure time range for full-size images	100µs-100ms	shorter when using windows, longer in over-exposure mode
image stare time		equal to the integration time plus the (sub)frame readout time
nominal frame time	~100ms	for rated maximum full frame speed of 10Hz
ADC	on-chip 10 bit flash ADC	

1.2.1 Integrating active pixel sensor with on-chip double sampling

The pixel architecture employs one photodiode, a local source follower, a reset transistor and a row-selection transistor per pixel. With a 0.5µ process the minimal pixel pitch is 15 µm (square), including radiation-hardening structures.

Processing-induced row and column non-uniformity is suppressed in *double sampling* column amplifiers, one for each column. Signal degradation components that are not compensated for are the reset noise in each pixel and the offset caused by non-uniform dark current generation, and its associated shot noise.

1.2.2 Format 1024 x 768 pixels

A minimum format of 1024 x 768 pixels is required, to offer a considerable improvement over previous imagers such as IRIS-1 and 2. However, due to the constraints posed by the envisaged 15 x 15 μm size of rad-hardened N-well pixels, in combination with a manufacturing reticle size of 19 x 19 mm, 1024 x 768 pixels is also the largest possible imager than can be made.

1.2.3 Noise, sensitivity and dynamic range

Previous IMEC imagers such as IRIS-1 and Ibis-4b were optimised for low absolute levels of noise and high sensitivity, hereby somewhat sacrificing the pixel well capacity and total dynamic range.

Space scenes are rich of contrast and have thus a high dynamic range. In addition, in space monitoring applications absolute levels of intensity are high, even when f/4-8 lenses are employed.

For IRIS-3 it is proposed to not pursue the lowest possible noise and the highest possible sensitivity, but rather to strike a balance between an acceptable noise behaviour and a large dynamic range.

1.2.4 On-chip ADC

The IRIS-3 chip features an on-board 10MHz 10 bit flash ADC. This component has previously been used on the Ibis-4b and 4c imagers.

1.2.5 Image readout rate, system clock frequency

IRIS-3 is designed for a nominal image readout speed of 13 frames per second, amounting to a pixel rate of approximately12.5MHz. This requires a system clock frequency of 25MHz. Temperature range and thermal effects

1.3 Functional specification

on-chip logic	yes	for timing, control and high-level interfacing
user commands		high-level user commands, following the IRIS/VMC/XMXU command template
image access method	line scan	progressive line-scan, synchronous to local clock, idle times between lines and between frames; no random access; re-configuration for windowing or subsampling causes latency times about the duration of the current integration time
windowing	yes	one window, position and size adjustable in fixed increments
subsampling	yes	sparse sampling, NxM subsampling yields ~NxM gain in frame rate
exposure control	yes	fully manual, fully automatic, or bracketed around a center value
autonomous mode	yes	hardwired mode selector, puts camera in automatic image capture mode or in interactive command mode after power-on
fault tolerance	yes (limited)	some commands imply a system restart; system has limited parity control and can report fault occurrences to end-used (TBC)
packetised data and commands	Yes	selectable: off, CCSDS-style grouping, ESA-style segmentation
pixel data resolution	-	two modes: 8-bit pixels or 10-bit pixels .
stand-alone mode	Yes	sensor dumps images onto output interface during image acquisition
buffered mode	Yes	images are acquired and stored in a local SDRAM buffer, for later download over the output interface
image compression mode	Yes	images are sent to the ICA via an SDRAM buffer. Compressed data are received through the same buffer and downloaded over the output interface. ICA can be transparently controlled through direct user-access to the SDRAM buffer.
SDRAM control	Yes	IRIS-3 controls external SDRAM, which can be shared with one other device (e.g. ICA) under arbitration of IRIS-3
SDRAM scheme	-	two schemes: 8-bit wide memory without EDAC, or 16-bit wide memory having 10-bit wide data words and 4 bits for EDAC.

1.3.1 On-chip timing and control

The IRIS imager section consists of the actual focal plane and its associated low-level readout logic. This plane requires a carefully timed sequence of control signals to be read out. The responsibilities of the IRIS controller section are: low level timing and control of the image plane, implementations of extra readout functionality (windowing, sparse sampling, shutter control,...), interpretation and execution of high-level user commands, and finally the provision of the necessary hardware interfaces to the outside world, to a local industry-standard SDRAM buffer, and to the ICA wavelet compression chip.

1.3.2 SDRAM interface

IRIS-3 interfaces to industry-standard SDRAM. No alternative memory types or architectures are supported. This SDRAM can be shared with one external device, the ICA compression chip, to exchange image data and commands. At all times IRIS-3 takes care of the necessary SDRAM refresh control, with the additional demand that this process never disturbs possibly on-going image acquisitions.

1.3.3 User commands

IRIS-3 can be controlled by the end-user via one of three possible command/data input interfaces. The commands to be used include:

- define system parameters
- define image sensor settings (frame position, size, subsampling settings, exposure time and mode, gain, …)
- write digital telecontrol output[1..8]
- read housekeeping information (telemetry inputs, fault status, ...)
- read images directly
- manage memory pointers for read and write
- acquire N images and store in memory
- read N images from memory
- transparently write user-specified portion of memory
- transparently read user-specified portion of memory
- signal ICA
- acquire N images, store them in memory, let ICA process them,
- download compressed images from memory

These commands are similar to the commands used previously in the IRIS-2, VMC, and XMXU camera and memory systems. This way a certain level of cross-system compatibility will be obtained.

1.3.4 Image acquisition mechanism

The imager's readout mechanism is *line*-based, much like a video camera. It runs synchronous to a local pixel clock, and is driven by precisely timed sequences of control signals. A frame rate of 13Hz requires a *pixel clock* of approximately 13MHz. In order to cope with internal timing constraints and interfacing properties, a higher-rate *system clock* is necessary. The baselined clock rate is a system clock of 25MHz, a pixel clock of 12.5MHz, and a resulting image rate of about 13Hz (due to line-based overheads). This selection of clock rates also complies with the maximum speeds of some standard I/O interfaces used.

All frame, line and pixel synchronisation is done locally, synchronous to the local pixel clock. There are no provisions for random access, be it in space or in time. This is a direct result of the integrating nature of the pixels. Another result is that any re-configuration of the readout process (change of window dimensions, change of window position, change of subsampling step size,...) requires a latency equal to the currently-set integration time before the first image line can be put out to the end-user.

1.3.5 Stare time

IRIS-3 is a line-based integrating CMOS imager without local analogue frame memory. Hence, light is not captured at the same instant over the whole pixel plane. If one defines *(image) stare time* as the total period in time a given image has been sensitive to incoming light, then the stare time of the IRIS-3 starts with the reset of the first line, and ends with the readout of the last line in the frame. As a result, the global image stare time is always equal to a single frame (readout) time, plus the selected integration time, meaning that stare time and readout rate are interrelated. This also implies that the imager can not immediately respond to a command by producing a picture, as first the full integration time for the first image line has to be built-up

Within each frame, line stare times are not synchronous to each due to the progressive nature of the line-read and line-reset processes.

The user of an imager of this type must be aware of the fact that exposure time and stare time are not equal, and that the stare time equals the integration time plus the readout

time. The readout time is coupled to the data rate of the output interface when a buffer memory is not used

1.3.6 Windowed readout

IRIS provides for readout of user-selectable parts of the entire focal plane, the so-called window-of-interest readout. Due to the integration mechanism of the imager, reconfiguring window co-ordinates and/or sizes requires first the set-up of internal addressing registers, causing a certain bounded latency, and then another latency time during which the integration time for the first line builds up. The impact of this is that window-reconfiguration can be a relatively expensive operation, the more so when long integration times are employed.

IRIS supports only one active window at a time. The behaviour of the image area lying outside the current window is undefined.

1.3.7 Subsampling

Subsampling is implemented in the digital domain. Using this method an NxM subsampling tile size results in an NxM reduction of data, and an (approximate) gain of NxM in frame rate. Subsampling step sizes N and M of 1, 2, 4 and 8 are allowed. Step size can be independently specified for the Y and X directions.

1.3.8 Variable integration time (electronic shutter)

Integration time can be set by sending appropriate commands to the imager controller. The allowable exposure times are fractions of the current frame read time. With a frame rate of 14Hz and 768 lines, integration time can be set in steps from a full frame time down to approximately one 768th of a frame time, in this case 1/14..1/10832th of a second.

With smaller frames, integration time settings scale. Suppose, for instance, a subframe of 512x384 pixels. This is one quarter of a full image, and hence frame rate will be four times the nominal frame rate, i.e. 56Hz, corresponding to a normal integration time of 1/56th of a second for this frame. The shortest allowable integration time is now 1/384th of this frame time, the exposure range now being 1/56..1/21504 seconds.

Longer integration times than the nominal frame read time ('over exposure') are possible, by introducing wait cycles during which no readout is done. These wait cycles are expressed as an integer number of frame read times. Note that without active cooling, dark current generation will make the imager saturate after 10 to 30 seconds.

After changing the imager's integration time settings, a latency equal to that integration time has to be respected, during which the imager lines take up their correct exposure times.

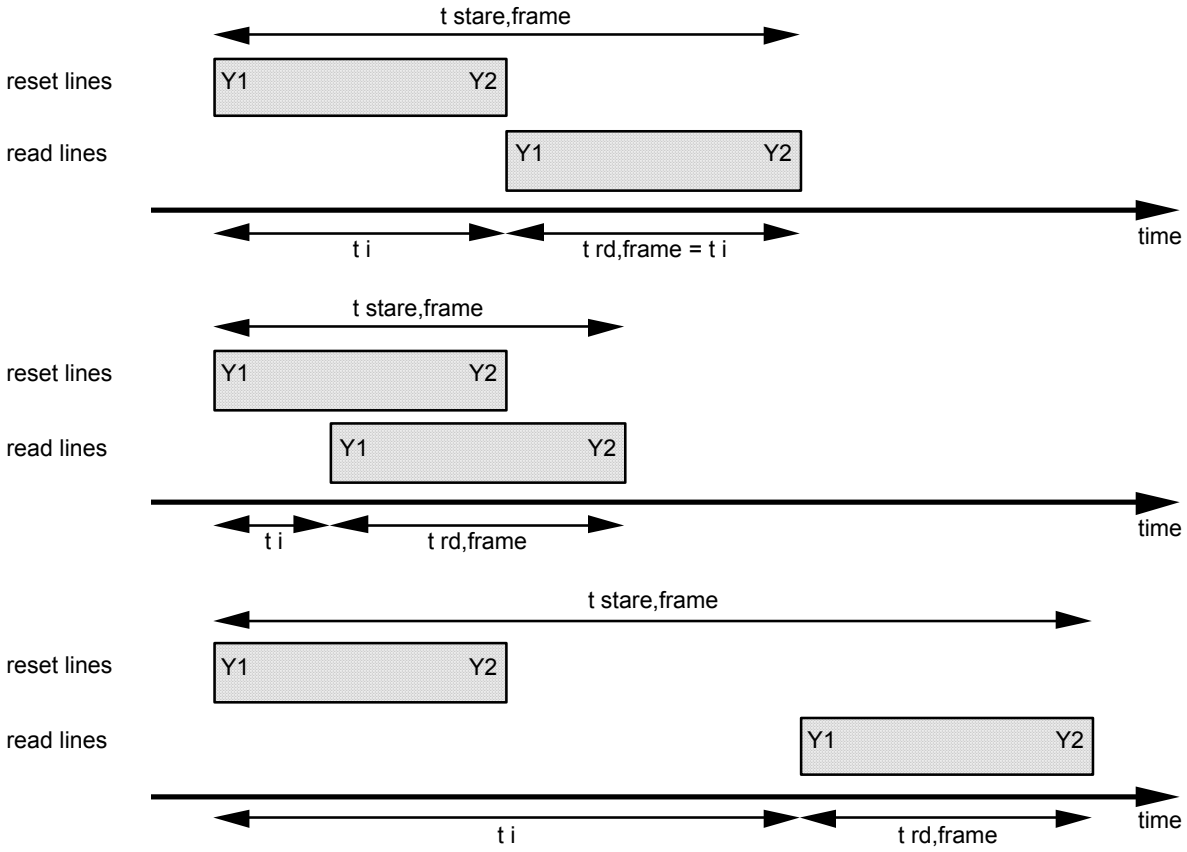


Figure 1.2: Exposure time and stare time for frame-length exposure, under-exposure, and over-exposure

1.3.9 Combining electronic shuttering with windowing and subsampling

The effective integration time is a function of window and subsampling settings, and, when images are not written to the local SDRAM buffer, the available output interface data bandwidth. The integration time should be communicated to the IRIS-3 in the

suitable low-level format, as to be defined in IRIS-3' command format. This format for time settings has the dimension of line co-ordinates on the imager's readout and reset addressing structures. Hence, the end-user is fully responsible for the translation of integration times to co-ordinates, taking into account the bandwidth of the output interface and the current window settings.

1.3.10 Automatic exposure control

The system can be made to perform autonomous control of the integration time. The envisaged method for control regulates the approximately-calculated average light intensity in the most recently taken frame towards a fixed value.

1.3.11 Automatic bracketing

The system can be made to acquire three images for each image requested. These three images each have a different exposure time, centered around the then-holding nominal exposure time.

Two bracketing modes are present:

- Narrow: exposing a series of Exp, Exp x 2, Exp/2
- Wide: exposing a series of Exp, Exp x 8, Exp/8.

Bracketing and automatic exposure control are mutually exclusive.

1.3.12 Dual-slope exposure mode

The intra-scene dynamic range can be expanded by abandoning the standard linear response of the pixels in favour of a bi-linear response curve. Dark areas in the scene experience now a high pixel sensitivity, while brightly-lit parts cause the pixels to convert with a lower sensitivity. The position of the 'knee' in the transfer function of a pixel now is set by the exposure time parameter, which loses its normal meaning, and by an external reference voltage. It is possible to switch between linear mode and dual-slope mode by command.

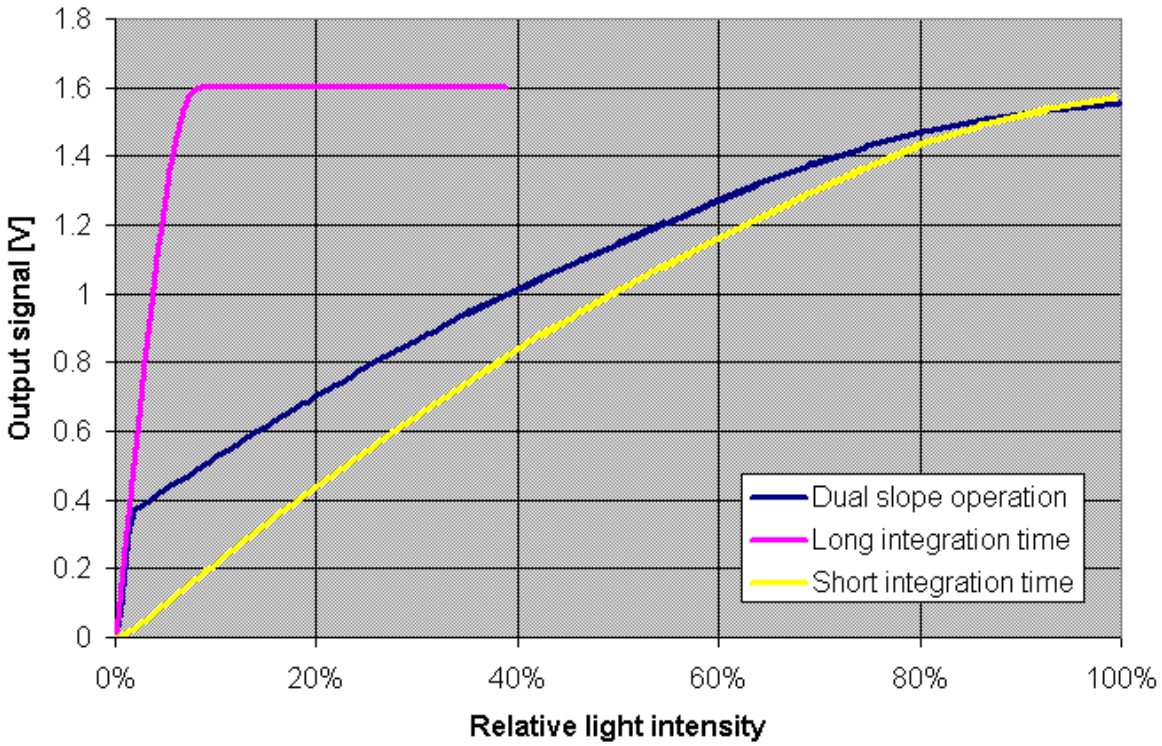


Figure 1.3 : Dual-slope electro-optical transfer curve

1.3.13 System start-up

The behaviour of the IRIS-3 after start-up can be controlled by means of strappable configuration pins, setting:

- start-up scenario
  - automated acquisition and/or storage and/or compression and/or download of images
  - timed instant, triggered instant
- default sensor settings:
  - image size
  - exposure time
  - exposure mode: fixed, automatic, bracketed

1.3.14 Triggered actions

A transient signal on an external trigger port, fed into the IRIS-3, causes the execution of the system start-up scenario as described in above paragraph.

1.3.15 Fault tolerance

The following fault-tolerancing strategy will be implemented:

- command and data interfaces have watchdogs that re-initialise the associated FSMs when no action has been seen in the past 1-2 seconds.
- the main control FSMs have their state register protected by tripple-voting.
- all FSMs return to their initial state whenever an illegal state is encountered
- all memory access pointers and write-locks are protected by tripple-voting
- long-term settings registers (imaging parameters, ...) are protected by tripple-voting
- the internal command reset mechanism is protected by tripple-voting

Stored data are protected as follows: when a 16-bit wide image buffer SDRAM is employed, 10-bit data words in this buffer are protected with 4 additional EDAC bits, providing the correction of 1 bit-error per word. In this scheme, two bits of the word are not used.

Downloaded data can be protected with the same EDAC scheme.

1.3.16 Analogue gain setting

In order to make optimal use of the on-chip ADC, even when viewing low-contrast sceneries, the gain of the voltage amplifier before the ADC is made user-controllable. One of three available hardwired gains can be selected by command. Normally, this command should be issued prior to actual image acquisition, so that the user actually knows the gain used during acquisition. However, the command can also be issued *during* on-going image acquisition; one should realise here that changing gain when reading out a frame effectively corrupts the current frame's data.

It should be noted that this configurable gain by no means can be considered as a calibrated or precise extension to the ADC's resolution..

2 Detailed description

2.1 Operational modes

2.1.1 Stand-alone single-chip camera

In this mode IRIS-3 behaves as a camera without any form of on-line image storage or buffering. Image acquisition commands are received and processed, the output containing an image, a stream of images, or housekeeping data, with or without CCSDS packetizing.

Flow control at the data interfaces is not possible; the available bandwidth at the data interfaces has a direct impact on the framerate, and coupled to this on sensor parameters like exposure time.

In this mode IRIS-3 functionality closely mimicks the older IRIS-2 chip, or perhaps even a digital video camera.

The following image gathering scenario is supported:

- Take N images (N=1..128 or infinite), spaced T seconds in time (T=0..TBD) and download them while acquiring. The image exposure time and acquisition time depend on the available download bandwidth. The inter-image time T is defined as between the end of the previous download and the start of a new acquisition. Each image can be preceded with a housekeeping packet. (READ_FRAMES and READ_HKFRAMES command).

- The initiation of above procedure can be power-on , after an external trigger signal, or after a command, with a delay.

2.1.2 Camera with local image buffer

In this mode images can be acquired directly, as in stand-alone mode, or they can be buffered in a local SDRAM mass memory. The end-user can then retrieve the images from the memory at a later time. CCSDS packetizing can be used.

Commands are available for writing a specified number of images to the memory, with a specified period of time in-between two successive images. Commands are also available for reading any specific image from memory, or for reading the whole memory as a circular buffer.

When images are buffered over the memory, sensor parameters like exposure time and acquisition time are not influenced by the chosen output data interfaces and their bandwidth. The actual image acquisition is then at the highest supported rate, i.e. 12.5MHz pixels/s. The actual exposure time is then expressed as a number of pixel lines, scanned at 12.5Mpixels/s.

The following image gathering scenarios are supported:

- Take N images (N=1..128 or infinite), spaced T seconds in time (T=0..32 seconds) and download them while acquiring. The image acquisition time depends on the available download bandwidth. The inter-image time T is defined as between the end of the previous download and the start of a new acquisition. No images are stored in memory. (READ_FRAMES and READ_HKFRAMES commands.)

- Take N images (N=1..128 or infinite), spaced T seconds in time (T=0..32s) and store them in memory. The image acquisition is at maximum rate (~12.5MHz). The acquisition process stops after N images have been taken, or when the memory is full. The download of the memory can only start after the acquisition of the required images. (STORE_HKFRAMES command.)

- The initiation of above procedures can be power-on , after an external trigger signal, or after a command, with a delay.

2.1.3 Camera with local buffer and compression engine

In this mode images are passed on to an external Image Compression ASIC (ICA) through a shared SDRAM frame memory. The ICA then compresses the images and re-writes them into said memory, where IRIS-3 can retrieve them for transmission over its output data interfaces, with or without CCSDS packetizing.

In addition the shared memory offers the end-user a means for controlling the ICA internal settings and operations, transparently through IRIS-3: part of the memory contains pass-through registers to the ICA. IRIS-3 provides commands to the user for directly writing this register area.

Another part of the memory contains image data descriptors through which IRIS-3 tells ICA where to find raw images, and through which ICA tells IRIS-3 where to find compressed images, and how compressed data are arranged.

IRIS-3 itself has no particular notion of the ICA compression device. A common data format is to be established to allow for the transport of image data between the two ASICs. From ICA's side, this format has to include all the parameters which are necessary to allow IRIS-3 to packetise compressed images complying to the CCSDS standard, i.e. size and location of compressed data objects.

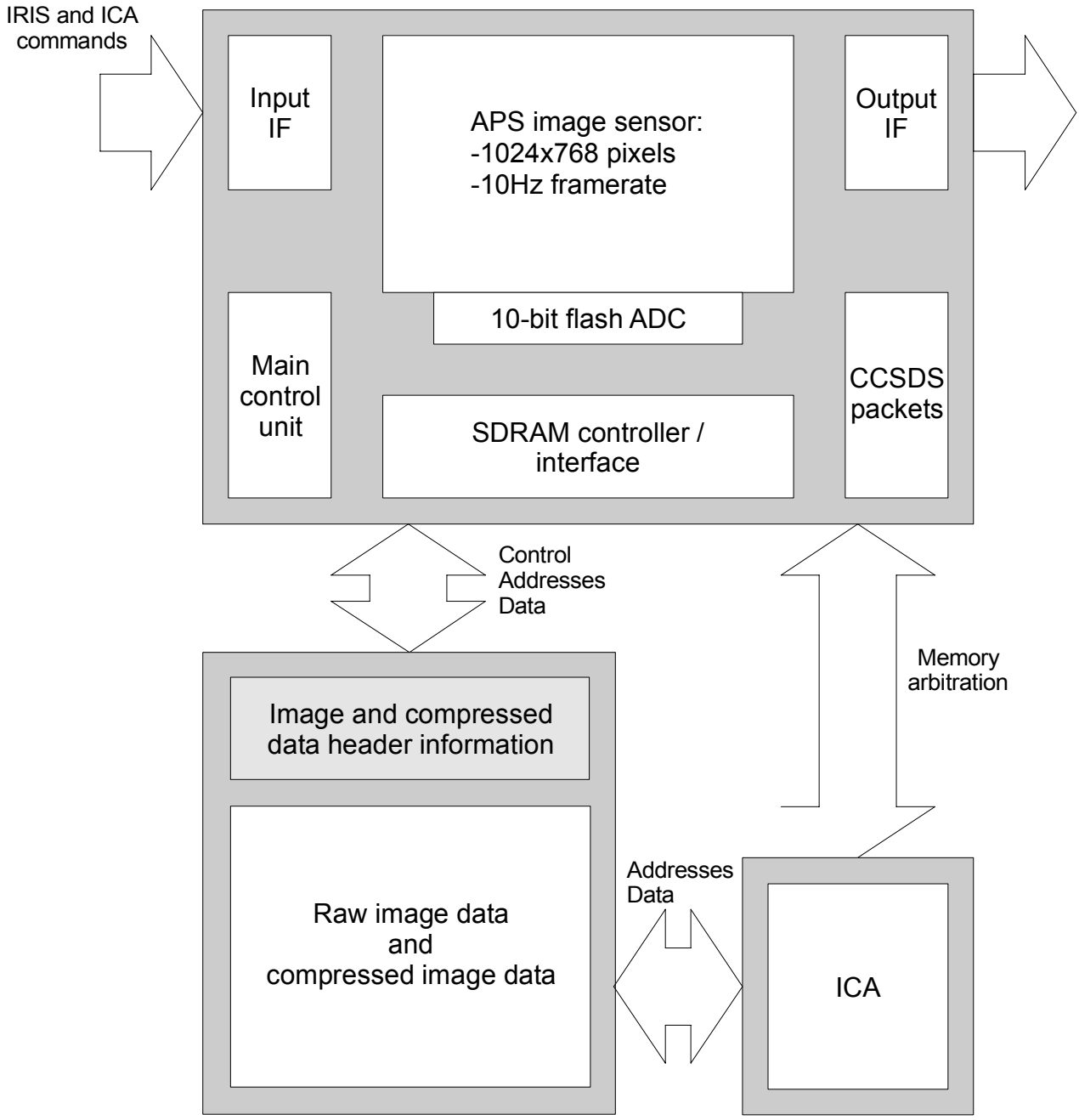


Figure 2.1 : Image Compression Camera: IRIS-3 with SDRAM buffer and ICA compression chip

The following image gathering scenarios are supported:

- Take N images (N=1..128 or infinite), spaced T seconds in time (T=0..32s) and download them while acquiring. The image acquisition time depends on the available download bandwidth. The inter-image time T is defined as between the end of the previous download and the start of a new acquisition. No images are stored in memory. (READ_FRAMES, READ_HKFRAMES.)

- Take N images (N=1..128 or infinite), spaced T seconds in time (T=0..32s) and store them in memory. The image acquisition is at maximum rate (~12.5MHz). The acquisition process stops after N images have been taken, or when the memory is full (only complete images are stored). The download of the memory can only start after the acquisition of the required images. (STORE_HKFRAMES.)

- Take N images (N=1..128 or infinite), spaced T seconds in time (T=0..32s) and store them in memory. Start compression of the images as soon as possible. Note: this scenario supports two more specific operational modes. The first mode gives a small number of images to be recorded, but at the highest acquisition rate, e.g. T=0, and the total amount of images is limited by the memory size and the raw image size. When T is larger than the compression time of an image, the scenario yields storage efficiency, limited by the amount of *compressed* images the memory can hold. (COMPRESS_HKFRAMES.)

- Take N images (N=1..128 or infinite), spaced T seconds in time (T=0..32s) and store them in memory. Start compression of the images as soon as possible. Download the images when all of them have been compressed. (COMPRESS_DOWNLOAD_HKFRAMES.)

- Take N images, spaced T seconds, store each image in memory, compress it, and download it, prior to acquiring the next new image. (COMPRESS_DOWNLOAD2_HKFRAMES.)

- The initiation of above procedures can be power-on, after an external trigger signal, or after a command, with a delay.

2.1.4 Chip I/O overview

Telecommand and telemetry standard compatibility	Defeatable	ESA PSS-04-106 and 04-107
Digital line drivers and receivers	No	Use off-chip drivers when required
Asynchronous serial command input		Low-speed RS-422-like
Synchronous serial command input		Medium-speed, PTD compatible
Synchronous serial command input		Low-speed, TTC-B-01 compatible
Synchronous parallel command input		High-speed, bus-compatible
Asynchronous serial data output		Medium-speed RS-422-like
Synchronous serial data output		Medium-speed, VCA compatible
Synchronous serial data output		Medium-speed, TTC-B-01
Synchronous parallel data output		High-speed, VCA/PRDC compatible
Simplified parallel data output		High-speed, frame grabber like, possibly compatible with digital video, e.g. for interfacing to ADV601 compression engine
Analogue output		With sample and hold and separate digital sync signals, compatible with external frame grabber
Memory interface		To SDRAM for image storage
Interface to compression engine		To IMEC/ICA, through memory
Analogue telemetry (TM) inputs	1	Telemetry input to local ADC, range to be confirmed
Digital telecontrol (TC) outputs	6	User-controllable digital outputs for telecontrol, number to be confirmed, depending on number of free package pins (probably multiplexed on other output pins)

Mode selectors	Yes	Hardwired input pins for selection of various operation modes and interface settings

2.2 Command and data interface specifications

2.2.1 Overview

IRIS-3 provides several types of interfaces for command and data communications from/to the spacecraft's data handling system (including standard components such as telecommand decoders, virtual channel assemblers, SMCSLite, FIFOs, compression engines, …)

- asynchronous serial command input (RS-422-like)
- synchronous serial command input (PTD and TTC-B-01 standards)
- synchronous parallel command input (bus-like)
- asynchronous serial data output (RS-422-like)
- synchronous serial data output (VCA and TTC-B-01 standards)
- synchronous parallel data output
- synchronous parallel data output (frame grabber-like)
- analogue data output (frame grabber-like)

All of these interfaces can be used to transport either raw data, or data packetised according to the CCSDS/ESA telecommand and telemetry transmission layer standards described in ESA PSS-04-106 and PSS-04-107.

Most of the electrical command and data interfaces described here are versions of interfaces already existing on the IRIS-2 and VMC systems, where applicable upgraded to reflect the higher system clock frequency of IRIS-3. Specific line drivers and receivers are not included. When an interface or application requires it, these components should be placed off-chip.

2.2.2 Interface configuration

The interfaces have to be configured by wiring external pins to a static logical 0 or 1 level. As interface pins are overloaded to accommodate multiple interface types, the use of some interface types is mutually exclusive. In addition, the semantics of pins may differ considerably from interface type to interface type.

The specified datarates are nominal and are only valid when the nominal system clock frequency of 25 MHz is used.

Command input interface type selection

CMD_IF[0..1]	
00	Synchronous serial (PTD)
01	Asynchronous serial
10	Synchronous serial (TTC-B-01, 16 bit)
11	Synchronous serial (TTC-B-01, 8 bit)

The assertion of the CMD_DIRECTb input pin, however, overrides above setting and allows to input a command via what is normally the imager's parallel data output bus.

Command input data rate selection

Four data rates can be selected. Their values are dependant on the type of interface chosen. When in this text reference is made to the currently selected command data rate, the symbol CMD_RATE* is used.

CMD_RATE[0..1]	
00	CMD_RATE1
01	CMD_RATE2
10	CMD_RATE3
11	CMD_RATE4

Data output interface type selection

DATA_IF[0..1]	
00	Synchronous serial (VCA)
01	Asynchronous serial
10	Synchronous parallel, digital frame grabber
11	Synchronous serial (TTC-B-01, wordlength same as CMD_IF when TTC-B-01, otherwise 16 bit)

Data output data rate selection

Four data rates can be selected. Their values are dependant on the type of interface chosen. When in this text reference is made to the currently selected data rate, the symbol DATA_RATE* is used.

DATA_RATE[0..1]	
00	DATA_RATE1
01	DATA_RATE2
10	DATA_RATE3
11	DATA_RATE4

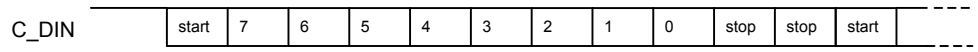
2.2.3 Asynchronous serial command input

2.2.3.1 Interface signals

signal name	**direction**	
C_DIN	in	Serial data input

These interface signals can be made compatible with the RS-232 and RS-422 standards by means of off-chip drivers and receivers.

2.2.3.2 Timing diagram



2.2.3.3 Data rates

CMD_RATE1	115200b/s
CMD_RATE2	38400b/s
CMD_RATE3	19200b/s
CMD_RATE4	9600b/s

2.2.3.4 Interface operation

The octet transfer protocol complies with the RS-422 standard, using one start bit, 8 data bits, no parity bit, and two stop bits:

Start Bit	8 Data Bits	2 Stop Bits
"0"	(LSB first)	"11"

All the octets of the command or command segment are to be transmitted contiguously, with their least significant bit (bit 7) first. Apart from the contiguity of octets, no packet delimiter is used.

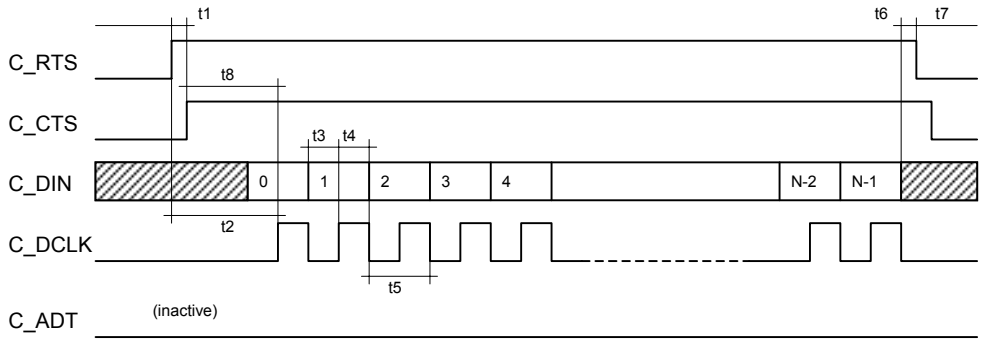
Note: The EIA-232 BREAK command, which pulls the line to ‘0’, is not applicable here to indicate an aborted transmission. Rather, the receiver detects breaks in TC segments when the line remains idle (‘1’) for longer than a period of 1 to 2 seconds.

2.2.4 Synchronous serial command input (PTD-style)

2.2.4.1 Interface signals

signal name	Direction	
C_RTS	In	Sender ready/telecommand segment valid
C_CTS	Out	Clear to send
C_DIN	In	Serial data input
C_DCLK	In	Serial data bit clock
C_ADT	In	Aborted data transfer indicator

2.2.4.2 Timing diagram



-	min	typ	max	comment
t1			40ns	
t2	125ns			
t3	50ns	80ns		

t4	50ns	80ns		
t5	160ns	160ns		
t6		250ns		
t7	1.4µs			time between packets
t8	125ns			

2.2.4.3 Data rates

The allowed input data rates span a range of DC up to $f_{CLK}/4$. With a clock of 25MHz, this is from 0 up to 6.25MHz.

2.2.4.4 Interface operation

This interface behaves like the serial MAP interface described in [RD1], pages 27-29.

Data transfer is initiated by the assertion of C_RTS. After the receiver responds by asserting C_CTS, the transmission of a stream of octets starts. A command (segment) is transmitted contiguously, octet by octet, and each octet is transmitted with its most significant bit (i.e. bit 0) first. The whole command (segment) counts N bits. C_DIN should be stable on the rising edges of C_DCLK. After a full segment or packet, C_RTS is de-asserted, followed by C_CTS.

Premature abortion of a command transfer is indicated by the assertion of C_ADT, followed by the de-assertion of C_RTS and then of C_ADT.

2.2.5 Synchronous serial command input (TTC-B-01-style, 16 bits)

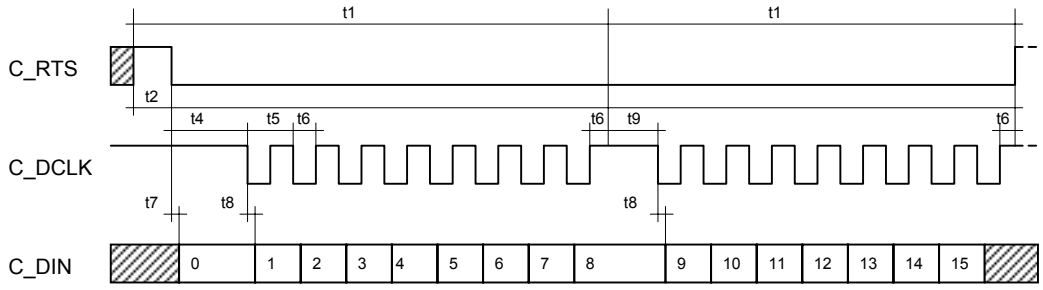
2.2.5.1 General description

The synchronous serial command input employs three signals and is fully compatible with the TTC-B-01 ML16 variant as described in [AD23], page 30. Note that the standard prescribes differential signals, while IRIS only offers single-ended inputs: external receivers and baluns are required.

2.2.5.2 Interface signals

Signal name	TTC-B-01 name	Direction	
C_RTS	MLS_P	In	Word valid sample signal, active low
C_DCLK	TFC_P	in	Bit transfer clock
C_DIN	MLD_P	in	Command data, 16 bits serial

2.2.5.3 Timing diagram



-	min	typ	max	comment
t1		-		
t2	240ns			

t4	240ns			
t5	240ns			
t6	t5/2			
t7	120ns			
t8	40ns			
t9	0ns			

2.2.5.4 Data rates

The interface is self-synchronising. The allowed input data rates span a range of 1kHz up to 4MHz, which is much wider than the actual rate of standard TTC-B-01. However, compliance to standard TTC-B-01 is at all times guaranteed.

2.2.5.5 Interface operation

See [AD23], page 30.

All the octets of the command/argument pairs or of a command segment are to be transmitted contiguously (16 bit transfers). Apart from the contiguity of octets/words, no packet delimiter is used. The input interface features a time-out which comes into play when any initiated command transfer stalls mid-word or in-segment and is not resumed within a time of 2 millisecond.

2.2.6 Synchronous serial command input (TTC-B-01-style, 8 bits)

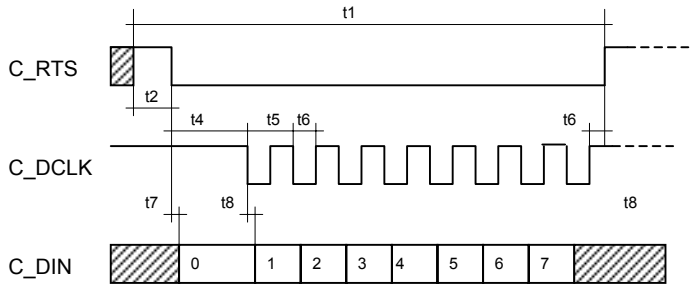
2.2.6.1 General description

The synchronous serial command input employs three signals and is compatible with the TTC-B-01 8-bit standard.

2.2.6.2 Interface signals

Signal name	TTC-B-01 name	Direction	
C_RTS	MLS_P	In	Word valid sample signal, active low
C_DCLK	TFC_P	in	Bit transfer clock
C_DIN	MLD_P	in	Command data, 16 bits serial

2.2.6.3 Timing diagram



-	min	typ	max	comment
t1	-			
t2	240ns			
t4	240ns			

t5	250ns			
t6	t5/2			
t7	120ns			
t8	40ns			
t9	0ns			

2.2.6.4 Data rates

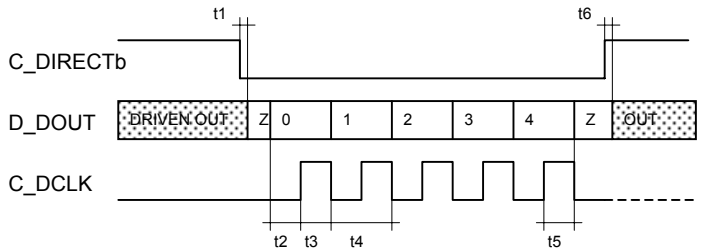
The interface is self-synchronising. The allowed input data rates span a range of 1kHz up to 4MHz, which is much wider than the actual rate of standard TTC-B-01. However, compliance to standard TTC-B-01 is at all times guaranteed.

2.2.6.5 Interface operation

The octets of command/argument pairs or of a command segment are transmitted individually (8 bit transfers). No packet delimiter is used. The input interface features a time-out which comes into play when any initiated command transfer stalls mid-octet, intra octest or in-segment and is not resumed within a time of 1 millisecond.

2.2.7 Synchronous parallel direct command input (bus)

2.2.7.1 Timing diagram



-	min	typ	max	comment
t1	80ns			
t2	0ns			setup time to C_DCLK
t3	50ns			
t4	130ns			
t5	80ns			hold time from C_DCLK
t6	40ns		80ns	

2.2.7.2 Interface operation

The imager's data output pins D_OUT[0..7] are tristated when C_DIRECTb is asserted, and the user can then write an 8-bit command word into the imager via the data output bus, strobed with the positive edge of the C_DCLK signal.

Any output packet in progress of being transmitted when this happens is aborted.

The direct parallel command input is intended for testing purposes and for interfacing to a microprocessor.

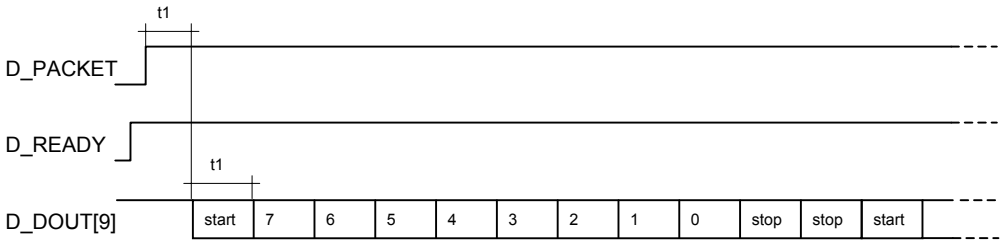
2.2.8 Asynchronous serial data output

2.2.8.1 Interface signals

Signal name	Direction	
D_PACKET	out	Like C_RTS, sender ready/telemetry packet valid
D_READY	in	Like C_CTS, receiver ready
D_DOUT[9]	out	Serial data output

These interface signals can be made compatible with the RS-232 and RS-422 standards by means of off-chip drivers and receivers.

2.2.8.2 Timing diagram



-	min	typ	max	comment
t1		T_d		±10%

2.2.8.3 Data rates

		Nominal data rate (f_{CLK}=25MHz)	Bit period T_d
DATA_RATE1	f_{CLK}	25Mb/s	40ns
DATA_RATE2	$f_{CLK}/2$	12.5Mb/s	80ns
DATA_RATE3	$f_{CLK}/8$	3.125Mb/s (VTS-speed)	320ns
DATA_RATE4	115200	115200b/s (PC-compatible)	8.68µs

2.2.8.4 Interface operation

The octet transfer protocol complies with the RS-422 standard, using one start bit, 8 data bits, no parity bit, and two stop bits:

Start Bit	8 Data Bits	2 Stop Bits
"0"	(LSB first)	"11"

With the receiver's D_READY at a high level, a packet transfer is initiated by the assertion of D_PACKET. After this, all the octets of the data packet are transmitted contiguously. D_PACKET remains asserted during this whole phase. D_PACKET is de-asserted after the last octet of the packet.

Abortion of a data transmission can be indicated by IRIS by de-asserting D_PACKET prematurely.

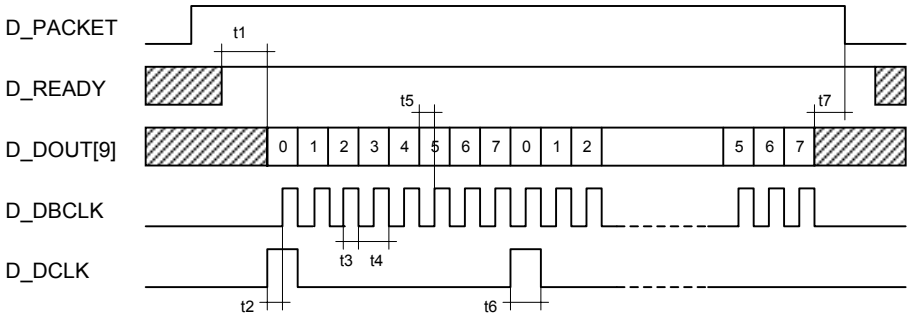
Flow control with D_READY is only allowed in modes where the IRIS sensor is not read directly. When D_READY is de-asserted, the presently being transmitted octet is finished, and IRIS halts the transmission until D_READY is re-asserted.

2.2.9 Synchronous serial data output (VCA-style)

2.2.9.1 Interface signals

Signal name	Direction	
D_PACKET	Out	Telemetry packet valid
D_READY	In	Receiver ready
D_DOUT[9]	Out	Serial data output
D_DBCLK	Out	Serial data bit clock
D_DCLK	Out	Word delimiter

2.2.9.2 Timing diagram



-	min	typ	max	comment
t1	40ns			
t2	20ns			
t3		$T_d/2$		
t4		T_d		

t5		$T_d/2$		
t6		40ns		
t7	80ns			

2.2.9.3 Data rates

		Nominal data rate (f_{CLK}=25MHz)	Bit period T_d
DATA_RATE1	f_{ECLK}	25Mb/s	40ns
DATA_RATE2	$f_{ECLK}/2$	12.5Mb/s	80ns
DATA_RATE3	$f_{ECLK}/4$	6.25Mb/s	160ns
DATA_RATE4	$f_{ECLK}/8$	3.125Mb/s	320ns

2.2.9.4 Interface operation

This interface is compatible with the serial input interface on the telemetry Virtual Channel Assembler, as described in [RD5], pages 12-14.

After and during assertion of D_PACKET, followed by D_READY sensed active, a data packet is output serially, octet by octet contiguously, and bit 0 first in each octet. Bits are synchronised to D_DBCLK, and should be sampled by the receiver on positive edges of D_DBCLK. D_DBCLK can go inactive at word boundaries for an indeterminate time.

Flow control with D_READY is only allowed in modes where the IRIS sensor is not read directly. If during a packet transmission D_READY is sampled low, the transmission halts until D_READY is sampled high again. The breaks in transmissions only happen on octet boundaries, i.e. between transmitted bit 7 and 8, or 15 and 16, and so on …

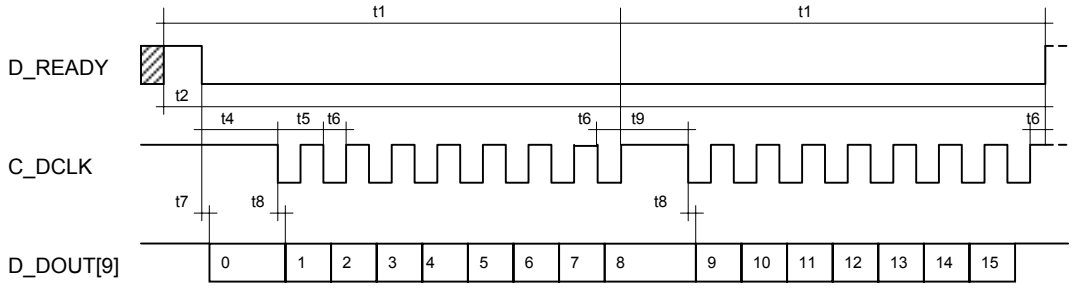
For each pixel transmitted, D_DCLK cycles high and low once, indicating the availability of a new pixel value on the analogue output A_OUT. This is of relevance should one use both the serial output and the analogue output simultaneously.

2.2.10 Synchronous serial data output (TTC-B-01-style, 16 bit)

2.2.10.1 Interface signals

Signal name	TTC-B-01 name	Direction	
D_READY	SDS_P	In	Word valid sample signal, active low
C_DCLK	TFC_P	in	Bit transfer clock
D_DOUT[9]	SDD_P	out	Data, 8 or 16 bits serial

2.2.10.2 Timing diagram



-	min	typ	max	comment
t1	-			
t2	240ns			
t4	240ns			
t5	240ns			

t6		t5/2		
t7	0ns			
t8		160ns		
t9	0ns			

2.2.10.3 Data rates

The interface is self-synchronising to the externally applied bit transmit clock TFC. The allowed TFC input clock rate spans a range of DC up to 4MHz, with a nominal duty cycle of 50%. This is a much wider range than the actual rate of standard TTC-B-01. However, compliance to standard TTC-B-01 is at all times guaranteed.

2.2.10.4 Idle pattern and implicit DOWNLOAD_HKFRAMES command

In case the TTC interface is used and no image data are available when the S/C's RTU interrogates the camera (activity on TFC and SDS), an idle pattern equal to 55AAh is output. This particular case happens when

- the camera has not yet acquired and buffered an image, e.g. after power-on, or
- the camera sensor is in progress of acquiring a new image.
- With direct sensor-to-spacecraft image download, during the line blanking intervals of the image acquisition.

Alternatively, when interrogation cycles are present, and when downloadable data are present on the system (i.e. the memory holds data and the system is not busy acquiring or compressing new images), the IRIS reacts as if a DOWNLOAD_HKFRAMES(128) command was received. I.e. activity on the TTC-B-01 interface can start a data download, even when no explicit download command was given.

2.2.10.5 No download abortion

Stalling of the RTU interrogation during an image download does not abort the download: it is resumed as soon as the RTU starts interrogating again. To explicitly abort a download, the end-user has to issue the RESET or STOP telecommand.

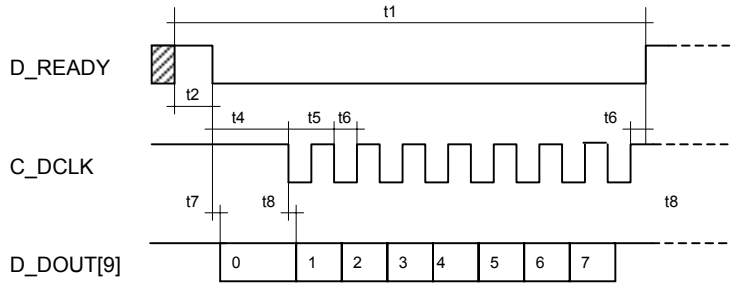
2.2.11 Synchronous serial data output (TTC-B-01-style, 8 bit)

2.2.11.1 Interface signals

Signal name	TTC-B-01 name	Direction	
D_READY	SDS_P	In	Word valid sample signal, active low
C_DCLK	TFC_P	in	Bit transfer clock

D_DOUT[9]	MLD_P	out	Data, 8 or 16 bits serial

2.2.11.2 Timing diagram



-	min	typ	max	comment
t1	-			
t2	240ns			
t3				
t4	240ns			
t5	240ns			
t6		t5/2		
t7	0ns			
t8		160ns		
t9	0ns			

2.2.11.3 Data rates

The interface is self-synchronising to the externally applied bit transmit clock TFC. The allowed TFC input clock rate spans a range of DC up to 4MHz, with a nominal duty cycle of 50%. This is a much wider range than the actual rate of standard TTC-B-01. However, compliance to standard TTC-B-01 is at all times guaranteed.

2.2.11.4 Idle pattern

In case the TTC interface is used and no image data are available when the S/C's RTU interrogates the camera (activity on TFC and SDS), an idle pattern equal to 55AAh, thus two 8-bit words long, is output. This particular case happens when

- the camera has not yet acquired and buffered an image, e.g. after power-on, or
- the camera sensor is in progress of acquiring a new image.
- With direct sensor-to-spacecraft image download, during the line blanking intervals of the image acquisition.

Alternatively, when interrogation cycles are present, and when downloadable data are present on the system (i.e. the memory holds data and the system is not busy acquiring or compressing new images), the IRIS reacts as if a DOWNLOAD_HKFRAMES(128) command was received. I.e. activity on the TTC-B-01 interface can start a data download, even when no explicit download command was given.

2.2.11.5 No download abortion

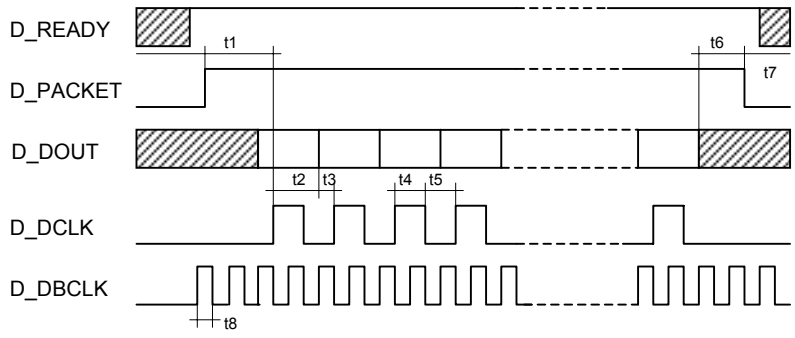
Stalling of the RTU interrogation during an image download does not abort the download: it is resumed as soon as the RTU starts interrogating again. To explicitly abort a download, the end-user has to issue the RESET or STOP telecommand.

2.2.12 Synchronous parallel data output

2.2.12.1 Interface signals

signal name	Direction	
D_PACKET	Out	Telemetry packet valid
D_PACKETb	Out	Inverted D_PACKET
D_READY	In	Receiver ready
D_DOUT[0..9]	Out	Parallel data output
D_DCLK	Out	Parallel data word clock
D_DCLKb	Out	Inverted D_DCLK
D_DBCLK	Out	Fast clock

2.2.12.2 Timing diagram



-	min	typ	max	comment
t1	40ns			
t2	60ns			
t3	20ns	$T_d/4$		
t4		$T_d/2$		
t5	40ns	$T_d/2$		
t6	40ns			
t7	320ns			time between packets
t8	20ns	$T_d/4$		

2.2.12.3 Data rates

		Nominal data rate (f_{CLK}=25MHz)	Word period T_d
DATA_RATE1	$f_{CLK\_XRD\_MAX}$	12.5MW/s	80ns
DATA_RATE2	$f_{CLK\_XRD\_MAX}/2$	6,25MW/s	160ns
DATA_RATE3	$f_{CLK\_XRD\_MAX}/4$	3.125MW/s	320ns
DATA_RATE4	$f_{CLK\_XRD\_MAX}/8$	1.5MW/s	640ns

2.2.12.4 Interface operation

This interface is compatible with the parallel input interface on the telemetry Virtual Channel Assembler, as described in [RD5], pages 10-12. The interface is also compatible with the TEMIC PRDC packetising RICE compression chip [RD4], and with TEMIC M67200-series FIFOs and IDT IDT7200-series FIFOs. It will be attempted to obtain compatibility with an existing IEEE-1355 bridge chip as well.

Transmission of a data packet occurs after D_READY has been sampled high, followed by the assertion of D_PACKET. Data words are transferred synchronously to D_DCLK and D_DCLKb, and can be sampled by the receiver on rising edges or during the high states of D_DCLK, and vice versa for D_DCLKb. During transmission, D_DCLK can go inactive for an indeterminate time. D_DBCLK is an internal clock to which all interface signals are synchronised and which is to be used as an interface clock for the PRDC.

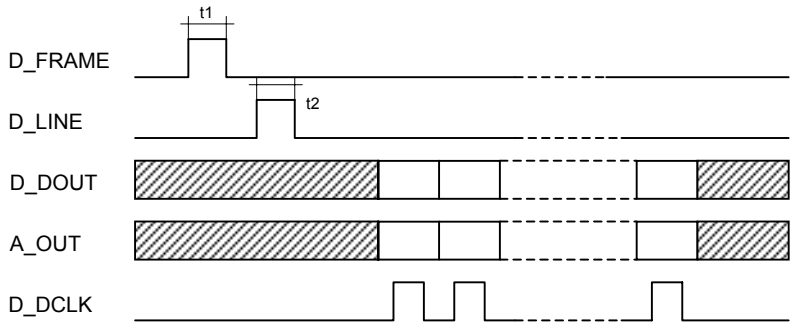
Flow control with D_READY is only allowed in modes where the IRIS sensor is not read directly. When within a packet D_READY is sampled low, the output interface halts until D_READY is sampled high again.

2.2.13 Digital frame grabber data output

2.2.13.1 Interface signals

Signal name	Direction	
D_DOUT[0..9]	Out	Parallel data output
D_DCLK	Out	Parallel data word clock
D_FRAME	Out	New frame indicator
D_LINE	Out	New line indicator

2.2.13.2 Timing diagram



-	min	typ	max	comment
t1	80ns			
t2	80ns			

2.2.13.3 Data rates

		Nominal data rate (f_{CLK}=25MHz)
DATA_RATE1	$f_{CLK\_XRD\_MAX}$	12.5MW/s
DATA_RATE2	$f_{CLK\_XRD\_MAX}$/2	6.25MW/s
DATA_RATE3	$f_{CLK\_XRD\_MAX}$/4	3.125MW/s
DATA_RATE4	$f_{CLK\_XRD\_MAX}$/8	1.5MW/s

2.2.13.4 Interface operation

Raw data words are output on D[0..9], synchronous to D_DCLK and D_DCLKb. These data can be sampled on a positive edge or during a high state of D_DCLK, and vice versa for D_DCLKb. Frames and lines are indicated by the assertion of D_FRAME and D_LINE, respectively.

2.2.14 Analogue frame grabber data output

2.2.14.1 Interface signals

Signal name	Direction	
A_OUT	Out	analogue pixel output, 2 to 4 V
D_DCLK	Out	pixel clock
D_FRAME	Out	new frame indicator
D_LINE	Out	new line indicator

2.2.14.2 Timing diagram

See digital frame grabber output .

2.2.14.3 Pixel rates (maximum)

See Digital Frame Grabber output.

2.2.14.4 Interface operation

The output of the internal analogue multiplexer is always present at pin A_POUT. This signal can be sampled on a positive edge or during a high state of D_DCLK, and vice versa for D_DCLKb. Frames and lines are indicated by D_FRAME and D_LINE, respectively.

A_OUT offers a DC-coupled voltage, range 2 to 4 V (TBC), from a low source impedance.

2.3 Telecontrol and telemetry ports

One external input to the on-chip ADC is provided. This analogue input can be used for telemetry. Six user-controllable digital outputs are provided. These can be put to use for telecontrol local to the camera site, e.g. control of a camera pointing motor or of a protective lens hood.

2.4 Shared SDRAM interface

IRIS-3 can control an optional external SDRAM, acting as a master, sharing the memory with an optional slave component. As master, IRIS-3 takes care of all necessary actions to maintain memory integrity, such as periodic refresh cycles.

Two memory configurations are available:

- 8-bit wide data words, without EDAC.
- 16-bit wide, configured as 10 data bits (payload), 4 EDAC bits, and 2 unused bits, yielding per word a capability to detect two bit errors, and to correct one bit error.

When a slave component is connected to the memory, it has access to the SDRAM by default. However, whenever IRIS-3 signals that it requires access, the slave has to finish its current operation with the SDRAM and release it to IRIS-3.

2.4.1 Supported types and configurations

The specific type of SDRAM supported is equivalent to a common-denominator industry standard, as implemented in e.g.:

- the Hitachi HM5225805B 256 Megabit chip ([RD1])
- the NEC mPD45256841 256 Megabit chip ([RD2])
- the Micron MT48LC32M8A2 256 Megabit chip ([RD3])
- the Samsung K4S560832A 256 Megabit chip, allowing for compatibility with the 3D-Plus 3DSD2048-163 module (to be confirmed)([RD4])

While small differences exist in options and features of such SDRAM components, only functionality which is common to a larger group of devices will be used. The maximum amount of memory supported will be 64 megawords, which is sufficient for about 60 uncompressed images.

During image acquisition, with IRIS-3 writing the buffer, the maximum throughput to the SDRAM is 12.5 megapixels/s. During acquisition, the buffer can not be accessed by a slave.

Four memory size/EDAC configurations are possible:

- 32Mwords of 8 bits: using 1 8-Mword×8-bit×4-bank memory chip
- 32Mwords of 16 bits: using 2 8-Mword×8-bit×4-bank memory chips, each handling half of the data bus, and both sharing all control lines
- 64Mwords of 8 bits: using 2 8-Mword×8-bit×4-bank memory chips, both on RAM_D[0..7], sharing all controls, with the exception of the RAM_CS0b and RAM_CS1b lines, which differentiate between both chips.
- 64Mwords of 16 bits: using 4 8-Mword×8-bit×4-bank memory chips, two banks of 16b width (see configuration 1) on RAM_D[0..15], sharing all controls, with the exception of the RAM_CS0b and RAM_CS1b lines, which differentiate between both banks of each two chips.

The configurations are set with pin straps:

Settings pins	Value	Configuration
MEM_CFG[0..1]	00	8-bit, 32MB
	01	8-bit, 64MB
	10	16-bit, EDAC, 32MW
	11	16-bit, EDAC, 64MW

SRAM memory is not explicitly supported. However, it is possible to use SRAM, provided external components are present to translate between the native SDRAM addressing anf driven signals and standard SRAM signals. Smaller memory sizes than the

minimum of 32MB settable with MEM_CGF can be used, provided the end-user keeps track of memory allocation, avoiding by proper choice of commands that inexistent addresses are not accessed by the IRIS-3. This effectively precludes the use of IRIS3 in autonomous mode with smaller memories.

2.4.2 Interface signals

Signal name	Direction	
RAM_CLK	I/O	System clock as fed to SDRAM, connect with 50kΩ to ground
RAM_CS0b	I/O	Enable RAM chip 0, disables or enables SDRAM device operation by masking, enabling all inputs except RAM_CLK, RAM_CKE, and RAM_DQM, 50kΩ to power
RAM_CS1b	I/O	Enable RAM chip 1, disables or enables SDRAM device operation by masking, enabling all inputs except RAM_CLK, RAM_CKE, and RAM_DQM, 50kΩ to power
RAM_CKE	I/O	Masks RAM_CLK clock to freeze operation from the next clock cycle on. RAM_CKE should be enabled at least one cycle prior to new SDRAM command.
RAM_A[12..0]	I/O	Row address RA[12..0], column address CA[9..0] ([0] is LSB)
RAM_BA[1..0]	I/O	Bank address: selects bank to be activated during row address latch time, and selects bank for read/write during column address latch time.
RAM_RASb	I/O	Row address strobe: latches row addresses on the positive going edge of RAM_CLK with RASb low; enables row access and precharge
RAM_CASb	I/O	Column address strobe: latches column addresses on the positive going edge of RAM_CLK with CASb low, enables column address.
RAM_WEb	I/O	Enables write operation and row precharge; latches data in starting from CASb, WEb active

RAM_DQM	I/O	Data input/output mask: makes data output hi-Z, t_{SHZ} after the clock and masks the output; blocks data input when DQM active.
RAM_D[15..0]	I/O	Data from/to SDRAM bank, distributed over two 8 bit blocks ([0] is LSB). When only one block is installed (see MEM_CFG) only RAM_D[7..0] is used.
RAM_GRANT	O	RAM access granted to slave device
RAM_SLAVERDY	I	Slave currently not accessing RAM, 50k pull-up to VDD.

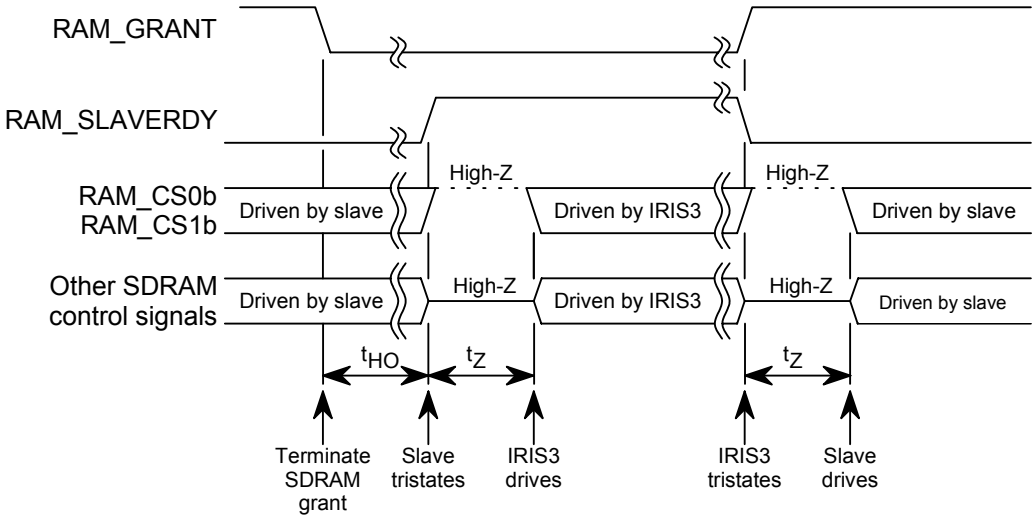
All SDRAM signals, except RAM_GRANT and RAM_SLAVERDY, are synchronous to the rising edge of RAM_CLK. In case of IRIS-3, RAM_CLK is half of the system's clock frequency, and all of the other RAM_ signals are timed so that they can be sampled on a positive edge of RAM_CLK.

Note: contrary to the conventions used elsewhere in this document, bit vector indices for the SDRAM signals are given from HIGH to LOW, with LOW denoting the least significant bits in the vector. This to avoid potential mistakes when interfacing to industrial components which do not follow the ESA conventions.

2.4.3 SDRAM hand-over sequence (IRIS->Slave, Slave->IRIS)

By default, the slave has access to the SDRAM. If IRIS3 needs access to the memory, the RAM_GRANT signal is de-asserted. The slave must assert the RAM_SLAVERDY within 50µs. When the memory is handed over to or from the slave all banks are expected to be precharged and idle. The device which controls the SDRAM provides all signals to the SDRAM, including the clock signal, while the other device tristates all of its SDRAM control signals. During the hand-over intervals the SDRAM control bus is kept from floating by suitable pull-up and pull-down resistors.

IRIS3 generates the necessary refresh cycles and shall interrupt the slave whenever needed to do so. The hand-over sequence is displayed below:



2.4.4 SDRAM timing

Symbol	Min	Typ	Max	Units	Remarks
t_{PU}	200	-	-	ns	
t_{RP}	20	-	-	ns	
t_{RFC}	70	-	-	ns	

t_{MRD}	3 x t_{CK}	-	-		
t_{CK}	-	40	-	ns	80 ns with IRIS3
t_{WR}	15	-	-	ns	
t_{RAS}	44	-	120000	ns	
t_{XRS}	75	-	-	ns	
t_{HO}	-	-	50	µs	
t_Z	160	-	240	ns	

2.4.5 Address mapping rules

For the remainder of this document, the physical memory space of the two memory stacks, each with one or two chips, each with four banks, will be translated into a two-dimensional address space (line,column) according to these rules:

- Line address = RAM_CS0b & RAM_BA[1..0] & RA[12..0], ranged 0 to 65535
- Column address = CA[9..0], ranged 0..1023
- RAM_CS1b = not(RAM_CS0b)

2.4.6 EDAC scheme

The EDAC scheme used is an additional Hamming code of 4 bits attached to a 10 bits data word, which allows correction of 1 bit error. The total of 14 bits is expanded to 16 bits by filler zeroes. Data are checked and corrected whenever they are read from the memory, prior to any other use.

2.4.6.1 EDAC encoding algorithm

```
subtype Word10Tp is std_logic_vector(9 downto 0);
subtype Word16Tp is std_logic_vector(15 downto 0);

function WriteEdac10(D: in Word10Tp)
  return Word16Tp is

  variable P1,P2,P3,P4: std_logic; --parity bits
  variable RESULT:     std_logic_vector(15 downto 0);
  variable D:          std_logic_vector(9 downto 0);

begin
  --
  --takes a 10 bit word in, and returns
  --a 16 bit word ordered as follows
  --IN_WORD&PAR_BITS&"00";
  --with PAR_BITS the corresponding Hamming protection bits
  --

  P4 := D(9) xor D(8) xor D(6) xor D(5) xor D(3) xor D(1);
  P3 := D(9) xor D(7) xor D(6) xor D(4) xor D(3) xor D(0);
  P2 := D(8) xor D(7) xor D(6) xor D(2) xor D(1) xor D(0);
  P1 := D(5) xor D(4) xor D(3) xor D(2) xor D(1) xor D(0);

  RESULT := D&P1&P2&P3&P4&"00";

  return(RESULT);

end WriteEdac10;
```

2.4.6.2 EDAC decoding/correction algorithm

```
function ReadEdac10(DS: in Word16Tp)
   return Word10Tp is

   variable P:  std_logic_vector(1 to 4); --local parities
   variable PS: std_logic_vector(1 to 4); --stored parities
   variable D:  std_logic_vector(9 downto 0);              --data
   variable DR: std_logic_vector(1 to 14);--re-ordered vector
   variable SYN: std_logic_vector(1 to 4);

  begin
```

```
--extract stored data
D := DS(15 downto 6); --extract stored data
PS := DS(5 downto 2); --extract stored parities

--calculate new parity bits
P(4) := D(9) xor D(8) xor D(6) xor D(5) xor D(3) xor D(1);
P(3) := D(9) xor D(7) xor D(6) xor D(4) xor D(3) xor D(0);
P(2) := D(8) xor D(7) xor D(6) xor D(2) xor D(1) xor D(0);
P(1) := D(5) xor D(4) xor D(3) xor D(2) xor D(1) xor D(0);

--calculate syndrome
SYN := P xor PS; --local versus stored parities

--re-order word for syndrome count
DR := PS(1)&PS(2)
     &D(9)
     &PS(3)
     &D(8 downto 6)
     &PS(4)
     &D(5 downto 0);

--determine error type
if (SYN="0000") then –no error(s) exist(s)
  --do nothing!
Else –error(s) exist(s)
  for I in 1 to 14 loop
    if (conv_integer("0"&SYN)=I) then –error in position I!
      DR(I) := not(DR(I));
    end if; --SYN,I
  end loop;
end if; --SYN

--re-assemble output word
D := DR(3)&DR(5 to 6)&DR(9 to 14);
return(D);

end ReadEdac10;
```

2.4.7 Memory data word alignment

"PAYLOAD_DATA[0..9]" indicates the user data stored in the SDRAM, noted in ESA-index format (low to high). User data can be pixels, compressed data from ICA, telemetry data, and IRIS3's own memory management tables.

"RAM_D[15..0]" indicates the data on the SDRAM's bus, in industry-standard index format (high to low).

"P[0..3]" indicates 4 error-correction EDAC bits.

16 bit memory

RAM_D[15..0] = PAYLOAD_DATA[0..9]&P[0..3]&"00"

8 bit memory

RAM_D[7..0] = PAYLOAD_DATA[0..7]

RAM_D[15..8] = not used.

2.4.8 Anticipating memory uploads

Commands to IRIS may include uploading data directly to the attached SDRAM. Whenever a command packet is received,. IRIS grabs access to the SDRAM to anticipate any such uploads.

2.4.9 SDRAM low power mode

IRIS3 itself does not implement the low power idle mode of the SDRAMs. As at idle time the control of the SDRAMs is with the slave device, it is the slave that should implement low-power modes when required.

2.5 Interfacing with the ICA image compression engine

2.5.1 Memory organisation

2.5.1.1 Memory map

Memory addresses (ranges) are specified in this document as (line, word) or (line range, word range). One line contains 1024 words (8 bits or 16 bits), and the memory can be configured as 32768 lines or 65536 lines.

The shared memory buffer always is partitioned into five sections, each with its own specific task:

Address range (lines, bytes or words)	Area name	Contents
(0, 0-1023)	ICA Command Area	Command and status registers for IRIS-ICA communication and control. 8-bit bytes plus optional EDAC.
(1-495, 0-1023)	ICA Parameter Area	End-user parameters for ICA operation. These are transparently uploaded through IRIS-3 to the SDRAM. Note that this space is not a mirror of internal ICA registers: it is merely a way of passing information to the ICA. Also memory pool for uploading ICA microcode. 507904 bytes in total. 8-bit bytes plus optional EDAC.
(496-511, 0-1023)	Image Data Location Table	Descriptor records for up to 512 images, each record holding up to 32 bytes, residing at a fixed location in memory. Records also hold system housekeeping data, attached to the image the record belongs to. Accesses to the location table must be atomic. 16384 bytes in total. 8-bit bytes plus optional EDAC.
(512-2559, 0-1023)	ICA Scratch Area	Work space for ICA, used for the assembly of

		compressed image data. 2097152 bytes in total. 8-bit bytes plus optional EDAC.
2560-32767, 0-1023) or (25604-65535, 0-1023)	Image Buffer	Raw and/or compressed image data, aligned at boundaries of 1024 words. 8-bit words without EDAC, optionally 8-bit words or 10-bit words with EDAC.

2.5.1.2 IRIS-ICA command passing area

Address range	Register name	Contents	Written by	Read by
(0,0)	ICACommand[0..7]	IRIS command to ICA	IRIS, ICA	ICA, IRIS
(0,1-2)	FirstToCompress[0..15] (note: high byte stored at (0,1), low byte stored at (0,2))	Number of first image in a stream to compress (only 9 LSB valid)	IRIS	ICA
(0,3-4)	NtoCompress[0..15] (note: high byte stored at (0,3), low byte stored at (0,4))	Number of images to compress (only 9 LSB valid)	IRIS	ICA

ICA examines the command register immediately each time IRIS actively grants access to the SDRAM to ICA, i.e. by ICA detecting a rising edge on RAM_GRANT. ICA shall not return the memory bus to IRIS before ICA has read the command and parameter space.

Likewise, IRIS shall update the command and parameter space each time before granting the memory to ICA.

A typical command phase is then:

- IRIS writes a new command and its parameters
- IRIS grants memory access to ICA
- ICA examines the new command and parameters

- ICA executes the command
- whenever IRIS gets memory access back, the command is reduced to NOP
- ICA ends the command execution
- whenever ICA gets access to the memory, it writes END in the command area
- ...

Joint IRIS-ICA command executions can only end when the command terminates completely, or when it is aborted by the reception of a STOP or RESET command at IRIS, which is communicated forth to ICA.

As long as a previous command has not terminated, IRIS shall not initiate a new image-related command phase with ICA.

2.5.1.3 ICA parameter area

The approx. 0.5 megabyte memory area at lines 1-511 is used for passing end-user parameters to the ICA, as well as ICA microcode programs. This area can be written with the memory write commands described in section 2.6.11.

2.5.1.4 Image location table

The image location table contains descriptors, IRIS housekeeping data, and optional additional ICA data, related to 512 (possible) raw or compressed images, stored in the image buffer. These images and their location descriptors are numbered 0 to 511.

The image location table is contained in address range 496x1024 to 511x1024+1023. The table exists of 8-bit words. When 16-bit memory is installed, the additional 8 bits available are only to be used for the EDAC scheme: the other bits are to be written ‘0’.

The record for image number N is located on address (496+N/32)x1024+Nmod32x32 in the location table.

Each record is structured as follows:

Base address	Address	object name	size	meaning	read by	written

	extension					by
(496+N/32, 32(Nmod32))	+0	ImageID[0..7]	8b	Image identifier	IRIS, ICA	IRIS
	+1	ImageID[8..11]	4b	Image identifier	IRIS, ICA	IRIS
		ImageIDMod	1b	Identifier modifier	IRIS, ICA	IRIS, ICA
		Written	1b	Written tag	IRIS, ICA	IRIS
		Compressed	1b	Compressed tag	IRIS	ICA
		-	1b	-		
	+2	StartAddress	16b	Memory line where raw or compressed image begins	IRIS, ICA	IRIS ICA
	+4	“00000”&Nlines	16b	Number of image lines of raw image; number of memory lines of compressed image	IRIS, ICA	IRIS, ICA
	+6	“00000”&LineLength	16b	number of pixels per line of raw image; 1024 for compressed image	IRIS, ICA	IRIS, ICA
	+8	X1			IRIS	IRIS
	+9	Y1			IRIS	IRIS
	+10	X2			IRIS	IRIS
	+11	Y2			IRIS	IRIS
	+12	“0000”&XS&YS			IRIS	IRIS
	+13	Exp[0..7]			IRIS	IRIS
	+14	Threshold			IRIS	IRIS
	+15	Gain			IRIS	IRIS

	+16	ControlOut			IRIS	IRIS
	+17	ErrorState			IRIS	IRIS
	+18	Mode[0..7]			IRIS	IRIS
	+19	Mode[8..15]			IRIS	IRIS
	+20	Period			IRIS	IRIS
	+21	AIN1[0..7]			IRIS	IRIS
	+22	AIN1[8..9]&"000000"			IRIS	IRIS
	+23	NextToWrite[0..7]			IRIS	IRIS
	+24	NextToWrite[8]&NextTo Donwload[8]&"000000"			IRIS	IRIS
	+25	NextToDownload[0..7]			IRIS	IRIS

ImageID is a 12-bit cyclic counter which is updated by IRIS for each image acquired. ImageIDMod is an extension bit for ImageID which can be set by ICA alone, upon completion of compression of said image.

The values of registers such as X1, Y1, Mode, … and of the analogue telemetry inputAIN1 are written into the image location table at the time the attached image is captured by IRIS-3.

Throughout this text, the above record format will be referred to as the TableRecordType. When an object N is declared to point to this type (i.e. N is of type &TableRecordType), N is an integer, pointing to the table record number N, residing at address (496x+N/32)x1024+32xNdiv32. The aggregate elements of N are then referred to as N.M, e.g. N.StartAddress.

2.5.1.5 Image data storage format

Raw and compressed image data are stored contiguously in the memory pool. The total size of an image is always aligned to the next memory line (one memory line comprises 1024 words), by the addition of padding zeroes. Of course, raw images sized 1024 pixels x768 lines, 1024x512, 512x512, etc. will never give rise to padding. It is recommended to only use such image formats.

2.5.2 Communications between IRIS-3 and ICA

All communication between IRIS-3 and ICA is through the shared memory.

2.5.2.1 Memory arbitration mechanism

IRIS-3 is always the active master of the shared memory. Whenever IRIS-3 does not need access to the memory, i.e. for data transfers, for memory configuration, or for refresh, the RAM_GRANT line is asserted. When RAM_GRANT is asserted, IRIS-3 disables all its memory lines (tristate) and a slave device can freely control the memory, using its own memory control signals. When the slave actively is using the memory, it has to de-assert the RAM_SLAVERDY input line to IRIS-3 and keep it de-asserted during use.

When IRIS-3 needs access to the memory, it de-asserts RAM_GRANT. The slave must respond to this with asserting RAM_SLAVERDY as soon as this is fit, but never later than 50μs. At the same time, the slave must tristate all of its memory control lines. When IRIS-3 sees RAM_SLAVERDY asserted, it effectively grabs control of the memory by actively driving its memory control lines.

Note that the slave, when accessing the memory, is fully responsible for properly configuring the SDRAMs, with the exception of refresh. Refresh control resides fully with IRIS-3. For this reason IRIS-3 shall take control of the memory whenever the refresh cycle demands this.

Passing on commands from IRIS-3 to ICA goes via a dedicated area in the memory that holds images of a command/status register and parameter registers. ICA has to examine these registers each time RAM_GRANT is asserted. Likewise, IRIS-3 examines the registers each time memory access for ICA is revoked. This mechanism yields an

effective way of signalling from IRIS to ICA that new parameters have been loaded, and vice versa.

2.5.2.2 Passing commands from IRIS-3 to ICA

The top-two bits of ICACommand always indicate the type of memory used, reflecting the settings at the MEM_CFG pins:

ICACommand[0..1] <= MEM_CFG[0..1]

The following commands are defined for the lower bits of ICACommand:

name	ICACommand[2..7]	description
NOP	"000000"	no operation
ATTN	"000001"	Attention: ICA parameter area has been written to by IRIS
COMP	"000010"	Compress: start compression now
STOP	"000011"	Stop: stop immediately, abort a running operation in a clean way, and return to initial state
END	"000100"	written by ICA: ICA has finished its present job

Whenever the end-user writes to the ICA parameter area through IRIS (with the WRITE_MEM command), IRIS passes the ATTN command to ICA after the memory write cycle.

Whenever IRIS has a compression job for ICA, IRIS passes the COMP command to ICA as soon as compression is allowed to start.

Whenever IRIS asserts the RAM_GRANT line, ICA is to examine the ICACommand, FirstToCompress and NtoCompress words in memory. When COMP is set, compression will start according to section 2.5.2.3. When ATTN is set, ICA shall read the new parameters from memory. When STOP is set, ICA shall return to a state where it can safely and correctly accept a COMP command, leaving the memory and the image descriptor records in a correct state. IRIS shall set a STOP before setting a COMP.

After ICA has completely finished the requested action, i.e. compression or parameter update, ICA shall write the value END back to the ICACommand word, indicating that ICA is idle. Through this means IRIS shall always keep track of ICA's internal state. When a new command arrives at IRIS leading to a new compression job for ICA, while ICA is still busy, IRIS shall buffer this command and its parameters, until ICA can start the new job. This command buffer has a depth of one command. The buffer will be written-over if another new command arrives, implying the complete loss of the former pending command.

2.5.2.3 Image data access protocols

The now-following pseudo-code defines how raw and compressed images are to be stored into and retrieved from the shared SDRAM memory pool, and how the data location table is updated during this process.

IRIS-3: Storing raw images (for compression)

Assumptions and rules:

- ICA is idling at the start of the command execution.
- There is no conceptual difference between storage for compression and storage of raw images for future download.
- When the image stream is non-ending the procedure is repeated until the memory bounds are reached. Only complete images reside in memory.
- The start position in memory stems from the system's prior history.

Declarations:

NextToWrite: &TableRecordType;

Initialisations (command start time):

determine **NextToWrite from internal memory management**
(get SDRAM access)
(ICACommand <= STOP;)
(grant SDRAM access to ICA)
(wait a TBD time)
(get SDRAM access)
(FirstToCOmpress <= NextToWrite;)
(NToCompress <= (from command);)
(ICACommand <= COMP;)

Operations:

loop over the images to store

write image from NextToWrite.StartAddress on;

OldAddress <= NextToWrite.StartAddress;
NextToWrite.Nlines <= size of this image expressed in lines;
NextToWrite.LineLength <= size of image line expressed in pixels;
NextToWrite.Written <= '1';
NextToWrite.Compressed <= '0';
NextToWrite.Image ID <= ID of this image;
NextToWrite.ImageIDMod <= '0';

wait for trigger to store new image;

if (NextToWrite.Compressed='1') then
--ICA already compressed the previously-written image,
--so we can re-use part of its memory space!!!
DataSize <= NextToWrite.Nlines; --as modified by ICA
else
--append to previous image
DataSize <= size of new raw image expressed in memory lines;
end if;
NextToWrite++;
NextToWrite.StartAddress <= OldAddress+DataSize;

end loop;

IRIS-3: downloading images (raw or compressed)

Declarations:

```
NextToDownload: &TableRecordType;
```

Operations:

```
for all images to download loop

    configure CCSDS headers;
    download data block at NextToDownload.StartAddress;
    NextToDownload.Written <= '0';
    NextToDownload.Compressed <= '0';
    NextToDownload++;

end loop;
```

ICA: compressing and re-writing images

Assumptions and rules:

- compressed images always overwrite their source image in the memory pool, to assure storage efficiency.
- ICA has access to the image location table, at least once for each image to compress.
- When NtoCompress = 128 the procedure is repeated until the memory bounds are reached. Only complete images reside in memory.

```
Declarations:

        FirstToCompress: &TableRecordType;
        NextToCompress: &TableRecordType;
        NumberToCompress: integer range 0 to 128;

Initialisations:

Operations:
        if (ICACommand = COMP) then

                get FirstToCompress, NumberToCompress from IRIS;

                for NextToCompress
                        in FirstToCompress .. FirstToCompress+NumberToCompress-1 loop

                        wait until (NextToCompress.Written='1');

                        compress image at NextToCompress.StartAddress;

                        move compressed data to NextToCompress.StartAddress;

                        NextToCompress.Nlines <= size of compressed data in memory lines;
                        NextToCompress.LineLength <= 1024;

                        NextToCompress.Compressed <= '1';

                end loop;

                ICACommand <= END;
        end if;
```

Handling of memory bounds

Before writing an image to memory, IRIS verifies that it will fit. If the memory is completely full, or when no new descriptor numbers are available, the command that caused the image acquisition is prematurely ended, terminates properly, and a flag in the ErrorState register is set. Any further image acquisitions demanded by said command are cancelled.

2.6 Commanding IRIS

2.6.1 Internal states and variables

IRIS holds the following variables in internal registers. These variables can be controlled and/or observed by the user by means of commands. The table also lists the default values the variables assume after power-on or reset.

Parameter or internal setting name	allowed range of values	reset value	description
X1	integer {0,8,…1016}	See CONFIG	start X coordinate of current/next frame, in steps of 8
Y1	integer {0,8,…1016} (or …760)	See CONFIG	start Y coordinate of current/next frame, in steps of 8
X2	integer {7,15,…1023}	See CONFIG	end X coordinate of current/next frame, in steps of 8
Y2	integer {7,15,…1023} (or ..767)	See CONFIG	end Y coordinate of current/next frame, in steps of 8
XS	integer {1,2,4,8}	1	subsampling X-increment
YS	integer {1,2,4,8}	1	subsampling Y-increment
Exposure	integer {1,3,…,767}	See EXP	integration time expressed in lines or frames
Threshold	integer {0,4,8,..,1016}	512	pixel threshold value for illumination control, in steps of 4
Gains	bit vector[0..7]	“00000101”	analogue output stage voltage gain for pixel array
ControlOut	bit vector[0..7]	“00000000”	remote control output settings
ErrorState	bit vector[0..7]	“00000000”	error log
Timer	integer {0,1,2,…,65535}	See DELAY pins	timeline execution delay
Period	Bit_vector[0..7]	See PERIOD pins	Intra-frame waiting time
Mode	bit vector[0..15]	See CONFIG/EXPstraps	operational mode settings (exposure mode, subsampling, binning, interleaving, auto illum.control, …)
Test	bit_vector[0..7]	“00000000”	selects on-chip test configuration
Memwrite_A	bit_vector[0..23]	X	start address (byte address) of direct memory write (even only)
Memwrite_L	integer 0..65535	X	length of memory write operation, in words (can only write lower parts of memory!)
Memread_A	bit_vector[0..15]	X	start address (line address) of direct memory read
Memread_L	integer 0..65535	X	length of memory read operation, in lines of 1024 words
NextToWrite	Bit_vector[0..8]	0	Next image memory slot to accept an image from the sensor (even only)
NextToDownload	Bit_vector[0..8]	0	Next image in memory to be downloaded (even only)
FirstToCompress	Bit_vector[0..9]	0	First mage in memory ICA has to compress
NtoCompress	Bit_vector[0..7]	0	Number of images in memory ICA has to compress
ImageID	Bit_vector[0..11]	0	A 12-bit cyclic counter updated once for each image acquired.

Table 5 IRIS internal parameters and settings

2.6.2 Error log register

8-bit register ErrorState accumulates and keeps the most recent error history of IRIS. The register is cleared (only) whenever it is written to the memory as part of an image acquisition command (STORE_HKFRAMES, …), or when it is read as part of a direct image or housekeeping acquisition command (READ_HKFRAMES, READ_HK).

The contents of ErrorState are:

Position	contents
ErrorState[0]	An operation attempted to go out of memory
ErrorState[1]	An illegal command has been received
ErrorState[2]	An illegal command packet/segment has been received (header error, CRC error, or wrong length)
ErrorState[3]	The liveness watchdog on the command interface timed out and re-started the interface FSMs
ErrorState[4]	The liveness watchdog on the data output interface timed out and re-started the interface FSMs
ErrorState[5]	An FSM in the image acquisition sequencer has encountered an illegal state and as a result the particular image acquisition has been aborted, after which the next acquisition (if any) was started.
ErrorState[6]	Illegal state encountered in main FSM.
ErrorState[7]	Memory handover problem: IRIS could not get memory from ICA.

2.6.3 System start-up and reset

2.6.3.1 System configuration overview

IRIS-3 's default hardware configuration, sensor configuration, and start-up command are set with strappable pins:

pins	configuration, start-up actions	remarks	equivalent command
CONFIG[0..3]	0000 : with ICA, take a non-ending sequence of full-frame images. Store, compress, and transmit each image before acquiring the next one.	similar to a compressed video mode	COMPRESS_DOWNLOAD_HKFRAMES(128)
	0001 : standalone, idle	SDRAM maintenance processes are disabled.	-
	0010 : standalone, take and send a non-ending stream of full-frame images	similar to a non-compressed video mode	READ_HKFRAMES(128)
	0011 : standalone, take and send a non-ending stream of quarter-frame images (X1=256, X2=767, Y1 = 128, Y2=639)	actually larger than quarter-frame, at 512x512 pixels	READ_HKFRAMES(128)
	0100 : with buffer, idle	SDRAM maintenance processes are enabled	-
	0101 : with buffer, take and store a maximum-length stream of full-frame images	maximum-length meaning until the attached memory is full	STORE_HKFRAMES(128)
	0110 : with buffer, take and store a maximum-length stream of quarter-frame images (X1=256, X2=767, Y1=128 , Y2=639)		STORE_HKFRAMES(128)
	0111 : with buffer, take, store, and then transmit a maximum-length stream of full-frame images	download starts when memory is	STORE_DOWNLOAD_HKFRAME

		full	S(128)
	1000 : with buffer, take, store, and then transmit a maximum-length stream of quarter-frame images (X1=256, X2=767, Y1=128 , Y2=639)		STORE_DOWNLOAD_HKFRAMES(128)
	1001: with buffer; take and store one full-frame image		STORE_HKFRAMES(0)
	1010 : with ICA, idle	SDRAM maintenance processes are enabled	-
	1011 : with ICA, take, store, compress a maximum-length stream of full-frame images		COMPRESS_HKFRAMES(128)
	1100 : with ICA, take, store, compress a maximum-length stream of quarter-frame images (X1=256, X2=767, Y1=128 , Y2=639)		COMPRESS_HKFRAMES(128)
	1101 : with ICA, take, store, compress a maximum-length stream of full-frame images. Then download all compressed data.		COMPRESS_DOWNLOAD_HKFRAMES(128)
	1110 : with ICA; take, store, compressa maximum-length stream of quarter-frame images (X1=256, X2=767, Y1=128 , Y2=639). Then download all compressed data.		COMPRESS_DOWNLOAD_HKFRAMES(128)
	1111 : with ICA; take, store, compress one single image		COMPRESS_HKFRAMES(0)
DELAY[0..2]	000: 0 seconds	Time between external trigger or power-on and initial action	
	001: 2		
	010: 4		
	011: 8		
	100: 16		

	101: 32		
	110: 64		
	111: 128		
PERIOD[0..2]	000: 0 seconds, all images are in a consecutive stream, at 10 full frames/second	Time between two consecutive image acquisitions during initial action	
	001: 0.25 seconds		
	010: 0.5 seconds		
	100: 1 second		
	101: 2 seconds		
	110: 4 seconds		
	111: 8 seconds		
EXP[0..3]	0000 : Exposure = 1 line		
	0001 : 2 lines		
	0010 : 4 lines		
	0011 : 8 lines		
	0100 : 16 lines		
	0101 : 32 lines		
	0110 : 64 lines		
	0111 : 128 lines		
	1000 : 256 lines		
	1001 : 512 lines		

	1010 : full frame (768 lines)		
	1011 : AIC on, initial exposure is 256 lines		
	1100 : Bracketting on, wide, Exposure is 8 lines		
	1101 : Bracketting on, wide, Exposure is 16 lines		
	1110 : Bracketting on, wide, Exposure is 32 lines		
	1111 : Bracketting on, wide, Exposure is 128 lines		
APIDMSB[0..3]		APID MSB selection	
LSEG[0..1]	00 : no CCSDS packetizing of commands and data		
	01 : CCSDS, with LSEGMENT = 256 octets		
	10 : CCSDS, with LSEGMENT = 512 octets		
	11 : CCSDS, with LSEGMENT = 1024 octets		
DL_EDAC	0: no EDAC on download data, 10 bit pixels truncated to 8 bits when 16bit wide memory is installed 1: EDAC on download data		
DATAPAC	0: grouping (version 000) on data	Requires CCSDS enabled	
	1: segmentation (version 100, ESA PSS-04-106) on data	Requires CCSDS enabled	

Note: when IRIS is used with ICA, the hardware configuration can be set to the ‘with ICA’ scenarios, as well as to the ‘with buffer’ scenarios. In the latter case, communication with ICA will only be established when a directly ICA-related command is received by IRIS.

When standalone operation is selected, all on-chip logic for managing, driving, and refreshing the SDRAM, and all on-chip interfacing to the ICA are disabled. This logic can then have no further influence on the operation of the IRIS.

2.6.3.2 System startup, system reset, initial states and actions

Upon power on, the IRIS performs a reset initiated by the asynchronous RSTb pin. After this reset all internal settings and parameters take on their default values (see 2.6.3.1). Depending on the setting of CONFIG, the interactive mode or one of the autonomous acquisition modes is entered and the default command, if TRIG is '1', is executed. After reset IRIS assumes that ICA is ready to accept commands.

During reset all output signals take on their default de-asserted values. For the output interfaces, the specific default value on an output pin may depend on the specific interface the IRIS has been configured for.

The asynchronous reset pin RSTb has a direct, non-clocked path to all of the chip's registers. In addition, the reset pulse is internally synchronised and prolonged to guarantee a clean start-up. The internal reset lines are used for the RSTb-initiated reset as well as for the commanded reset (see RESET). The active period of the external RSTb signal must encompass 10 CLK cycles, measured from the point in time when the IRIS3's power supply has stabilised after power-on.

2.6.3.3 Externally triggered actions

Whenever IRIS-3 sees a rising edge on the TRIG input pin, the default start-up command (2.6.3.1) is executed. More specifically, if after system power-on TRIG is 1, the action is started immediately. If after system power-on TRIG = 0, IRIS waits until it sees a rising edge on TRIG. Then an additional time set by DELAY is waited, after which the default action is started.

If during normal operations, a rising edge in TRIG is sampled, the default command (2.6.3.1) is executed immediately ('immediately' being defined as if a new command demanding such action has been received on the command interface),.

Any action initiated by TRIG takes places with all register values (i.e. sensor configuration) having the value they had at the moment the TRIG arrived.

At all times the present value of DELAY holds, which means that the action following a TRIG trigger can indeed be delayed.

2.6.4 Commands: format, overview, and handling

The IRIS is interactively controlled by user command words, issued to the command input interface. The generic structure of a command comprises the actual command identifier (6 bits) and command and argument parity bits (2 bits, making 1 8-bit word in total), followed by one argument (8 bits or 1 word). Commands that have no actual argument still require the transmission of a dummy argument, of which the contents are ignored by the IRIS.

Command			Argument
Bits 0..5	Bit 6	Bit 7	Bits 0..7
Command Identifier	Odd parity over Command Identifier	Odd Parity over Argument	Argument value (bit 0 is MSB)

A command communication error occurs when one of the command's parity bits is faulty or when an unrecognised command is received. Faulty commands are ignored and thus can not change the state of the IRIS.

In general newly-arrived commands overwrite any pending older command: there is no command buffering.

Table 6 gives an overview of the available commands, including the output they generate and optional delayed operation by means of the builtin timeline.

Command name	executes when / setting becomes valid from:	direct raw image output	uses memory	house-keeping output	optional timeline execution
RESET	immediately	-	-	-	-
NOP	immediately	-	-	-	-
STOP	after clean abort of present action	-	-	-	-
COMPRESS	after present (if any) image acquisition command finishes	-	yes	-	-

SET_X1	after present (if any) image acquisition command finishes	-	-	-	-
SET_X2	after present (if any) image acquisition command finishes	-	-	-	-
SET_Y1	after present (if any) image acquisition command finishes	-	-	-	-
SET_Y2	after present (if any) image acquisition command finishes	-	-	-	-
SET_YSXS	after present (if any) image acquisition command finishes	-	-	-	-
SET_EXP*	after present (if any) image acquisition command finishes	-	-	-	-
SET_THRESHOLD	after present (if any) image acquisition command finishes	-	-	-	-
SET_MODE*	after present (if any) image acquisition command finishes	-	-	-	-
SET_NEXTTOWRITE*	immediately				
SET_NEXTTODOWNLOAD*	immediately				
READ_FRAMES	after previous command finishes	yes		optional	yes
READ_HKFRAMES	after previous command finishes	yes		Yes	yes
READ_HK	after previous command finishes			yes	yes
DOWNLOAD_FRAMES	after previous command finishes		yes	optional	yes
DOWNLOAD_HKFRAMES	after previous command finishes		yes	yes	yes
STORE_HKFRAMES	after previous command		yes		yes

	finishes				
STORE_DOWNLOAD_HKFRAMES	after previous command finishes		yes		
COMPRESS_HKFRAMES	after previous command finishes		yes		Yes
COMPRESS_DOWNLOAD_HKFRAMES	after previous command finishes		yes	yes	Yes
COMPRESS_DOWNLOAD2_HKFRAMES	after previous command finishes		yes	yes	Yes
SET_RC	immediately	-	-	-	Yes
SET_APID	immediately				
SET_TEST	immediately				
SET_TIMER*	immediately	-	-	-	-
SET_PERIOD	immediately				
SET_GAIN	immediately	-	-	-	-
SET_MEMWRA*	immediately				
SET_MEMWRL*	immediately				
WRITE_MEM	immediately				
SET_MEMRDA*	immediately				
SET_MEMRDL*	immediately				
READ_MEM	after previous command finishes		Yes		Yes

table 6 Overview of commands and their output

When CCSDS packetising is not used, IRIS receives and handles individual atomic commands. Command/argument pairs with a faulty parity bit are ignored. Between command and argument a time-out of 1 to 2 seconds holds. If this time-out period is exceeded, the IRIS-2 treats the next-incoming octet as a new command octet.

When packetising is selected, several atomic commands are grouped into one telecommand segment. IRIS then only executes the whole group of commands after the correct reception of the whole TC segment, i.e. a correct decoding of the packet's CRC

checksum. The exception are writes to the SDRAM memory, which are immediately executed, regardless of correct packet reception.

A command communication error occurs when the optional CRC indicates a fault, or when the 1-2 second async input interface time-out is encountered within a segment.

With packetising, only the last-in-packet command of the subset RESET, STOP, READ_*, STORE_*, DOWNLOAD_*, COMPRESS_* is executed after reception of the packet. In other words, a command packet should ever only contain one of the above commands. The other, parameter-setting, commands are all executed after proper and correct reception of the packet. If duplicate parameter-setting commands are received, e.g. {SET_X1(A), SET_X2(B), SET_X1(C)}, then only the final instance of the command is executed, thus SET_X1(C) in the example.

2.6.5 Command priorities and interrupts

2.6.5.1 Parameter updates

Image geometry and read-mode parameters are only updated internally when no image stream acquisition is in progress. In other words, all of the images belonging to a stream are taken with the same parameters (X1, Y1, X2, Y2, …).

All other system parameters take immediate effect. It is recommended that the user take care of not uploading memory configuration commands while a memory-accessing command is still running.

2.6.5.2 Command priorities

RESET has immediate effect.

STOP has almost-immediately effect, cleanly aborting the currently-executed command.

All other action-triggering (acquisition, download, memory read and write, ..)commands are buffered (depth is one, new arrivals overwriting any pending command) and their execution only starts after the completion of any previous action-triggering command.

2.6.6 Reset command

Command name	Command ID format	Argument
RESET	000001	dummy

RESET interrupts all current actions and performs a complete asynchronous reset on the device. The effect of RESET is equivalent to the hardware reset performed at power-on, with the exception of the power-on (delayed) command, which is not executed after a RESET. After RESET IRIS assumes that ICA is ready to accept commands.

A RESET should not ever be grouped with other commands into one single packet.

2.6.7 Stop and NOP commands

Command name	Command ID format	Argument
STOP	000110	dummy
NOP	000000	dummy

STOP cleanly interrupts all current actions and IRIS awaits the next command. If an image, a memory dump unit, or a housekeeping data unit, is being downloaded, the present download is completed, compliant with any packetizing rules, before the IRIS halts. All other scheduled unit downloads are cancelled. This way only complete images or data units are downloaded.

If the STOP arrives while an image is being acquired and written into the memory, the image acquisition is completed. If ICA has to act on that last image, the IRIS lets ICA complete that action too.

The N(o)OP(eration) command has no effect and can be used to fill/stuff command packets.

2.6.8 Camera parameter setting commands

The following procedures are used to set the various internal parameters of the IRIS.

2.6.8.1 Frame coordinate setting

Command name	Command ID format	Argument
SET_X1	100101	X1[0..7]
SET_X2	100110	X2[0..7]
SET_Y1	100111	Y1[0..7]
SET_Y2	101000	Y2[0..7]

In windowed readout mode the exact position of the window of interest or frame, with respect to a full image, is given with the coordinates of the top-left pixel, (X1,Y1), and those of the bottom-right pixel, (X2,Y2).

These coordinates are set as 11 bit unsigned integers, of which the MSB is set to '0', and the 7 next bits can be entered by the user. Further, the 3 least significant bits (the bits that are never part of an argument) of start coordinates are always assumed 0, while the 3 least significant bits of end coordinates are always assumed 1.

This way the horizontal dimension coordinates can be set in the range 0..1023, in steps of 8 pixels. Frames can start at positions 0, 8, 16, … 1016, i.e. X1 = X1[0..7]&"000". Non-subsampled frames can end at positions 7, 15, 23, … 1023, i.e. X2 = X2[0..7]&"111". When X- subsampling is used, (sub)frames end at the highest position which is legal under the current sequencing scheme (i.e. subsampling with an increment of 4,…) and which is less than or equal to X2[0..7]&"111".

The vertical dimension coordinates can be set in the range 0..1023, in steps of 8 lines. Frames can start at positions 0, 8, 16, … 1016, or Y1 = Y1[0..7]&"000". Non-subsampled frames can end at positions 7, 15, 23, … 1023, i.e. Y2 = Y2[0..7]&"111". When Y-direction subsampling is used, (sub)frames end at the highest position which is legal under the current sequencing scheme (i.e. subsampling with an increment of 4, …) and which is less than or equal to Y2[0..7]&"111".

Newly-changed co-ordinates are actively used from the next image acquisition command on.

It is at all times the responsibility of the end-user to keep the coordinate settings consistent and valid. The following rules have to be obeyed:

- $X1 \leq X2$
- $Y1 \leq Y2$

2.6.8.2 Subsampling settings

Command name	Command ID format	Argument
SET_XSYS	101001	"0000"&PS[0..1]&LS[0..1]

Frames can be read in a subsampling or sparse readout mode (see the SET_MODE command), skipping pixels and/or lines and thus trading trade spatial resolution for data compactness and for temporal resolution.

Subsampling can be engaged for the X and the Y directions separately, and is defined by the distance between lines to read and/or the distance between pixels to read:

PS	pixel subsampling rate in pixels, XS	LS	line subsampling rate in lines, YS
00	1	00	1
01	2	01	2
10	4	10	4
11	8	11	8

The frames read then start at line Y1 and then go to line (Y1+YS) and so on. Likewise, the pixels read in a line start at X1, and proceed through (X1+XS) and so on. The last line or pixel read in a subsampled frame are the last line or pixel addressed by the above scheme and less than or equal to Y2 or X2, respectively.

Thus subsampling gives a YS x XS reduction in data amount and an *approximate* YS x XS gain in frame rate.

Newly-set subsampling settings are actively used from the next image acquisition command on.

2.6.8.3 Interactive exposure control

Command name	Command ID format	Argument
SET_EXPH	101111	"000000"&Exp[0..1]
SET_EXPL	100001	Exp[2..9]

The parameter Exp(osure), together with the Exposure Mode setting in the Modes register, sets the integration or exposure time for the IRIS sensor.

Exp is an integer of the range 0 to 767.

When Exposure Mode equals 0, the image exposure time comprises of Exposure times the time needed to output one line, i.e. the portion of an image defined by X1, X2, and XS, (and the datarate of the output interface in direct-download mode). When Exposure Mode equals 1, the image exposure time comprises of Exposure times the time needed to output one frame, as defined by all windowing parameters.

For the nominal case of a full frame, output at maximum rate on the parallel interface, or to the SDRAM image buffer, the relation between the value of Exp, Exposure Mode and the sensor exposure time T_I is approximately as follows:

$$T_I = 0.1ms \times (Exp+1) \quad when\ Exposure\ Mode = 0,\ and$$

$$= 75ms \times Exp \quad when\ Exposure\ Mode = 1$$

The resulting exposure time is the time during which each sensor line is exposed to light. The image stare time is the time that elapses between the beginning of the exposure time and the end of the data transfer from sensor core to output interface or memory.

Note that, at room temperature, integration times of over 30 seconds result in auto-saturation by excess dark signal. Dark signal decreases with temperature.

It is at all times the responsibility of the end-user to keep the exposure settings consistent and valid. The following rule has to be obeyed:

- $(Exp+1) \leq (Y2-Y1+1)/YS$

The new setting in Exp comes into action after any currently being acquired image has been finished completely.

2.6.8.4 Automatic exposure control

When Mode[7] is asserted, exposure is henceforth controlled internally by an illumination control system (note that this system overwrites any user-made value in the Exposure register).

This control system attempts to regulate the median value of the pixel values in the currently acquired frame(s) to approximate the value of the parameter Threshold: the number of pixels in the frame larger than Threshold is regulated to be between 25% and 75% of the total number of pixels in the frame.

Only one in each two sequentially-acquired images are used to feed the AIC control loop, this to promote stability: during image N the AIC control algorithm is fed pixel data; image N+1 is taken with still the same exposure time as image N, while the AIC control algorithm is not being fed data anymore; image N+2 is taken with the new value of exposure, as given by the AIC control loop.

When AIC is enabled, the control loop is always active, even between images taken with different acquisition commands.

Threshold can be set under user control; it is an integer range 0 to 255 where 0 is black and 255 is fully white:

Command name	Command ID format	Argument
SET_THRESHOLD	100011	Threshold[0..7]

Threshold takes on its new value immediately after the reception of the SET_THRESHOLD command, or of the CCSDS packet containing a SET_THRESHOLD command.

When automatic exposure control is engaged, the IRIS continuously takes images to feed its AIC control loop. These images are not output, nor are they written to the memory. When a command requires the acquisition of an image, or when a currently being executed timeline requires so, the demanded image is output or written to the memory.

2.6.8.5 Bracketed exposure control

When Mode[13..14] = “01” (bracket on, narrow), exposure control is done by narrow bracketing: each three images taken are acquired with an effective integration time derived from Exp as follows: the first image gets Exp , the second image gets Exp x 2, the third image gets Exp / 2. When Mode[13..14] = “10” (bracket on, wide), the bracket is widened: the first image gets Exp , the second image gets Exp x 8 , the third image gets Exp / 8.

Bracketing can be used in situations where some beforehand knowledge of the required exposure time is known, but uncertain. Bracketing enhances the chance of obtaining at least some well-exposed images in a stream of frames.

2.6.8.6 Internal operational modes

Operating modes of the imager are set in a 16 –bit word. Note that the structure of this word is compatible with the mode settings word of the IRIS-2 chip and of the VMC monitoring camera.

Command name	Command ID format	Argument
SET_MODEH	100100	Mode[0..7]
SET_MODEL	101101	Mode[8..15]

Bit	Name	Function	Default value
0-1	-		
2	FPA Source	0 = pixel array 1 = AIN1	0
3	Exposure Mode	0 = lines; 1 = frames	0
4	-		
5-6	Image Read Mode	00 = normal read 01 = subsampling 10 = - 11 = -	00
7	Automatic Illumination Control	0 = off; 1 = on	see EXP pins
8	-		
9	TMTYPE	0 = CCSDS grouping 1 = ESA segmentation	see DATAPAC pins
10-11	LSEGMENT	00 = 2048 octets 01 = 256 10 = 512 11 = 1024	see LSEG pins

12	EDAC on image data download	0 = off, reduce all downloaded pixels to 8 upper bits 1 = on, and 10 bit pixels enabled	see DL_EDAC pin
13-14	Bracketed Exposure	00 = off 01 = narrow 10 = wide 11 = off	
15	Dual Slope Exposure	0 = off; 1 = on	

The new settings in Mode come into action after any currently being executed image or housekeeping command has been finished completely.

2.6.8.7 APID setting

Command name	Command type format	Argument
SET_APID	110000	'0'&APID[4..10]

SET_APID sets the 7 lower bits of the chip's telemetry APID. The upper 4 bits of the APID are always determined by the APIDMSB pins. The uploaded APID is used for all telemetry packets generated after the reception of the SET_APID command.

2.6.8.8 Digital remote control setting

IRIS has six digital output pins that can be set or reset under command by the end-user. These pins can be used for remote control of other components local to the IRIS chip.

Command name	Command type format	Argument
SET_RC	101010	RC[0..5]&"XX"

SET_RC sets the 8 digital output pins RC_OUT[0..7] to the value RC given as argument. RC_OUT takes on its new value within 400 ns after the reception of the SET_RC command, or of the CCSDS packet containing a SET_RC command. Alternatively, the execution of SET_RC can be postponed with the timer delay (see 5.10.10)

The remote control outputs are internally latched and retain their values until overridden by a new SET_RC command or by a system reset.

After power-on or a system reset the outputs RC_OUT are de-asserted, i.e. set to "00000000".

2.6.8.9 Test mode

Command name	Command type format	Argument
SET_TEST	110001	Test[0..7]

SET_TEST enables and disables any of eight in-built simplified chip configurations that facilitate production testing, debugging, or operation with less logic active.

Test bit	Name	Function	Devault value
0	SHOW_SENSE	when '1' put sensor drive signals on SDRAM address/data bus.	'0'
1	SHOW_PIX	when '1' put raw ADC data on the RC bus	'0'
2	RAM_DIS	when '1' disable all SDRAM functionality	'0'
3	NO_ERR	when '1' ignore all command errors	'0'
4	NO_DELAY	when '1' bypass delayed command timer	'0'
5	SENS_INV	when '1' invert sensor address buses	'0'

6	GET_RAM1	when '1' hand over SDRAM to slave, except refresh	'0'
7	GET_RAM2	when '1' hand over SDRAM to slave, disable refresh manager	'0'

SHOW_SENSE

All internal drive signals for the sensor core, amplifier, and ADC are shown on the SDRAM control ports:

SDRAM pin	corresponding sensor signal
RAM_A[12]	START_FRAMES
RAM_A[11]	SENDER_ENDED
RAM_A[10]	CLK_XRD
RAM_A[9]	CLK_ADCb
RAM_A[8]	SEL
RAM_A[7]	AY9
RAM_A[6]	AY8
RAM_A[5]	AY7
RAM_A[4]	AY6
RAM_A[3]	AY5
RAM_CS0b	GAIN(1)
RAM_CS1b	GAIN(0)
RAM_BA[1]	CAL
RAM_BA[0]	S
RAM_DQM	R
RAM_GRANT	RESET

RAM_D[15]	RESET_DS
RAM_D[14]	AY4
RAM_D[13]	AY3
RAM_D[12]	AY2
RAM_D[11]	AY1
RAM_D[10]	AY0
RAM_D[9]	AX9
RAM_D[8]	AX8
RAM_D[7]	AX7
RAM_D[6]	AX6
RAM_D[5]	AX5
RAM_D[4]	AX4
RAM_D[3]	AX3
RAM_D[2]	AX2
RAM_D[1]	AX1
RAM_D[0]	AX0

SHOW_PIX

The upper 8 bits output from the ADC are shown on the RC[0..7] output port.

RAM_DIS

All SDRAM control, management, and refresh logic is disabled in a way which still allows the operation of the rest of the device.

NO_ERR

No error checking is done on arriving commands:

- header bits that are normally checked are ignored
- command and argument parity bits are ignored
- command packet CRCs are ignored
- all commands execute upon arrival of either the atomic command itself, or after reception of a complete telecommand packet.

NO_DELAY

The mechanism for delayed command execution is disabled. All commands execute as if TIMER=”0000000000000000”, i.e. upon reception.

SENS_INV

The AY and AX internal address buses to the sensor core are logically inverted.

GET_RAM1

All access to the SDRAM is continuously granted to the slave, with the exception of refreshes. IRIS still performs refreshes, and afterwards returns RAM access to the slave.

GET_RAM2

All access to the SDRAM is continuously granted to the external slave device. IRIS’s refresh controller is completely disabled, the slave has to maintain RAM integrity.

2.6.8.10 Delayed command execution setting

Command name	Command type format	Argument
SET_TIMERL	101011	Timer[8..15]
SET_TIMERH	101100	Timer[0..7]

The following commands can be executed with a delay relative to the time of command reception:

- READ_FRAMES(N)
- READ_HKFRAMES(N)
- STORE_HKFRAMES(N)
- STORE_DOWNLOAD_HKFRAMES(N)
- COMPRESS_HKFRAMES(N)
- COMPRESS_DOWNLOAD_HKFRAMES(N)
- COMPRESS_DOWNLOAD2_HKFRAMES(N)
- READ_HK(dummy)
- SET_RC(ControlOut)

With a 25MHz system clock, the delay is equal to 1.00073 (TBC) seconds x Timer, with Timer valued 0..65535. This amounts to a nominal delay range of 0 up to 65535 seconds (or about 18 hours), in steps of 1 second. The timer feature always has an uncertainty of one delay unit, i.e. one nominal second. The countdown starts at the instant the SET_TIMERH command (or command packet) is received.

If Timer is defined to be 0, command execution is immediate, i.e. the normal mode of operation. If Timer does not equal 0, the next-received command which belongs to the group of four commands listed above will be delayed by the set time. If Timer is re-set during a running delay countdown, the countdown restarts at the new Timer value.

If a new command of the above list is issued while a prior such command already is awaiting delayed execution, the new command effectively replaces the old one. The timing countdown is *not* restarted.

It is possible to abort a timer countdown by issuing a STOP command, to overrule the actual pending command, and then setting the timer register to 0.

2.6.9 Image acquisition, compression, download commands

2.6.9.1 Inter-frame period

Command name	Command type format	Argument
SET_PERIOD	101110	Period[0..7]

During image acquisition, Period sets the time between two consecutive frames, defined as the time between the acquisition of the last pixel of the first frame, and the start of the initial exposure time of the second frame. (In case of

COMPRESS_DOWNLOAD2_HKFRAMES Period is defined as between the last pixel downloaded of the first frame and the start of the initial exposure time of the second frame.)

The relation between the binary value of Period and the time is (approximately):

Period	time (s)
0	0 (stream of concatenated images)
1	0.25
2	0.5
3	1
4	2
5	4
6	8
7	16
8	32
Others	0

When Period = 0, all images are concatenated, and during the acquisition of image N, already some lines of image N+1 are exposed to light, due to the rolling blade principle of the electronic shutter.

Period is effective with the following commands:

- READ_FRAMES
- READ_HKFRAMES
- STORE_HKFRAMES
- STORE_DOWNLOAD_HKFRAMES

- COMPRESS_HKFRAMES
- COMPRESS_DOWNLOAD_HKFRAMES
- COMPRESS_DOWNLOAD_HKFRAMES

2.6.9.2 Pure image acquisition commands

Command name	Command type format	Argument
READ_FRAMES	000010	N[0..7]
READ_HKFRAMES	000100	N[0..7]

READ_FRAMES reads N+1 (N is an integer range 0..128) frames. When N = 128, an endless stream of frames is readREAD_FRAMES can not be used with CCSDS packetising enabled.

READ_HKFRAMES(N) works identical to READ_FRAMES(N), with the exception that, before an/each image is output, IRIS also sends housekeeping data as the first packet (HK, see 2.7.2). These housekeeping data hold information about the imager settings used in the following image frame, internal error information, and remote sensing measurements, and optional ICA information.

2.6.9.3 Image acquisition with memory storage, possibly followed by download

Command name	Command type format	Argument
STORE_HKFRAMES	001000	N[0..7]
STORE_DOWNLOAD_HKFRAMES	******	N[0..7]

STORE_HKFRAMES reads N+1 (N is an integer range 0..127) frames, and stores them in memory, the first frame at position NextToWrite. When the memory boundaries are exceeded STORE_HKFRAMES halts. With each image stored, a housekeeping packet is written in memory too, for future optional download

STORE_DOWNLOAD_HKFRAMES reads N+1 (N is an integer range 0..128, 128 meaning an endless stream) frames, and stores them in memory, the first frame at position NextToWrite. After the last image acquisition, all images are downloaded from the first image on. Each image downloaded is preceded by its housekeeping packet..

2.6.9.4 Image acquisition, storage, and compression

Command name	Command type format	Argument
COMPRESS_HKFRAMES	010001	N[0..7]

COMPRESS_HKFRAMES reads N+1 (N is an integer range 0..127) frames, and stores them in memory, the first frame at position NextToWrite. ICA is instructed to compress each image as soon as possible. When the memory boundaries are exceeded COMPRESS_HKFRAMES halts. With each image stored, a housekeeping record is written in memory too, for future optional download. Image acquisition, compression, and download

Command name	Command type format	Argument
COMPRESS_DOWNLOAD_HKFRAMES	010010	N[0..7]
COMPRESS_DOWNLOAD2_HKFRAMES	001100	N[0..7]

COMPRESS_DOWNLOAD_HKFRAMES reads N+1 (N is an integer range 0..128, 128 meaning an endless stream) frames, and stores them in memory, the first frame at position NextToWrite. ICA is instructed to compress each image as soon as possible. After compression of all the images, they are downloaded. Each image downloaded is preceded by its housekeeping packet.. COMPRESS_DOWNLOAD2_HKFRAMES reads N+1 (N is an integer range 0..128, 128 meaning an endless stream) frames, and stores each of them in memory, at position NextToWrite. ICA is instructed to compress each image as soon as possible. After compression, this image is downloaded. Then the next image is acquired and stored, in the same memory position. Each image downloaded is preceded by its housekeeping packet.

2.6.9.5 Handling of FSM crashes during image acquisition

Whenever any major controlling FSM in the image acquisition logic encounters an illegal state, the image acquisition is aborted. Any entries made in the memory location table for that image are cleared. If more images were still pending (e.g. READ_FRAMES(N) command with N > 1), the acquisition continuous with the next image.

2.6.9.6 Commanded compression

Command name	Command type format	Argument
COMPRESS	010000	-

COMPRESS forces IRIS-3 to release the memory to ICA. If prior to this the user has written ICACommand and related parameters directly into the parameter-passing area of the memory, this command can be used to start a new action on ICA.

2.6.9.7 Image download

Command name	Command type format	Argument
DOWNLOAD_FRAMES	001001	N[0..7]
DOWNLOAD_HKFRAMES	001010	N[0..7]

DOWNLOAD_FRAMES reads N+1 (N is an integer range 0..128) frames from the memory, beginning at NextToDownload, and downloads them over the data interface. When N = 128, an endless stream of frames is read. When the memory boundaries are exceeded DOWNLOAD_FRAMES halts. DOWNLOAD_FRAMES can not be used with CCSDS packetising enabled.

DOWNLOAD_HKFRAMES(N) works identical to DOWNLOAD_FRAMES(N), with the exception that, before an/each image is output, IRIS also sends its attached housekeeping data in the first packet (HK, see 5.12).

When no data are available for download, the command is ignored. When N brings the download beyond the last-available image/data slot, download wraps-around to position 0 and continues until N is reached.

Activity on the D_READY/SDS_P pin of a TTC-B-01 data output interface, not preceeded by any command causing data download, is to be interpreted as a DOWNLOAD_HKFRAMES command. If no download is busy, and data can be downloaded, when cycles on SDS_P start, a DOWNLOAD_HKFRAMES(128) is initiated. When SDS_P activity pauses, the download pauses, to be resumed when new SDS_P cycles arrive. When the equivalent DOWNLOAD_HKFRAMES(128) ends, i.e. when the memory bounds are exceeded, any following SDS_P cycles cause a new DOWNLOAD_HKFRAMES(128) to start.

2.6.9.8 Image memory management

Command name	Command type format	Argument
SET_NEXTTOWRITEH	110100	"0000000"&NextToWrite[0]
SET_NEXTTOWRITEL	110101	NextToWrite[1..8]
SET_NEXTTODOWNLOADH	110110	"0000000"&NextToDownload[0]
SET_NEXTTODOWNLOADL	110111	NextToDownload[1..8]

Sets parameters NextToWrite, where the next-acquired image will be written, and NextToDownload, indicating the next stored image to be downloaded.

When using these the user has to keep track of the number of frames to download and has to issue DOWNLOAD_HKFRAMES with the correct argument.

2.6.10 Housekeeping and analogue signal remote sensing commands

IRIS can sample local analogue signals, via one analogue input pin(see section 5.15 for a description of the analogue input). These data can be retrieved, together with internal system housekeeping and error log data, by means of the READ_HK(dummy) command, followed by an (ignored) dummy argument.

Command name	Command type format	Argument
READ_HK	000101	Dummy

2.6.11 Direct memory access commands

2.6.11.1 Writing the off-chip memory

Command name	Command type format	Argument
SET_MEMWRAL	111000	MEMWRITE_A[0..7]
SET_MEMWRAM	110011	MEMWRITE_A[8..15]
SET_MEMWRAH	111001	MEMWRITE_A[16..23]
SET_MEMWRLL	111010	MEMWRITE_L[0..7]
SET_MEMWRLH	111011	MEMWRITE_L[8..15]
WRITE_MEM	001110	D[0..7]

The buffer memory's lowest locations (range (0,0)..(127,1023), and only each word's 8 highest bits when 16 bit memory is installed), normally used for sharing commands and parameters between IRIS-3 and ICA, for configuration of the ICA, and for the data location table, can be randomly written by the end-user through commands. (Note: EDAC is active when 16-bit memory is used.)

The three SET_MEMWRA* commands set the memory write base address MEMWRITE_A[0..23]. This is a 24-bit address, addressing the lower memory range (0-16383, 0-1023), i.e. the lower 16 megawords, including ICA control and parameter area, the image data location tables, and part of the image space.

SET_MEMWRITEL* sets the amount of octets to be consecutively written into the memory, i.e. the memory positions written are MEMWRITE_A, MEMWRITE_A+1, … MEMWRITE_A+MEMWRITE_L-1.

After MEMWRITE_A and MEMWRITE_L have been set, the next MEMWRITE_L WRITE_MEM(D) commands received result in the value D being written into the address range MEMWRITE_A, MEMWRITE_A+1, … MEMWRITE_A+MEMWRITE_L-1.

The WRITE_MEM facility can be used to directly control the behaviour of ICA by writing the in-memory compression control parameters ICA_COMMAND, FIRST_TO_COMPRESS, NTOCOMPRESS.

Note: when CCSDS packetizing is used and full protection from command reception faults is required, each command packet can only contain a WRITE_MEM if MEMWRITE_L=1. In this case the write shall only be executed after correct reception of the packet's CRC.

When CCSDS is used and MEMWRITE_L > 1, all MEM_WRITE commands in the packet shall be executed at once, without checking the CRC.

If a MEM_WRITE is executed to the ICA Parameter Area, (1-495, 0-1023), then IRIS sets ICA COmmand to ATTN after each WRITE_MEM command has been executed (all expected writes have been done).

On receiving a CCSDS command packet, IRIS grabs the memory and starts a refresh cycle. This refresh cycle takes 1.4ms. In this period, from the first header byte sent till refreshing ends, no WRITE_MEM command must be sent to IRIS. Therefore the command packet could be stuffed with an appropriate amount of NOPs.

2.6.11.2 Reading the memory

Command name	Command type format	Argument
SET_MEMRDAL	111100	MEMREAD_A[0..7]
SET_MEMRDAH	111101	MEMREAD_A[8..15]
SET_MEMRDLL	111110	MEMREAD_L[0..7]
SET_MEMRDLH	111111	MEMREAD_L[8..15]
READ_MEM	001111	-

The entire buffer can be line-based read by the end-user through commands.

The two SET_MEMRD* commands set the memory read base line address MEMREAD_A. MEMREAD_A points to a physical memory address equal to

MEMREAD_A x 1024, or (MEMREAD_A, 0). SET_MEMWRITEL* sets the amount of memory lines, each 1024 8-bit words () or 16-bit words (), to be consecutively read from the memory, i.e. the memory positions read are MEMREAD_A x 1024, MEMREAD_A x 1024 +1, … (MEMREAD_A+MEMREAD_L-1) x 1024 + 1023.

After MEMREAD_A and MEMREAD_L have been set, the next READ_MEM(-) command received results in the IRIS-3 reading out the requested memory lines, downloading each of them as a memory dump packet, each line distributed over one or more packets. With packetising enabled, this group of memory dump packets is preceded by a housekeeping packet corresponding with the last image that was output.

2.6.11.3 Setting amplifier gain

Command name	Command type format	Argument
SET_GAIN	100010	"0000"&GAINI[0..1]&GAINF [0..1]

SET_GAIN sets the output amplifier's voltage gain for the pixel array (GAINF)

GAINF	amplifier gain
"00"	1
"01"	2.5
"10"	4.6
"11"	8.6

2.7 IRIS command and data formats

IRIS generates output in data units. A data unit is a set of octets, or of words, which logically belong to each other:

- Housekeeping data (dump of internal registers, CCSDS segmentation info, ICA info)
- Raw image line, or a segment of a line
- Compressed image data chunk

- Memory dump data chunk

In addition, data units can be packetized according to the CCDSDS standard, in which case each of them gets a packet header.

When CCSDS/ESA-PSS packetising is used, all data of a raw or compressed image as well as all data generated by a memory dump command, is output in packets that are grouped by the mechanisms explained in section 2.5.3. Such groups of packets always have a housekeeping data unit as the first packet of the group.

2.7.1 Command and data packet protocols

The digital interfaces, with exception of both frame grabber-like data outputs, can be used with a two-layered data format. The optional top layer packages data in CCSDS/ESA standard telecommand segments or telemetry packets. The bottom layer is proprietary to IRIS-3 and defines the format of application commands, housekeeping data and image data. ESA/CCSDS TC/TM standard packetising is selected by hardwiring configuration pins.

2.7.1.1 Protocol selection

Strappable pins APIDMSB, LSEG, and DATAPAC select between operation in CCSDS-packetised mode with grouping, ESA-packetised mode with segmentation, or unpacketised mode (see 2.6.3.).

When the packetised mode is selected, IRIS accepts telecommand (TC) and telemetry (TM) packets on its selected command input, and outputs source packets or telemetry I packets on its selected data output.

When the non-packetised mode is selected, IRIS accepts raw atomic commands and outputs raw data.

Strappable pins LSEG are used to set LSEGMENT, a parameter indicating maximum packet data length, or maximum segment data length, where applicable. LSEGMENT can take on the following values:

- 256 octets
- 512 octets

- 1024 octets
- 2048 octets

There are also commands that upload the APID, LSEGMENT, and type settings for the telemetry link. These commands overrule the corresponding settings straps for these parameters.

2.7.1.2 CCSDS telecommand segment definition (optional)

When the IRIS is configured for ESA/CCSDS TC/TM packetising mode, commands are received as packets.

Telecommand Packet or Telemetry Packet Interpreted as Command

PACKET HEADER							PACKET DATA FIELD	
PACKET IDENTIFICATION				PACKET SEQUENCE CONTROL		PACKET LENGTH	APPLICATION DATA	PACKET ERROR CONTROL
Version Number	Type	Data Field Header Flag	Application Process ID	Sequence Flags	Packet Name			
(3 bits)	(1 bit)	(1 bit)	(11 bits)	(2 bits)	(14 bits)	(16 bits)	(variable)	(16 bits)

- Version Number: "000" for TCs and CCSDS TMs proper,. "100" for PSS TMs (checked for equality to "*00")
- Type: not checked, accepting telecommands as well as telemetry data serving as commands.
- Data Field Header Flag: always set to "0" (checked).
- Application Process ID (APID): bits 0 to 3 of the inbound APID must match the settings at the strappable APID[0..3] pins for the telecommand to be accepted. In addition, the incoming APID[10] must equal '0', and incoming APID's bits 4 to 9 are echoed in the APID of all subsequent telemetry packets (until the outgoing APID is set with the SET_APID command)
- Sequence Flags: always set to "11" (checked).
- Packet Name: ignored.
- Packet Length: number of octets in the Packet Data Field –1.
- Application Data: contains one full IRIS telecommand, 0 up to 256 octets. Incoming packets with length in excess of 256 octets are rejected.
- Packet Error Control: a standard CRC-16 checksum over the whole telecommand packet. The polynomial is $x^{16}+x^{12}+x^5+1$, decoding register initial condition is FFFFh. Sample code for a decoding engine can be found in section 4.

2.7.1.3 CCSDS telemetry packet description, with grouping (optional)

When the IRIS is configured for TC/TM packetising mode, the following format is used for telemetry data (the format complies to TM packet version 000, see [AD24-26].

Grouping is used to keep packets that belong to a larger data entity (defined as a raw image or a compressed image) together.

Telemetry Packet (with CCSDS grouping)

PACKET HEADER							PACKET DATA FIELD
PACKET IDENTIFICATION				PACKET SEQUENCE CONTROL		PACKET LENGTH	APPLICATION DATA
Version Number	Type	Data Field Header Flag	Application Process ID	Sequence Flags	Source Sequence Count		
(3 bits)	(1 bit)	(1 bit)	(11 bits)	(2 bits)	(14 bits)	(16 bits)	(variable)

- Version Number: always set to“000”, for grouping of source packets.
- Type: always set to “0”, telemetry type.
- Data Field Header Flag: always set to “0”.
- Application Process ID: reflects the settings at pins APIDMSB[0..3], combined with a default 6Eh, and after reception of a telecommand, the bits 4 to 9 of the incoming command’s APID are reflected, augmented with a ‘1’in the LSB position, after a SET_APID command the outgoing APID is controlled by APIDMSB and the contents of the SET_APID command.
- Grouping Flags: “11” for a single ungrouped source packet. When subsequent source packets are to be grouped into one larger data entity, “01” for the first packet, “10” for the last packet, and “00” for intermediate packets.
- Source Sequence Count: contains a cyclic counter state of 14 bits, to distinguish and to order packets.
- Packet Length: number of octets in the Packet Data Field – 1.
- Application Data: a single ungrouped packet can contain only housekeeping data; raw or compressed image data, as well as memory dump data, are sent as grouped packets, the first packet always being a housekeeping packet.
- Image data, compressed or raw, are sent source-segmentated in packets of a fixed amount of octets, (packet data length is 256, 512 or 1024 octets). When using 8-bit pixel depth mode, each pixel (or each compressed-data word) needs one octet; when using EDAC-protected 8-bit or 10-bit pixel depth mode, each pixel (or each compressed-data word) needs two octets. When downloading EDAC-protected data from SDRAM, the data get checked and corrected when read from the memory, and the correction bits for the outbound data are re-calculated.

2.7.1.4 ESA PSS-04-106 telemetry packet description, with segmentation (optional)

When the IRIS is configured for ESA-style packetising mode, the following format is used for image and housekeeping telemetry data (the format complies to TM packet version 100, see [AD24].

True segmentation of source packets is not attempted. Rather, compatibility with the standard is arrived at by making all source packets identical to segments (i.e. unsegmented), and by providing the end-user with meta-data describing the segments that belong together. These meta-data are part of a housekeeping telemetry packet (see section 2.7) included at the beginning of each set of related image or memory data packets.

Telemetry Packet (with ESA-PSS segmentation)

PACKET HEADER							PACKET DATA FIELD
PACKET IDENTIFICATION				PACKET SEQUENCE CONTROL		PACKET LENGTH	APPLICATION DATA
Version Number	Type	Data Field Header Flag	Application Process ID	Sequence Flags	Source Sequence Count		
(3 bits)	(1 bit)	(1 bit)	(11 bits)	(2 bits)	(14 bits)	(16 bits)	(variable)

- Version Number: always set to“100”, for segmentation of source packets.
- Type: always set to “0”, telemetry type.
- Data Field Header Flag: always set to “0”.
- Application Process ID: reflects the settings at pins APIDMSB[0..3], combined with a default 6Eh, and after reception of a telecommand, the bits 4 to 9 of the incoming command’s APID are reflected, augmented with a ‘1’ in the LSB position , after a SET_APID command the outgoing APID is controlle byd APIDMSB and the contents of the SET_APID command.

- Sequence Flags: “11”.
- Source Sequence Count: contains a cyclic counter state of 14 bits, to distinguish and to order packets.
- Packet Length: number of octets in the Packet Data Field – 1, with a maximum of LSEGMENT-1.
- Application Data: When using 8-bit pixel depth mode, each pixel (or each compressed-data word) needs one octet; when using EDAC-protected 8-bit or 10-bit pixel depth mode, each pixel (or each compressed-data word) needs two octets. When downloading EDAC-protected data from SDRAM, the data get checked and corrected when read from the memory, and new correction bits are added to the output data.

2.7.2 Housekeeping data unit format

The housekeeping unit contains the IRIS register settings attached to each image acquisition, possibly augmented with image or data object meta-information to be used when segmenting CCSDS packets.

Octet nr.	Contents	Remarks
1	HK_TYPE[0..1]&MEM_SLOT[0..5]	HK_TYPE: Type of housekeeping packet "00": stand-alone HK "01": linked to raw image "10": linked to compressed image "11": linked to memory dump MEM_SLOT: Image location table entry number the following image is linked to (undefined when HK_TYPE="00" or "11")
2	MEMSLOT[6..8]	
3	ImageID[0..7]	Unique image identifier, for following image (undefined when HK_TYPE="00" or "11")
4	ImageID[8..11]&IMageIDMod&Written&Compres"e"&"0"	
5	NPACS[0..7]	Number of packets for the following image or memory dump (ESA PSS segmentation meta info, see 2.5.3.2)
6	NPACS[8..15]	
7	X1[0..7]	
8	Y1[0..7]	
9	X2[0..7]	

10	Y2[0..7]	
11	“0000”&XS&YS	
12	Exposure[0..7]	
13	Threshold[0..7]	
14	Gains[0..7]	
15	ControlOut[0..7]	
16	ErrorState[0..7]	
17	Mode[0..7]	
18	Mode[8..15]	
19	Period[0..7]	
20	AIN1[0..7]	
21	-	undefined
22	-	undefined
23	AIN1[8..9]&”000000”	
24	NextToWrite[0..7]	
25	NextToDownload[0..7]	
26	NextToWrite[8]&NextToDownload”8]&”00”000”	

Normally a housekeeping data unit is linked into a – raw or compressed – image packet, through commands such as COMPRESS_HKFRAMES(N). When a housekeeping packet is downloaded with a READ_HK(N) command, then some values in the register dump are not defined (MEM_SLOT, ID), NPACS=0, and ICAL=0.

2.7.3 Raw image data unit format

PixelValue: bit vector [0..9]; 1023 = white, 0 = black

Non-packetized

	8-bit format		16-bit format
octet nr.	Contents	octet nr.	Contents
1	PixelValue[0..7]	1	PixelValue[0..7]
2	PixelValue[0..7]	2	PixelValue[8..9]&EDAC[0..3]&"00"
3	PixelValue[0..7]	3	PixelValue[0..7]
4	PixelValue[0..7]	4	PixelValue[8..9]&EDAC[0..3]&"00"
…		…	
L-1	PixelValue[0..7]	2xL-1	PixelValue[0..7]
L	PixelValue[0..7]	2xL	PixelValue[8..9]&EDAC[0..3]&"00"

In 8-bit format, a unit holds L 8-bit pixel values, L being the length of the image line read (i.e. (X2-X1+1)/XS). In 16-bit format, a unit holds up 2xL octets, two octets for each 10-bit pixel value with its own EDAC checkbits.

Packetized

	8-bit format		16-bit format
octet nr.	Contents	octet nr.	Contents
1	PixelValue[0..7]	1	PixelValue[0..7]
2	PixelValue[0..7]	2	PixelValue[8..9]&EDAC[0..3]&"00"
3	PixelValue[0..7]	3	PixelValue[0..7]
4	PixelValue[0..7]	4	PixelValue[8..9]&EDAC[0..3]&"00"
…		…	
LSEGMENT-1	PixelValue[0..7]	LSEGMENT-1	PixelValue[0..7]

LSEGMENT	PixelValue[0..7]	LSEGMENT	PixelValue[8..9]&EDAC[0..3]&"00"

In 8-bit format, a unit holds up to LSEGMENT 8-bit pixel values. In 16-bit format, a unit holds up to LSEGMENT/2 10-bit pixel values, each with its own EDAC checkbits.

If, even when 16-bit memory is installed, MODE[12]=0 (meaning: no EDAC on image data), the raw image download happens as if 8-bit memory were installed. I.e. the 8-bit output words of the sensor are transmitted, after possible error-correction using the EDAC bits stored in memory, but new EDAC bits are not generated for the downlink, and no EDAC bits are transmitted. Note that this loses the two LSBs of the originally 10-bit wide pixel data.

2.7.4 Compressed data unit format

DataValue: bit vector [0..7];

Non-packetized

	8-bit format		16-bit format
octet nr.	Contents	octet nr.	Contents
1	DataValue[0..7]	1	DataValue[0..7]
2	DataValue[0..7]	2	"00"&EDAC[0..3]&"00"
3	DataValue[0..7]	3	DataValue[0..7]
4	DataValue[0..7]	4	"00"&EDAC[0..3]&"00"
…		…	
L-1	DataValue[0..7]	2xL-1	DataValue[0..7]
L	DataValue[0..7]	2xL	"00"&EDAC[0..3]&"00"

In 8-bit format, a unit holds 1024 8-bit data values,. In 16-bit format, a unit holds 2048 octets, two octets for each 8-bit data value with its own EDAC checkbits.

If, even when 16-bit memory is installed, MODE[12]=0 (meaning: no EDAC on compressed data), the compressed image download happens as if 8-bit memory were installed. I.e. the 8-bit output words of the ICA are transmitted, after possible error-

correction using the EDAC bits stored in memory, but new EDAC bits are not generated for the downlink, and no EDAC bits are transmitted.

Packetized

	8-bit format		16-bit format
octet nr.	Contents	octet nr.	Contents
1	DataValue[0..7]	1	DataValue[0..7]
2	DataValue[0..7]	2	“00”&EDAC[0..3] &”00”
3	DataValue[0..7]	3	DataValue[0..7]
4	DataValue[0..7]	4	“00”&EDAC[0..3] &”00”
…		…	
LSEGMENT-1	DataValue[0..7]	LSEGMENT-1	DataValue[0..7]
LSEGMENT	DataValue[0..7]	LSEGMENT	“00”&EDAC[0..3]&”00”

In 8-bit format, a unit holds up to LSEGMENT 8-bit data values. In 16-bit format, a unit holds LSEGMENT/2 8-bit data values, each with its own EDAC checkbits.

A compressed data unit may contain ICA-related header information in its first octets. Consult the ICA Data Sheet for more information on the internal compressed data unit structure.

2.7.5 Memory dump data unit format

DataValue: bit vector [0..7];

Non-packetized

	8-bit format		16-bit format
octet nr.	Contents	octet nr.	Contents
1	DataValue[0..7]	1	DataValue[0..7]
2	DataValue[0..7]	2	“00”&EDAC[0..3] &”00”
3	DataValue[0..7]	3	DataValue[0..7]
4	DataValue[0..7]	4	“00”&EDAC[0..3] &”00”
…		…	
L-1	DataValue[0..7]	2xL-1	DataValue[0..7]
L	DataValue[0..7]	2xL	“00”&EDAC[0..3] &”00”

In 8-bit format, a unit holds 1024 8-bit data values,. In 16-bit format, a unit holds 2048 octets, two octets for each 8-bit data value with its own EDAC checkbits.

Packetized

	8-bit format		16-bit format
octet nr.	Contents	octet nr.	Contents
1	DataValue[0..7]	1	DataValue[0..7]
2	DataValue[0..7]	2	“00”&EDAC[0..3] &”00”
3	DataValue[0..7]	3	DataValue[0..7]
4	DataValue[0..7]	4	“00”&EDAC[0..3] &”00”
…		…	
LSEGMENT-1	DataValue[0..7]	LSEGMENT-1	DataValue[0..7]

LSEGMENT	DataValue[0..7]	LSEGMENT	“00”&EDAC[0..3] &”00”

In 8-bit format, a unit holds up to LSEGMENT 8-bit data values. In 16-bit format, a unit holds 2048 8-bit data values, each with its own EDAC checkbits.

2.7.6 Additional EDAC in stream

With the DL_EDAC pin or the MODE[12] bit the generation of EDAC bits can be enabled for all downloaded data, even when no EDAC on the memory has been specified. As a result, each data octet requires two transmitted octets.

2.8 Known bugs

2.8.1 Immediate reset

The RESET command is always executed immediately upon reception, ignoring the rest of the packet and packet validity when in CCSDS mode. Any other command or command packet immediately following this RESET can be ignored. It is recommended to observe a 2 second period between sending a RESET and any other next command or command packet.

2.8.2 Parallel data interface at 3.125MW/s

When using CCSDS packet telemetry on the parallel output interface combined with the 3.125MW datarate, the first 6 octets of the CCSDS header are transmitted at 6.25MW/s.

3 Physical and electrical specifications

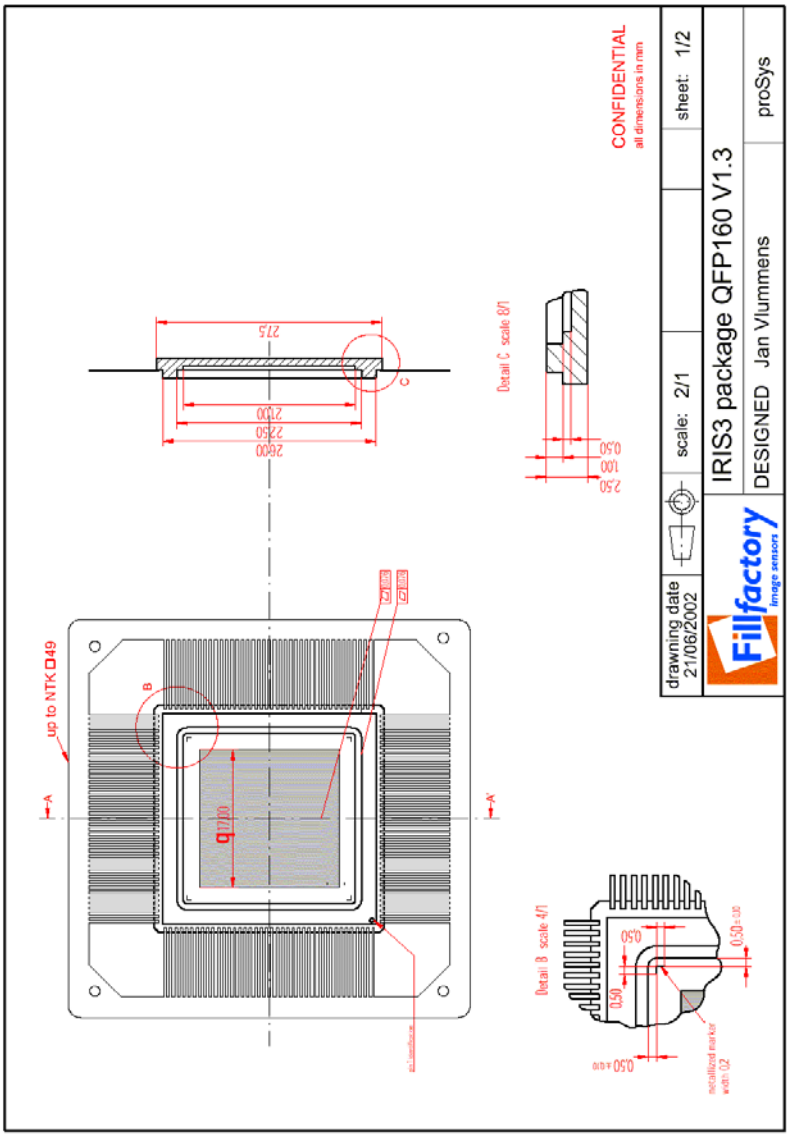
3.1 Overview

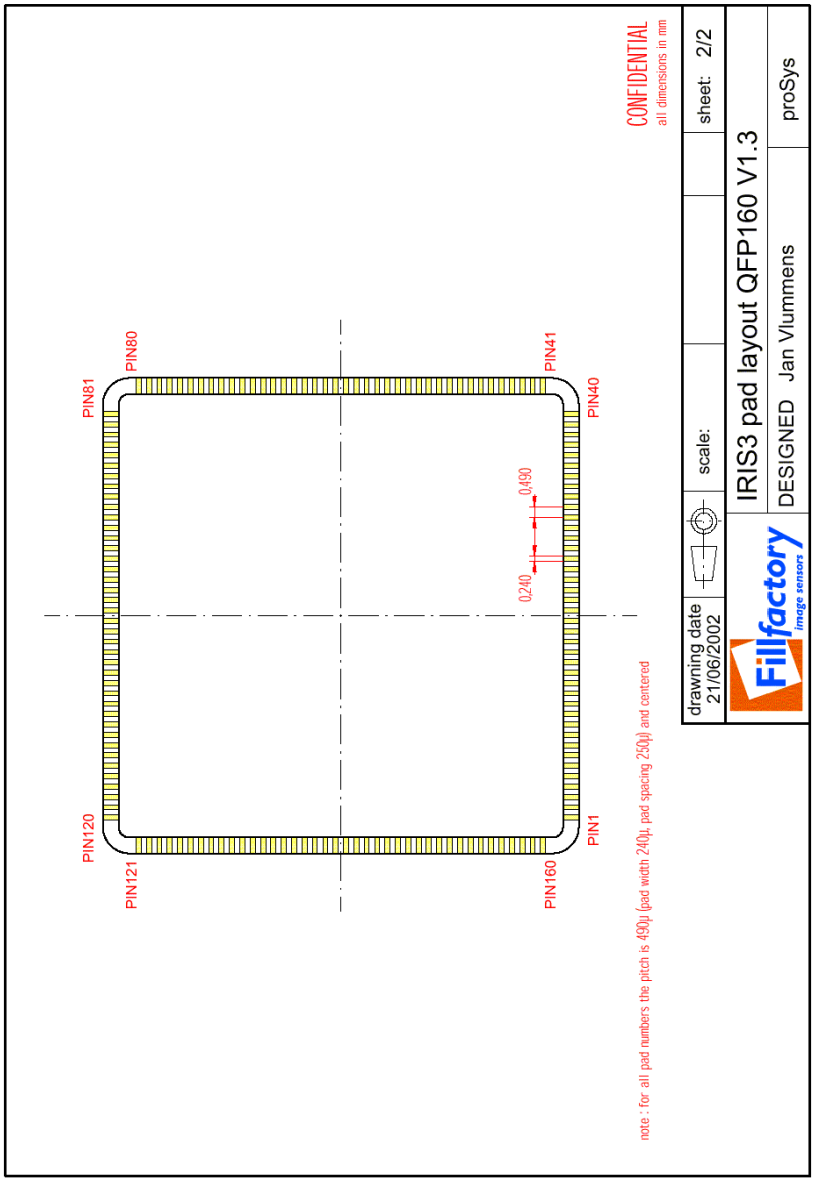
ASIC technology	AMI Semiconductor Belgium 0.5µ analogue CMOS C05M-A	formerly Alcatel MicroElectronics/Mietec
Electrical I/O	3.3V CMOS I/O	
packages	CQFP160, PGA201	specific glass lid on demand
total-dose radiation tolerance	30 krad	80 krad with reduced performance
LU/SEU resistance	TBA	
clock frequency	20MHz or 25MHz	other rates, up to 28MHz, when SDRAM interface not in use
power consumption	< 620mW	30 krad
Power supply voltages	5V and 3.3V	
Temperature range	-40..65°C	

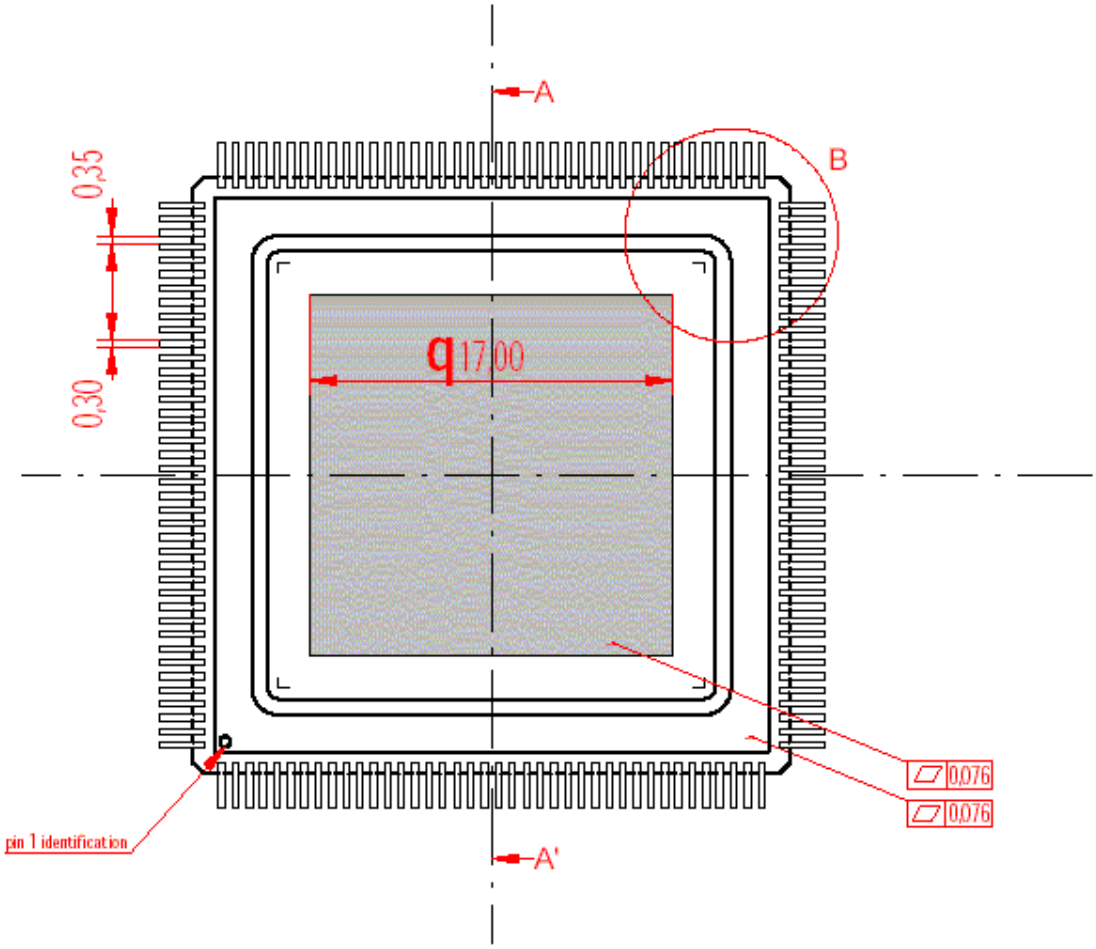
3.2 Mechanical specifications and pin list

3.2.1 Package drawings

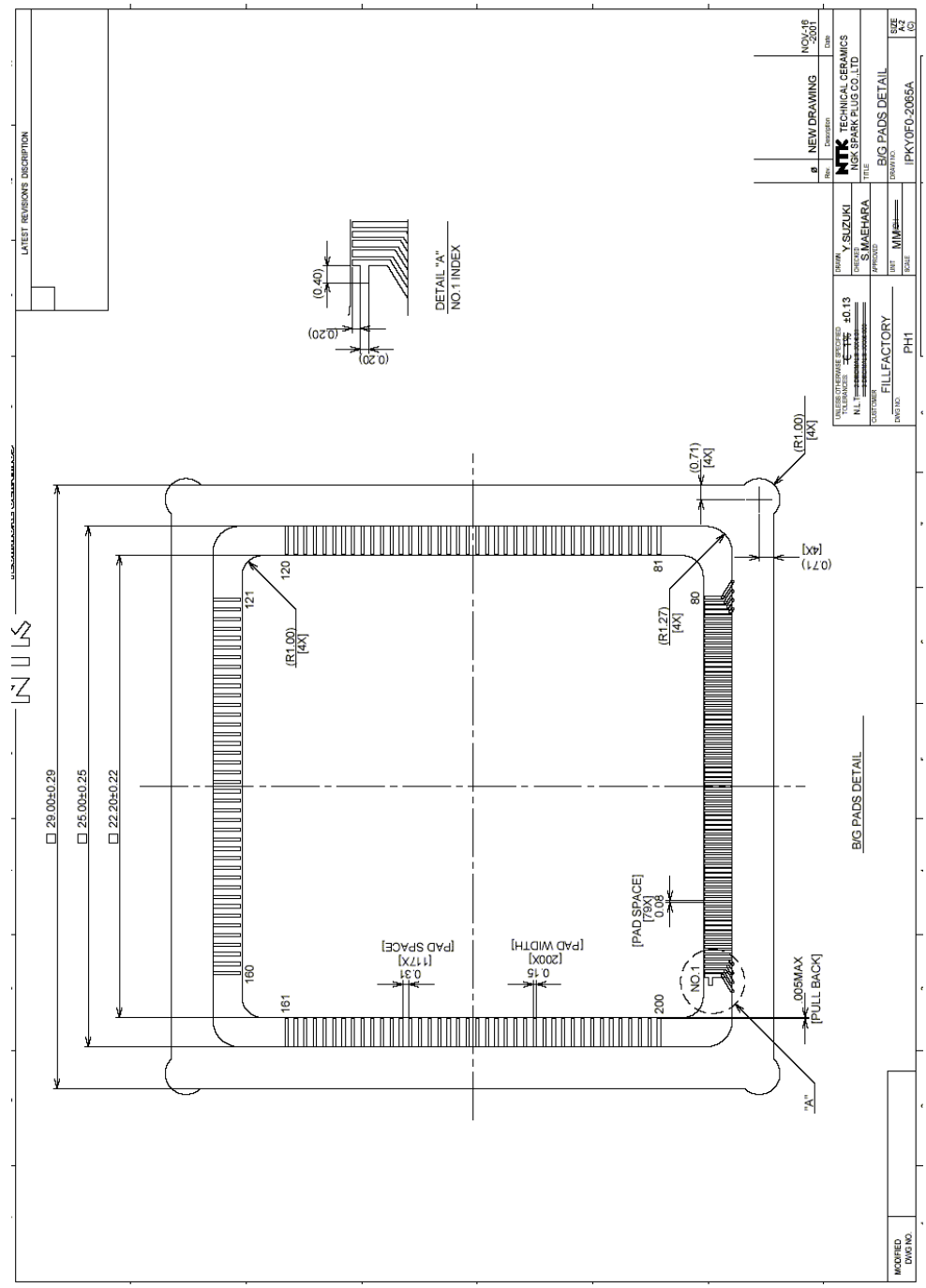
QCFP-160

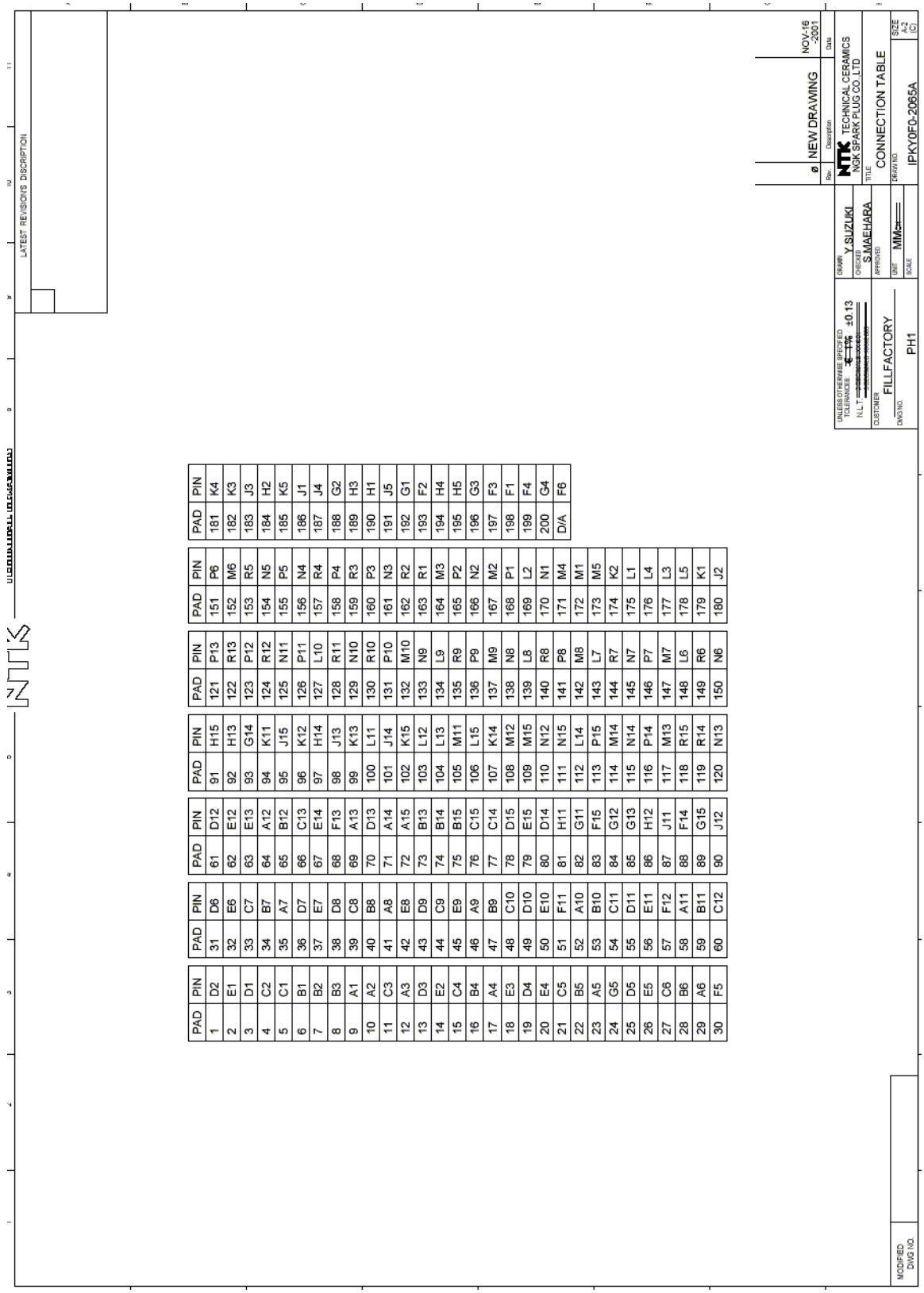



CONFIDENTIAL
all dimensions in mm
sheet: 2/2
scale:
drawning date 21/06/2002
IRIS3 pad layout QFP160 V1.3
DESIGNED Jan Vlummens
proSys
Fillfactory image sensors
PIN80
PIN81
PIN41
PIN40
PIN120
PIN121
PIN1
PIN160
0,490
0,240
note : for all pad numbers the pitch is 490µ (pad width 240µ, pad spacing 250µ) and centered


A
B
0,35
0,30
q17,00
0,076
0,076
pin 1 identification
A'

PGA-201


B/G PADS DETAIL
DETAIL "A"
NO.1 INDEX
NEW DRAWING
TECHNICAL CERAMICS
NGK SPARK PLUG CO.,LTD
FILLFACTORY
PH1
IPKY0F0-2065A
29.00±0.29
25.00±0.25
22.20±0.22
[PAD SPACE]
[PAD WIDTH]
NO.1
.005MAX
[PULL BACK]
"A"



PAD	PIN
1	D2
2	E1
3	D1
4	C2
5	C1
6	B1
7	B2
8	B3
9	A1
10	A2
11	C3
12	A3
13	D3
14	E2
15	C4
16	B4
17	A4
18	E3
19	D4
20	E4
21	C5
22	B5
23	A5
24	G5
25	D5
26	E5
27	C6
28	B6
29	A6
30	F5

PAD	PIN
31	D6
32	E6
33	C7
34	B7
35	A7
36	D7
37	E7
38	D8
39	C8
40	B8
41	A8
42	E8
43	D9
44	C9
45	E9
46	A9
47	B9
48	C10
49	D10
50	E10
51	F11
52	A10
53	B10
54	C11
55	D11
56	E11
57	F12
58	A11
59	B11
60	C12

PAD	PIN
61	D12
62	E12
63	E13
64	A12
65	B12
66	C13
67	E14
68	F13
69	A13
70	D13
71	A14
72	A15
73	B13
74	B14
75	B15
76	C15
77	C14
78	D15
79	E15
80	D14
81	H11
82	G11
83	F15
84	G12
85	G13
86	H12
87	J11
88	F14
89	G15
90	J12

PAD	PIN
91	H15
92	H13
93	G14
94	K11
95	J15
96	K12
97	H14
98	J13
99	K13
100	L11
101	J14
102	K15
103	L12
104	L13
105	M11
106	L15
107	K14
108	M12
109	M15
110	N12
111	N15
112	L14
113	P15
114	M14
115	N14
116	P14
117	M13
118	R15
119	R14
120	N13

PAD	PIN
121	P13
122	R13
123	P12
124	R12
125	N11
126	P11
127	L10
128	R11
129	N10
130	R10
131	P10
132	M10
133	N9
134	L9
135	R9
136	P9
137	M9
138	N8
139	L8
140	R8
141	P8
142	M8
143	L7
144	R7
145	N7
146	P7
147	M7
148	L6
149	R6
150	N6

PAD	PIN
151	P6
152	M6
153	R5
154	N5
155	P5
156	N4
157	R4
158	P4
159	R3
160	P3
161	N3
162	R2
163	R1
164	M3
165	P2
166	N2
167	M2
168	P1
169	L2
170	N1
171	M4
172	M1
173	M5
174	K2
175	L1
176	L4
177	L3
178	L5
179	K1
180	J2

PAD	PIN
181	K4
182	K3
183	J3
184	H2
185	K5
186	J1
187	J4
188	G2
189	H3
190	H1
191	J5
192	G1
193	F2
194	H4
195	H5
196	G3
197	F3
198	F1
199	F4
200	G4
D/A	F6

NEW DRAWING — NOV-16-2001

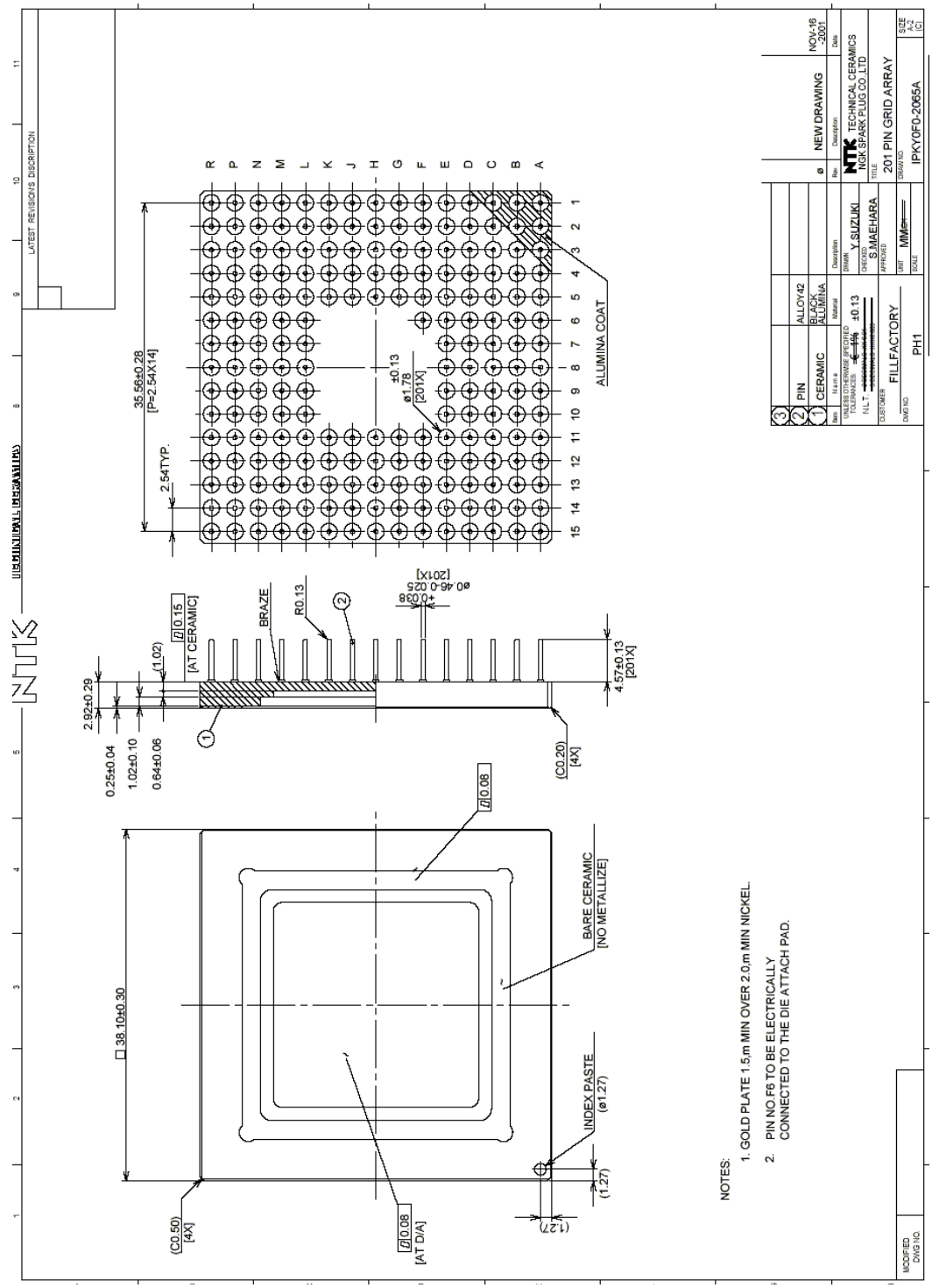
NTK TECHNICAL CERAMICS NGK SPARK PLUG CO.,LTD

CONNECTION TABLE

IPKY0F0-2065A

FILLFACTORY

PH1


NOTES:
1. GOLD PLATE 1.5μm MIN OVER 2.0μm MIN NICKEL.
2. PIN NO.F8 TO BE ELECTRICALLY CONNECTED TO THE DIE ATTACH PAD.
ALUMINA COAT
BRAZE
BARE CERAMIC [NO METALLIZE]
INDEX PASTE (ø1.27)
35.56±0.28 [P=2.54X14]
2.54TYP.
38.10±0.30
4.57±0.13 [201X]
2.92±0.29
0.25±0.04
1.02±0.10
0.64±0.06
(1.02)
(C0.20) [4X]
(C0.50) [4X]
(1.27)
NEW DRAWING
NOV-16-2001
TECHNICAL CERAMICS
NGK SPARK PLUG CO.,LTD
201 PIN GRID ARRAY
IPKY0F0-2065A
FILLFACTORY
PH1
Y.SUZUKI
S.MAEHARA
PIN
CERAMIC
ALLOY42
BLACK ALUMINA

3.2.2 Pin list

Pin types:

AI Analogue input

AO Analogue output

DI Digital input

DO Digital ouput

DIO Digital bidirectional

DOZ Digital output or high-impedant

DIOZ Digital bidirectional or high-impedant

CQFP160 package, starting BOTTOM LEFT, working COUNTERCLOCKWISE

pin	pad	name	remarks
1			
2			
3	DIO	D_DOUT1	Output data (also parallel command input)
4	DIO	D_DOUT2	
5	DIO	D_DOUT3	
6	DO	D_PACKET	Data packet present
7	DO	D_PACKETb	Inverted D_PACKET
8	DI	D_READY	Ready for transmission
9	DI	CLK	20 or 25MHz clock, 50% duty cycle
10	DOZ	RAM_CKE	Masks RAM_CLK clock to freeze operation from the next clock cycle. RAM_CKE should be enabled at least one cycle prior to new SDRAM command.
11		VDD_DIG	3.3V logic supply
12		GND_DIG	logic ground

13	DOZ	RAM_CS0b	Enable RAM chip 0, disables or enables SDRAM device operation by masking enabling all inputs except RAM_CLK, RAM_CKE, and RAM_DQM, 50kΩ to power
14	DOZ	RAM_CS1b	Enable RAM chip 1, disables or enables SDRAM device operation by masking enabling all inputs except RAM_CLK, RAM_CKE, and RAM_DQM, 50kΩ to power
15	DIOZ	RAM_D0	Data from/to SDRAM bank, distributed over two 8 bit blocks ([0] is LSB). When only one block is installed (see MEM_CFG) only RAM_D[7..0] is used.
16	DIOZ	RAM_D1	
17	DIOZ	RAM_D2	
18	DIOZ	RAM_D3	
19	DIOZ	RAM_D4	
20	DIOZ	RAM_D5	
21	DIOZ	RAM_D6	
22	DIOZ	RAM_D7	MSB when 8 bit memory used.
23		RAM_WRb	Enables write operation and row precharge; latches data in starting from CASb, WEb active
24		RAM_DQM	Data input/output mask: makes data output hi-Z, t_{SHZ} after the clock and masks the output; blocks data input when DQM active.
25	DOZ	RAM_RASb	Row address strobe: latches row addresses on the positive going edge of RAM_CLK with RASb low; enables row access and precharge
26	DOZ	RAM_CASb	Column address strobe: latches column addresses on the positive going edge of RAM_CLK with CASb low, enables column address.
27	DOZ	RAM_CLOCK	System clock as fed to SDRAM, connect with 50kΩ to ground
28	DOZ	RAM_BA1	Bank address: selects bank to be activated during row address latch time, and selects bank for read/write during column address latch time. MSB.
29	DOZ	RAM_BA0	LSB.

30		VDD_DIG	3.3V logic supply
31		GND_DIG	logic ground
32	DIOZ	RAM_D8	
33	DIOZ	RAM_D9	
34	DIOZ	RAM_D10	
35	DIOZ	RAM_D11	
36	DIOZ	RAM_D12	
37	DIOZ	RAM_D13	
38	DIOZ	RAM_D14	
39			
40			
41			
42			
43	DIOZ	RAM_D15	MSB when 16 bit memory used.
44	DOZ	RAM_A0	Row address RA[12..0], column address CA[9..0] ([0] is LSB)
45	DOZ	RAM_A1	
46	DOZ	RAM_A2	
47	DOZ	RAM_A3	
48	DOZ	RAM_A4	
49	DOZ	RAM_A5	
50	DOZ	RAM_A6	
51	DOZ	RAM_A7	
52	DOZ	RAM_A8	
53		GND_DIG_IO	IO ground
54		VDD_DIG_IO	3.3V IO supply
55		NC	not connected
56	AO	AOUT	analogue test output; do not connect in normal use; very short trace to test point otherwise
57		GND_ADC_ANA	ADC analogue ground
58		VDD_ADC_ANA	5V ADC analogue supply
59		VDD_ADC_DIG	5V ADC digital supply
60		VDD_DIG_OUT	3.3V sensor logic level shifters, 3.3V, connect to VDD_DIG
61		GND_ADC_DIG	ADC digital ground
62	DOZ	RAM_A9	
63	DOZ	RAM_A10	
64	DOZ	RAM_A11	
65	DOZ	RAM_A12	
66	AI	PBIASDIG2	connect with 100K to GND_ADC_DIG and decouple to VDD_ADC_DIG
67	AI	VHIGH_ADC	Upper reference voltage for ADC, see section 3.2.3. Connect with a resistor to VDD_ADC_ANA and

			decouple to GND_ADC_ANA.
68	AI	NBIASARR	Connect with 1 MEG to VDD_ANA and decouple to GND_ANA with 100 nF
69	AI	BLACKREF	Control voltage for output signal offset level Generate the reference level with a 100k resistor devider.
70	AI	PBIAS	Connect with 40K to ground and decouple to VDD_ANA with 100 nF
71	AI	NBIAS_AMP	Output amplifier speed/power control Connect with 80K to VDD_ANA and decouple with 100 nF to GND_ANA for 12.5 MHz output rate.
72	AI	AIN1	telesense input to ADC, via unity-gain buffer. See section 3.2.3.
73		VDD_ANA	5V analogue sensor supply
74		GND_ANA	analogue sensor ground
75	DI	MEM_CFG0	strap
76	DI	MEM_CFG1	strap
77	DI	RAM_SLAVERDY	Slave currently not accessing RAM, 50k pull-up to VDD.
78	DO	RAM_GRANT	RAM access granted to slave device
79			
80			
81			
82			
83		GND_DIG_2	sensor digital ground
84		VDD_DIG_2	5V sensor digital supply
85	DI	DATAPAC	strap
86	DI	DL_EDAC	strap
87	DI	LSEG1	strap
88	DI	LSEG0	strap
89	DI	APIDMSB3	strap
90	DI	APIDMSB2	strap
91	DI	APIDMSB1	strap
92	DI	APIDMSB0	strap
93	DI	EXP3	strap
94	DI	EXP2	strap
95	DI	EXP1	strap
96	DI	EXP0	strap
97	DI	PERIOD2	strap
98	DI	PERIOD1	strap
99	DI	PERIOD0	strap
100	DI	DELAY2	strap

101	DI	DELAY1	strap
102	DI	DELAY0	strap
103	DI	CONFIG3	strap
104	DI	CONFIG2	strap
105	DI	CONFIG1	strap
106	DI	CONFIG0	strap
107	DI	RC0	remote control output, e.g. to LED
108	DI	RC1	remote
109	DI	RC2	remote
110	DI	RC3	remote
111	DI	RC4	remote
112	DI	RC5	remote
113	AI	GND_ANA	sensor analogue ground
114	AI	G_AB	Anti-blooming sink. Connect to GND or connect to low-impedant 1V level for enhanced anti-blooming.
115	AI	DSREF	Dual slope reference, connect to 4.3V.
116		VDD_RESR	5Vsensor analogue supply, tie to VDD_ANA
117	DI	CMD_IF0	strap
118		CMD_IF1	strap
119			
120			
121			
122			
123	DI	CMD_RATE0	strap
124	DI	CMD_RATE1	strap
125	DI	DATA_IF0	strap
126	DI	DATA_IF1	strap
127	DI	DATA_RATE0	strap
128	DI	DATA_RATE1	strap
129	DO	D_FRAME	Frame strobe
130	DO	D_LINE	Line strobe
131	DI	TRIG	trigger
132	DI	RSTb	reset
133	DI	C_RTS	Telecommand packet valid
134	DO	C_CTS	Clear to send
135	DI	C_DCLK	Serial data bit clock
136	DI	C_DIN	Serial command input
137	DI	C_ADT	Abort command transfer
138	DI	C_DIRECTb	Make D_DOUT[0..7] direct command inputs
139		GND_ANA	sensor analogue ground
140		VDD_ANA	5V sensor analogue supply
141		GND_DIG_2	sensor digital ground
142		VDD_DIG_2	5V sensor digital supply
143		XMUXNBIAS	Connect with 100k to VDD ANA and decouple to

			GND_ANA.
144		NBIASANA	connect with 100K to GND_ANA and decouple to GND_ANA
145		NBIASANA2	connect with 100K to VDD_ANA and decouple to GND_ANA
146		VLOW_ADC	Lower reference voltage for ADC, see section 3.2.3. Connect with a resistor to GND and decouple to GND.
147		GND_DIG_IO	IO ground
148		VDD_DIG_IO	3.3V IO supply
149	DIO	D_DOUT4	
150	DIO	D_DOUT5	
151	DIO	D_DOUT6	
152	DIO	D_DOUT7	
153	DO	D_DOUT8	
154	DO	D_DOUT9	Output data LSB, or serial output
155	DO	D_DBCLK	Serial data bit clock or 25MHz system clock
156	DO	D_DCLK	Output data word clock or pixel strobe
157	DO	D_DCLKb	Inverted D_DCLK
158	DIO	D_DOUT0	
159			
160			

Analogue and digital/logic ground planes must be tied together at one single point on the board. All supply pins must be decoupled with 100nF to their nearest corresponding ground.

Separately-fed power supply domains must be protected from latch-up with anti-parallel diodes between each two domains.

PGA201 package, starting BOTTOM LEFT, working COUNTERCLOCKWISE

note: the 201st pin is not connectable on the package.

pin	pad	name	remarks
1			
2			
3			
4			
5		D_DOUT1	
6			
7		D_DOUT2	
8			
9		D_DOUT3	
10			
11		D_PACKET	
12			
13		D_PACKETb	
14			
15		D_READY	
16			
17		CLK	
18			
19		RAM_CKE	
20			
21		VDD_DIG	
22			
23		GND_DIG	
24			
25		RAM_CS0b	
26			
27		RAM_CS1b	
28			
29		RAM_D0	
30			
31		RAM_D1	
32			
33		RAM_D2	
34			
35		RAM_D3	
36			

37		RAM_D4	
38			
39		RAM_D5	
40			
41		RAM_D6	
42			
43		RAM_D7	
44			
45		RAM_WRb	
46			
47		RAM_DQM	
48			
49		RAM_RASb	
50			
51		RAM_CASb	
52			
53		RAM_CLOCK	
54			
55		RAM_BA1	
56			
57		RAM_BA0	
58			
59		VDD_DIG	
60			
61		GND_DIG	
62			
63		RAM_D8	
64			
65		RAM_D9	
66			
67		RAM_D10	
68			
69		RAM_D11	
70			
71		RAM_D12	
72			
73		RAM_D13	
74			
75		RAM_D14	
76			
77			
78			
79			
80			

81			
82			
83		RAM_D15	
84		RAM_A0	
85		RAM_A1	
86		RAM_A2	
87		RAM_A3	
88		RAM_A4	
89		RAM_A5	
90		RAM_A6	
91		RAM_A7	
92		RAM_A8	
93		GND_DIG_IO	
94		VDD_DIG_IO	
95		NC	
96		AOUT	
97		GND_ADC_ANA	
98		VDD_ADC_ANA	
99		VDD_ADC_DIG	
100		VDD_DIG_OUT	
101		GND_ADC_DIG	
102		RAM_A9	
103		RAM_A10	
104		RAM_A11	
105		RAM_A12	
106		PBIASDIG2	
107		VHIGH_ADC	
108		NBIASARR	
109		BLACKREF	
110		PBIAS	
111		NBIAS_AMP	
112		AIN1	
113		VDD_ANA	
114		GND_ANA	
115		MEM_CFG0	strap
116		MEM_CFG1	strap
117		RAM_SLAVERDY	
118		RAM_GRANT	
119			
120			
121			
122			
123		GND_DIG_2	
124		VDD_DIG_2	

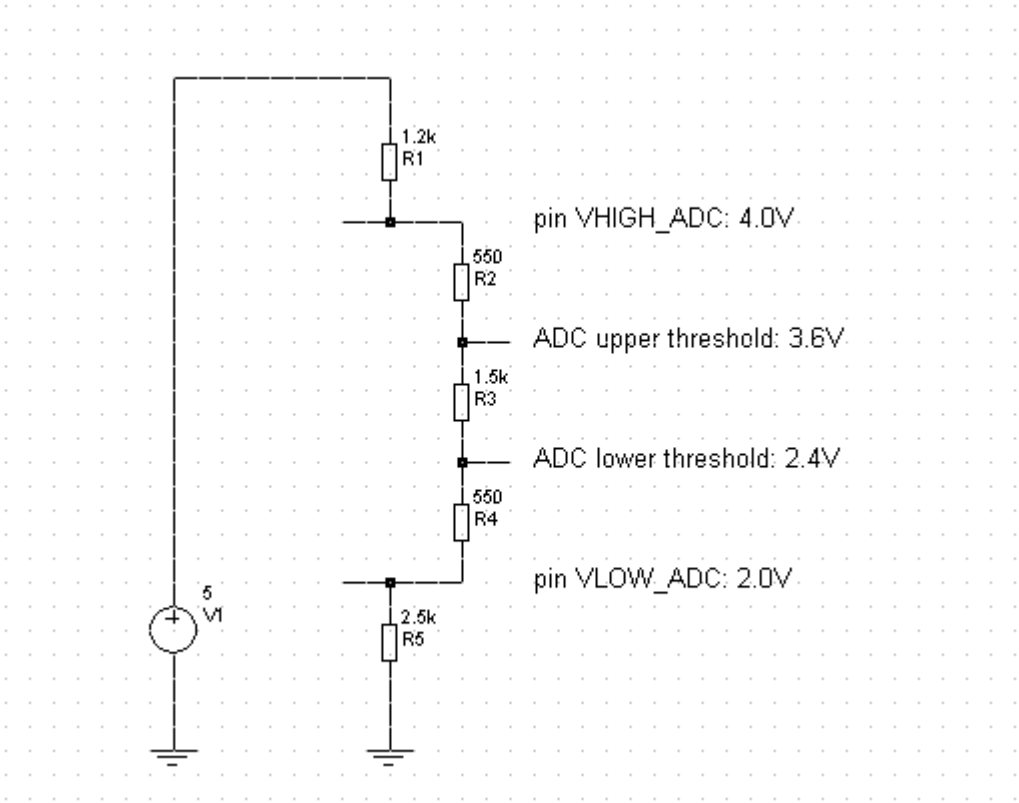
125		DATAPAC	strap
126		DL_EDAC	strap
127		LSEG1	strap
128		LSEG0	strap
129		APIDMSB3	strap
130		APIDMSB2	strap
131		APIDMSB1	strap
132		APIDMSB0	strap
133		EXP3	strap
134		EXP2	strap
135		EXP1	strap
136		EXP0	strap
137		PERIOD2	strap
138		PERIOD1	strap
139		PERIOD0	strap
140		DELAY2	strap
141		DELAY1	strap
142		DELAY0	strap
143		CONFIG3	strap
144		CONFIG2	strap
145		CONFIG1	strap
146		CONFIG0	strap
147		RC0	remote
148		RC1	remote
149		RC2	remote
150		RC3	remote
151		RC4	remote
152		RC5	remote
153		GND_ANA	
154		G_AB	
155		DSREF	
156		VDD_RESR	
157		CMD_IF0	strap
158		CMD_IF1	strap
159			
160			
161			
162			
163		CMD_RATE0	strap
164		CMD_RATE1	strap
165		DATA_IF0	strap
166		DATA_IF1	strap
167		DATA_RATE0	strap
168		DATA_RATE1	strap

169		D_FRAME	
170		D_LINE	
171		TRIG	trigger
172		RSTb	reset
173		C_RTS	
174		C_CTS	
175		C_DCLK	
176		C_DIN	
177		C_ADT	
178		C_DIRECTb	
179		GND_ANA	
180		VDD_ANA	
181		GND_DIG_2	
182		VDD_DIG_2	
183		XMUXNBIAS	
184		NBIASANA	
185		NBIASANA2	
186		VLOW_ADC	
187		GND_DIG_IO	
188		VDD_DIG_IO	
189		D_DOUT4	
190		D_DOUT5	
191		D_DOUT6	
192		D_DOUT7	
193		D_DOUT8	
194		D_DOUT9	
195		D_DBCLK	
196		D_DCLK	
197		D_DCLKb	
198		D_DOUT0	
199			
200			

Analogue and digital/logic ground planes must be tied together at one single point on the board. All supply pins must be decoupled with 100nF to their nearest corresponding ground.

Separately-fed power supply domains must be protected from latch-up with anti-parallel diodes between each two domains.

3.2.3 Adjusting the ADC input window



The ADC's upper and lower acceptance levels are set with a five-element resistive voltage divider, of which two resistors are off-chip (R1, R5), and three resistors are on-chip, the middle one (R3) corresponding to the ADC input window. Above figure gives values for R1 and R5 to attain an ADC input window between 2.4V and 3.6V.

Note that the voltages observed at chip pins VHIGH_ADC and VLOW_ADC do not correspond to the true ADC acceptance window.

3.2.4 Colour mosaic alignment

To be added.

3.3 Electro-optical specification

3.3.1 Nominal operation

Parameters marked * measured on the electro-optically identical STAR1000 sensor.

Nominal supply voltages and biasing, 20 degrees ambient temperature, 25MHz clock frequency, allowed radition dose 30 krad (Si), unless indicated otherwise.

	min.	typ.	max.	remarks
fill factor (FF) x Quantum Efficiency (QE)		25 %		*480-650nm
optical bandwidth		400-900nm		*QE x FF > 5% BG39 filter recommended for VIS imaging
horizontal MTF		0.26		*
vertical MTF		0.37		*
pixel voltage conversion factor		10.4µV/e-		*
pixel saturation charge		120000e-		*
pixel linear range		85000e-		*
analogue output signal swing		1.34V		at unity gain
temporal noise (RMS)	500µv	550µv 53 e-	610µv	
dynamic range		67dB		full range, analogue domain

signal to noise ratio		64dB		linear range
dark current		23 mV/s 2200 e-/s	60 mV/s 6000 e-/s	20 degrees ambient; max values at 30 krad (Si) dose.
dark current at higher temperature		230 mV/s	290 mV/s	55 degrees ambient
static non-uniformity (FPN)		0.57% of full-scale		global
pixel response non-uniformity (PRNU)		3.58% of full-scale		global, at 50% illumination
ADC non-linearity		4 LSB		
ADC missing codes		0		

3.3.2 Gamma radiation degradation

Nominal supply voltages and biasing, 20 degrees ambient temperature, 25MHz clock frequency, allowed radition dose 80 krad (Si).

	min.	typ.	max.	remarks
dark current			110 mV/s 11000 e-/s	due to radiation damage and self-heating

3.3.3 Heavy ion/LU/SEU tolerance

Test setup

Two samples have been tested at the ESA heavy ion facility of the university of Louvain-la-Neuve (UCL) with the following beam configuration:

- cocktail #1
- M/Q = 5
- LET = 1.7 to 56 MeV/mg/cm^2

Ions	*M/Q*	*DUT energy [MeV]*	*Range [µm Si]*	*LET [MeV/mg/cm²]*
^{40}Ar $^{8+}$	5	150	42	14.1
^{84}Kr $^{17+}$	4.94	316	43	34
^{132}Xe $^{26+}$	5.07	459	43	55.9

The beam spot size was 25 mm, focussed on the center of the bare IRIS-3 die, which was therefore fully covered by the ion beam.

Test results

No latchup was seen over the test range of beam flux 10 to 11000 ions/s/cm² with LETs of 14.1 MeV/mg/cm² to 55.9 MeV/mg/cm².

At a beam flux of 10 ions/s/cm² no SEUs were observed. At a beam flux of 100 ions/s/cm², no SEUs were recorded at a fluence of less than 2300 ions/cm² (LET=55.9 MeV/mg/cm²).

3.4 Electrical specification

3.4.1 Signal and supply voltages

	min	typ	max	remarks
'0' logic level in			0.8V	
'1' logic level in	2.0V			
'0'logic level out		0.2V	0.4V	at 4mA
'1' logic level out	2.4V	3.0V		at 4mA
logic IO input current			+/-10µA	
tristate output leakage current			+/-10µA	
input capacitance		2.0pF	4.0pF	
output capacitance		4.0pF		
bidirectional IO capacitance	0.9pF	1.1pF		
logic IO latch-up current	200mA	500mA		
logic IO ESD protection	2000V	4000V		human body model
array analogue output range	2V		3.4V	
ADC analogue input range				see section 3.2.3.
power supply 5V nom.	4.5V	5.0V	5.5V	VDD_RESR should never exceed VDD
power supply 3.3V nom.	2.7V	3.3V	3.6V	
allowerd temperature	-40°C		+60°C	

Note: separately fed power supply domains must be protected from latch-up with anti-parallel diodes between each two domains.

3.4.2 Power consumption up to 30 krad(Si)

Power consumption with a 25MHz chip clock:

- idle: executing no commands, 25MHz
- active: average current when acquiring images, at 25 and 12.5MHz clock rates

power domain	idle 25MHz	active 25MHz	active 12.5MHz	
3.3V logic	49 mA	50 mA	27 mA	
5V logic	5 mA	45 mA	15 mA	
5V analogue	61 mA	45 mA	42 mA	
	482 mW	616 mW	374 mW	

The device should not be powered for long times (e.g. tens of seconds) without a clock signal present.

3.4.3 Power consumption up to 80 krad(Si)

power domain	idle 25MHz			
3.3V logic	230 mA			
5V logic	37 mA			
5V analogue	61 mA			
	1250 mW			

The device should not be powered for long times at an accumulated dose over 30 krad(Si).

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