STARS-3: Fully Integrated Communication Terminal and Equipment: Image Compression Camera

Work Package 2300: **IRIS Characterization and Evaluation**

IRIS-3 Characterization Report

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Authors	:	Thys Cronje
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ESTEC Technical Management: R. Weigand

Review list

name	Date
Werner Ogiers (FillFactory)	2003-03-11
Jean Roggen (IMEC)	2003-03-12

Distribution list

ESA – ESTEC: R. Weigand (TOS-ESM)

IMEC: Ch. Van Hoof (MCP)
T.Cronje (MCP)
J. Roggen (BD)

FillFactory W.Ogiers (Digital ASICs)

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Purpose

The purpose of this document is to report on the electro-optical evaluation of the CMOS active pixel sensor that was custom designed for the STARS-3 project. (ESTEC contract 13716/99/NL/FB)

Scope.

This document reports on the electro-optical of the devices that was performed in the scope of the STARS-3 project. It contains a description of the tests and the test conditions and an overview of the measurement results.

The Electro-optical evaluation comprises two phases: the establishment of the bias- and operating conditions and the electro optical evaluation to confirm the electro optical specifications.

The results of the radiation tests that were also foreseen in the contract are compiled in a separate document.

Abbreviations and acronyms

AC	Alternating Current
ADC	Analogue to Digital Converter
ADU	ADC unit: least significant bit
DC	Direct Current
FPN	Fixed Pattern Noise
FS	Full Scale
GND	Ground
IRIS	Integrated Radiation-tolerant Imaging System 3
LCDSS	Low Cost Digital Sun Sensor
MTF	Modulation Transfer Function
PRNU	Photo response Non Uniformity
VDD	Power supply voltage

Reference:

[RD1] LCDSSOG-FF-DL-2001-001 Electro-optical evaluation report for CMOS APS, Version 1, October 27, 2001

Applicable Documents

[AD1] Total Dose Steady-State Irradiation Test Method, ESA/SCC Basic Specification No.22900, Issue 4, April 1995

[AD2] Single Event Effects Test Method and Guidelines, ESA/SCC Basic Specification No.25100, Issue 1, October 1995

[AD3] IMEC P50314-IM-DL-0005 IRIS-3 Imager Test and Validation Plan, Draft Issue 0.4 March 5, 2001

1.Introduction

During the design phase, the specifications of the IRIS-3 image sensor were predicted, based upon experience and upon simulations wherever possible. However, assessment of the specifications implies production and measurement on real devices. This document reports on the electro-optical measurements that were made on the produced devices to verify and assess their performance.

2.Overview of tests

The following list contains the electro-optical and functional test flow of the IRIS-3 image sensor samples.

- Dicing and packaging of first samples
- Operation and establishment of bias conditions
- Electro-optical evaluation of samples from the production run.
- Functional testing of digital core.

3.Operation and establishment of bias conditions

2.1.1 Procedure

After production one wafer is diced and ten devices were packaged in a 201 pin PGA package and sealed with a glass window. One of the packaged devices was plugged into the test system and the test system is debugged such that the device can operate at nominal conditions. When the device was operational, the bias conditions were varied to find the optimal setting.

2.1.2 Measurement results

The establishment of bias conditions resulted in the list in Table 1 of advised bias settings and components. The resistor values were chosen such that they comply with available values in standard resistance ranges.

Table 1: Bias conditions

Pin name	Measured voltage	Description
XMUXNBIAS	0.001	Connect with 100K to GND
NBIAS_AMP	1.161	Output amplifier speed/power control Connect with 75K to VDD and decouple with 100 nF to GND for 12.5 MHz output rate. (lower resistor values yield higher maximal pixel rates at the cost of extra power dissipation)
PBIAS	3.623	Connect with 39K to ground and decouple to Vdd by 100 nF capacitor for 12.5 MHz pixel rate. (Lower resistor values yield higher maximal pixel rates at the cost of extra power dissipation)
BLACKREF	2.46	Control voltage for output signal offset level Buffered on-chip, the reference level can be generated by a 100K resistive divider. Connect to 2 V DC for use with on-chip ADC
NBIASARR	0.757	Connect with 1 MEG to Vdd and decouple to ground by 100 nF capacitor
NBIASANA	1.083	Connect with 100K to VDD and decouple to GND
NBIASANA2	1.082	Connect with 100K to VDD and decouple to GND
VLOW_ADC	2.062	Low- and high reference voltages of ADC. Nominal input range is between 2V and 4V, to be fine-tuned when working samples are available. The resistance between VLOW_ADC and VHIGH_ADC is about 2.6 K. The required voltage settings on VLOW_ADC and VHIGH_ADC can be approximated by tying VLOW_ADC with 2.7 K to GND and VHIGH_ADC with 1.2 K to VDD
PBIASDIG2	3.606	Connect with 100K to GND and couple to VDD
VHIGH_ADC	4.101	Low- and high reference voltages of ADC. Nominal input range is between 2V and 4V, to be fine-tuned when working samples are available. The resistance between VLOW_ADC and VHIGH_ADC is about 2.6 K. The required voltage settings on VLOW_ADC and VHIGH_ADC can be approximated by tying VLOW_ADC with 2.7 K to GND and VHIGH_ADC with 1.2 K to VDD
G_AB	0.010	Anti-blooming drain control voltage: Default: connect to ground. The anti-blooming is operational but not maximal Apply 1 V DC for improved anti-blooming
VREF	5.00	Reset level for RESET_DS: 5V DC Apply different voltage for extended dynamic range
DSREF	4.30	Connected with 100K to GND and with diode to VDD

An additional 1.1kohm internal resistance was observed in the ADC ladder path, shifting the VLOW and VHIGH values accordingly. When calculating the external resistance values for biasing an internal resistance of 0.5kohm must be added to the top and bottom of the ladder for the correct calculation of the biasing voltages.

3 Electro-optical evaluation

The electro-optical evaluation of the samples comprises the tests that are needed to confirm the device specifications. Table 2 lists the measurements and indicates on how many samples these measurements were performed.

Table 2: Electro-optical measurement overview

Measurement	Test sample	Comment
Spectral response	2 test structure of 2 devices	Spectral response measurement yields calculation of quantum efficiency
Photo-voltaic response	1 pixel on 3 devices	Enables calculation of saturation level, linearity, diode capacitance and voltage conversion factor.
Output amplifier gain	4 pixels on 3 devices	Measurement of relative gain versus setting “00”
Pixel profile	On 1 pixel on 3 devices in both horizontal and vertical direction	Allows calculation of MTF
Dark current	On 4 pixels of 3 devices	
FPN	On 3 devices	
DCNU	On 3 devices	
PRNU	On 3 devices	
Noise	On 5 pixels of 3 devices	
Power	On each kind of power supply line of 3 devices	
Output amplifier DC response	On 3 devices	Measurement only at unity gain
Output amplifier gain/phase diagram	On 3 devices	Measurement at unity gain, allows calculation off –3dB frequency
ADC minimum set-up time	On 3 devices	
ADC missing codes	On 3 devices	
ADC linearity	On 3 devices	

3.1 Spectral response and quantum efficiency

The results of the spectral response measurements are normally obtained from the two test structures on two devices. The first test structure is a plain photo diode with an area that is equal to an array of 20 x 35 pixels. The second test structure consists of an array of 20 x 35 pixels with all photodiodes connected in parallel and made externally. This structure allows measuring the photon-generated current in the pixel directly.

Due to the fact that these structures does not exist on the IRIS-3 sensor, these measurements were not done, but was copied from a device (LCDSS, RD1) with identical pixels and analogue signal path that showed no spread in production. See Figure 1 for the spectral response.

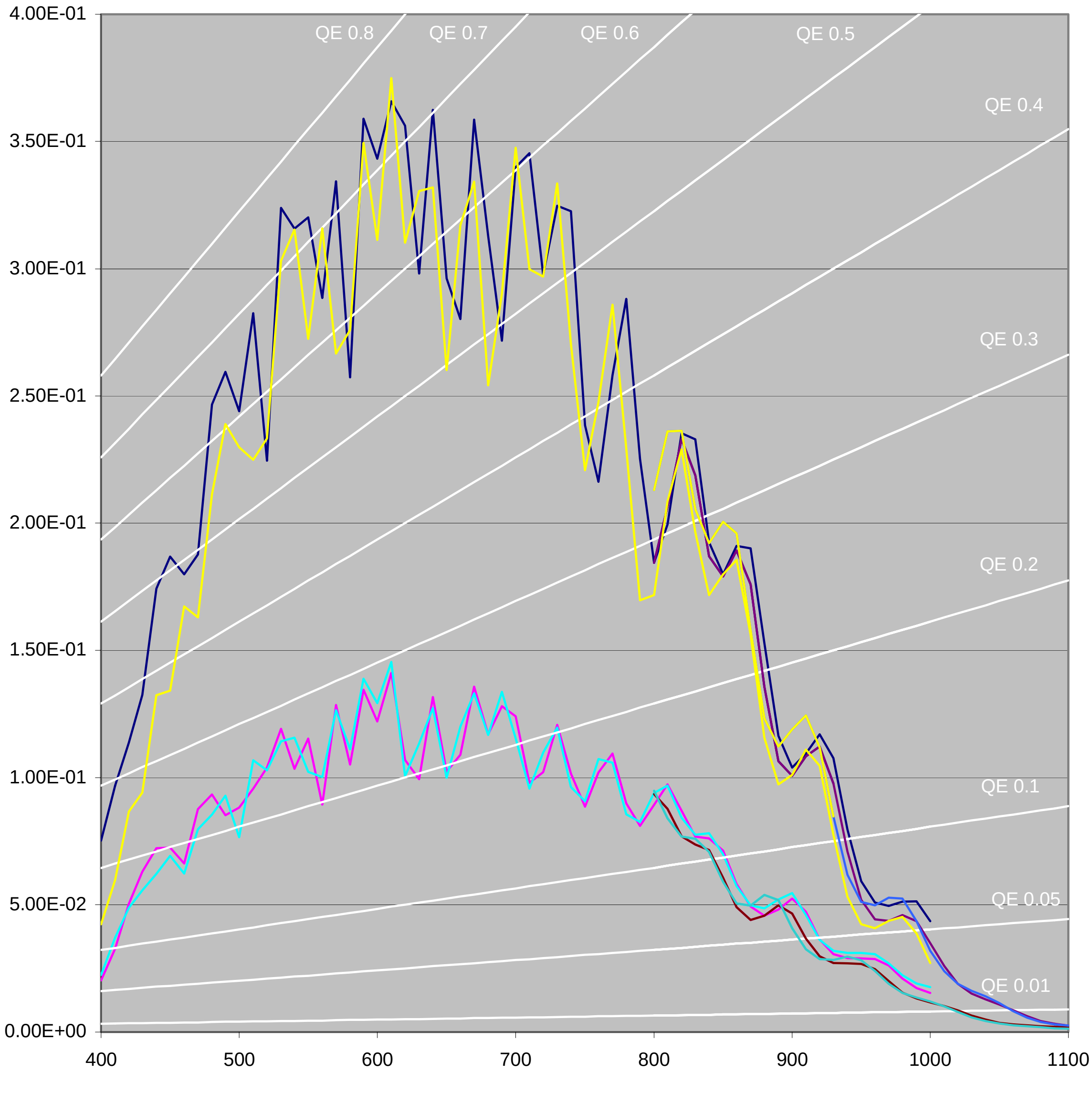

Figure 1: Spectral response measurement results as obtained with LCDSS sensor [RD1].

In Figure 1 the photoresponse (A/W) is plotted against spectral wavelength (nm). The top two traces are the photoresponse of full-area diodes on two test chips, 100% fillfactor and the bottom traces are the photoresponse of two samples of LCDSS chips.

3.2 Photo Voltaic Response

The photovoltaic response measurement yields the voltage output of a device as function of the illumination power. From this curve, the linear range and the saturation capacity can be calculated.

The results as obtained from the LCDSS sensor [RD1] was used due to the similarity in imaging cores.

Output Voltage Swing [V]	**Voltage Conversion factor [µV/e-]**	**Saturation Charge [e-]**	**+/- 1% linearity charge [e-]**
1.278V	10.43	121 550	84533

Table 3: Saturation charge, linear response and voltage conversion factor.

The gains given in Table 4 are all relative to "Gain 00", taken as 1.00. These measurements were obtained from LCDSS/STAR1000 data [RD1].

Gain 00	**Gain 01**	**Gain 10**	**Gain 11**
1.00	2.47	4.59	8.64

Table 4: Relative gain settings.

3.3 Pixel Profile

The pixel profile measurement yields the calculation of the Modulation Transfer Function (MTF) value at Nyquist pixel repetition frequency. Table 5 shows the measured MTF values for the LCDSS sensor, identical to the IRIS-3 FPA.

Horizontal MTF	Vertical MTF
0.26	0.37

Table 5: LCDSS MTF results [RD1].

To correlate these results with IRIS-3 images, a black square on white paper was photographed with both the IRIS-3 and LCDSS imagers. Figure 2 and Figure 3 shows the respective transitions from white to black of the black square on white paper imaged with both LCDSS and IRIS-3. No degradation is visible.

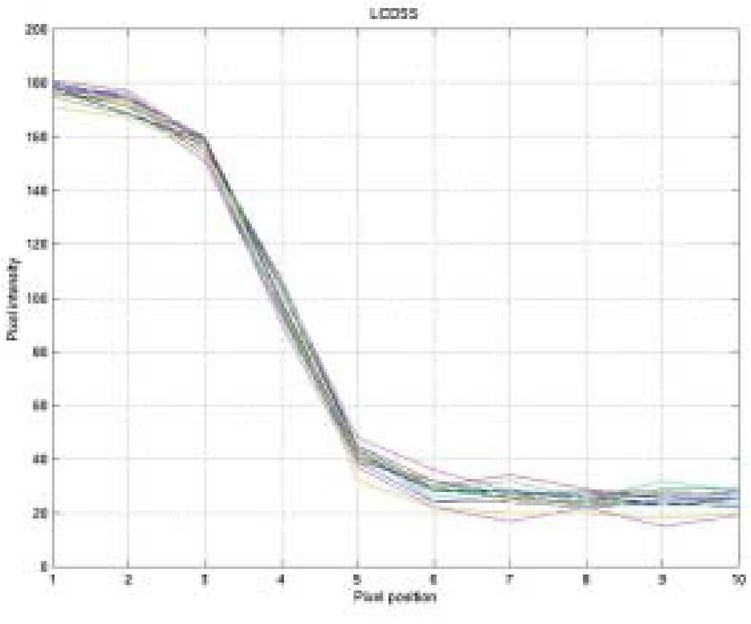

Figure 2: Pixel intensities for white to black transition on LCDSS sensor.

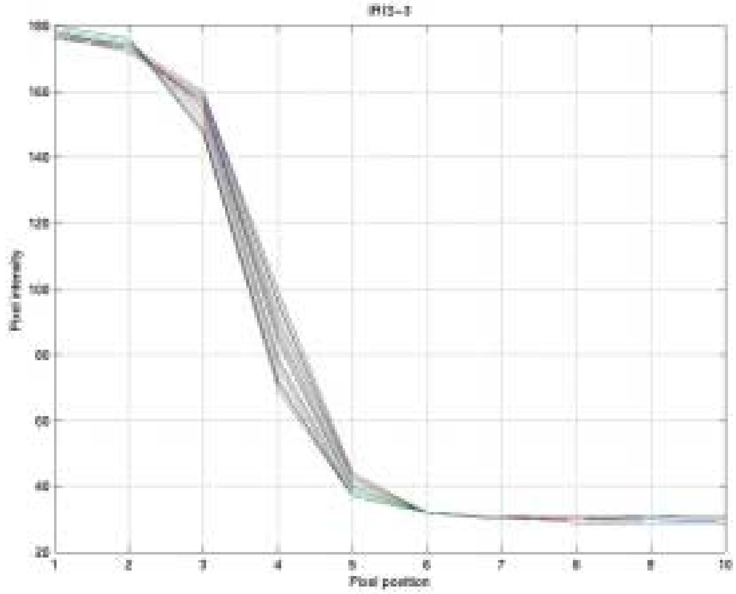

Figure 3: Pixel intensities for white to black transition on IRIS-3 sensor.

3.4 Number of Defective Pixels

Determining the number of defective pixels in a FPA.

3.4.1 Procedure

To count the number of defective pixels the image array is illuminated with a uniform white light source. An image is taken and each pixel value is compared with the average value of all pixels in the array.

A pixel is considered dark or bright if it falls outside predefined limits around the average value. Typically these limits are set to ±20% of the average value.

3.4.2 Measurement Results

No defective pixels were found in the three devices tested.

3.5 Non-uniformity: FPN, DCNU and PRNU

3.5.1 Procedure

To measure the Fixed Pattern Noise (FPN) images are stored without any illumination and zero exposure. Pixels with a value that is brighter than 20% of the saturation value are discarded. The global FPN is defined as the RMS value of the detector; the local FPN is defined as the average RMS value of all 3-by-3 pixel tiles of the array.

To measure the Dark Current Non-Uniformity (DCNU) images are stored without any illumination but a long exposure (24 frames in over-exposure mode). Pixels with a value that is darker or brighter than 20% of the average value are discarded. The global DCNU is defined as the RMS value of the detector; the local DCNU is defined as the average RMS value of all 3-by-3 pixel tiles of the array.

The Photo Response Non Uniformity was measured by illuminating the image sensor with a uniform DC powered lamp such that the output signal was at about 50% of saturation. An image was taken and stored with this illumination. The global PRNU is calculated as the RMS value of all pixels of the detector; the local PRNU is calculated as the average RMS value of all 3-by-3 pixel tiles of the array.

3.5.2 Measurement Results

Device	**Local FPN [% of FS]**	**Global FPN [% of FS]**	**Local DCNU [% of FS]**	**Global DCNU [% of FS]**	**Local PRNU [% of sig]**	**Global PRNU [% of sig.]**
1A	0.089	0.55	0.65	1.85	0.64	4.24
1B	0.092	0.53	0.68	1.67	0.54	2.73
1C	0.094	0.63	0.53	1.49	0.55	3.49
Average	**0.092**	**0.57**	**0.62**	**1.67**	**0.57**	**3.48**

Table 6: FPN, DCNU and PRNU measurement results.

3.6 Noise

The noise level and saturation charge allow the calculation of the dynamic range of the detector.

3.6.1 Procedure

On four selected pixels, the output voltage is sampled 125 times using an oscilloscope. The noise level is the RMS of the sampled values.

The output amplifier is set to mode "01" to enable better detection of the noise signal. In the calculation the average gain at this setting is taken into consideration.

3.6.2 Measurement Results

Table 7 lists the results of the noise measurements on 4 pixels for three devices. The average dark voltage was measured as 2.04V and the saturation voltage as 3.38V and the gain at setting "00" as 1.00. For the dynamic range a total voltage swing of 1.34V was used.

Device ID: Pixel	Noise [uV]	Noise [e-]	Dynamic Range
1A: (256,256)	526	50	2545
1A: (768,256)	530	50	2525
1A: (256,512)	534	51	2506
1A: (768,512)	543	52	2467
1B: (256,256)	497	47	2693
1B: (768,256)	611	58	2192
1B: (256,512)	549	52	2442
1B: (768,512)	524	50	2555
1C: (256,256)	587	56	2284
1C: (768,256)	558	53	2402
1C: (256,512)	560	53	2391
1C: (768,512)	548	52	2444
Average	**547**	**52**	**2454 (-67.8dB)**
Maximum	**611**	**58**	**2192 (-66.8dB)**
Minimum	**497**	**47**	**2693 (-68.6dB)**

Table 7: Noise measurement results

These results are worse than measured on the LCDSS device and could be attributed to the large amount of logic on chip, but is not correlated to any clock signals.

3.7 Dark Current

The dark current of the sensor is measured on selected pixels for different devices.

3.7.1 Procedure

The dark current level is defined by measuring the dark output voltage of selected pixels at different integration times.

The dark current is the ratio between the voltage difference and the integration time difference for the readings. These differences can also be expressed in number of electrons per second or current per area. These figures are calculated as follows:

$$V_{dark} = \frac{V_{out}}{T_{\text{int}}}$$

V_{dark} : Dark signal [V/s]

V_{out} : Output voltage difference due to dark current [V]

T_{int} : Integration time difference [s]

$$\#e-_{dark} = \frac{V_{dark}}{F_v}$$

$\#e-_{dark}$: Dark signal expressed as [Number electrons / s]

V_{dark} : Dark signal in [V/s]

F_v : Voltage conversion factor: 10.43µV/e-

$$I_{dark} = \frac{\#e-_{dark} * Q_{e-}}{A_{pix}}$$

I_{dark} : Dark current signal, expressed as current per area [A/cm2]

$\#e-_{dark}$: Dark signal expressed as [Number electrons / s]

Q_{e-} : Electron charge: 1.6 E-19 [C/e-]

A_{pix} : Pixel area [cm2]

3.7.2 Measurement results:

The dark current was calculated from the results of taking images at different exposure times and room temperature, 23^{o}C.

Device ID: Pixel	Dark Current: mV/s	Dark Current: e-/s	Dark Current: pA/cm^2
1A (256, 256)	30.7	2943	209
1A (768, 256)	21.6	2070	147
1A (256, 512)	27.3	2617	186
1A (768, 512)	9.86	945	67
1B (256, 256)	34.6	3317	235
1B (768, 256)	18.8	1802	128
1B (256, 512)	33.0	3164	225
1B (768, 512)	10.8	1035	73
1C (256,256)	26.5	2540	180
1C (768, 256)	12.5	1198	85
1C (256, 512)	38.6	3700	263
1C (768, 512)	9.43	904	64
Average	**22.8**	**2186**	**155**
Maximum	**38.6**	**3700**	**263**
Minimum	**9.43**	**904**	**64**

Table 8: Calculated dark currents.

In Table 8 a summary of the calculated and measured dark currents are given expressed as mV/s (dark signal), -e/s and pA/cm^2. The voltage conversion factor as measured on the LCDSS device was used.

3.8 Power consumption

The power supply current to the different parts of the image sensor is measured separately.

3.8.1 Procedure

The device-specific test board of the IRIS-3 system contains a provision to separately measure the supply current to the different kinds of power supply lines. The following currents are measured:

Idda_5: Supply current to the analogue part of the FPA sensor core
Iddd_5: Supply current to the digital part of the FPA sensor
Iddd_33: Supply current to the digital part of the imager core: sequencer, Rx/Tx, Memory IF

The power for measured under the following conditions:

- With no clock signal provided
- Idle mode, directly after start-up - no image acquisition (25MHz).
- During image acquisition the peak and mean currents were measured (25MHz).
- Repeated for 12.5MHz.

3.8.2 Measurement results:

Table 9 shows the power consumption with no input clock, thus for the default start-up conditions. These conditions are unknown when no clock is provided and therefore could vary.

Device ID	VDDD_33 [mA]	VDDA_5 [mA]	VDDD_5 [mA]	Power [mW]
1A	< 1	135	< 1	675
1B	< 1	134	< 1	670
1C	< 1	135	< 1	675
Average	**< 1 (< 3mW)**	**134.6 (673mW)**	**< 1 (< 3mW)**	**673mW**

Table 9: Power consumption with no clock.

The following power measurements were performed at a nominal clock speed of 25MHz.

Table 10 shows the power consumption under idling conditions when no image acquisition is performed. Table 11 shows the peak power consumption measured while capturing images at the nominal operation speed of 25MHz (10 Frames/s). These peaks can be seen as current spikes. Table 12 shows the average power consumption while capturing images at the nominal clock frequency (25MHz).

Device ID	VDDD_33 [mA]	VDDA_5 [mA]	VDDD_5 [mA]	Power [mW]
1A	49	60	3	478
1B	50	61	2	480
1C	49	62	3	487
Average	**49.3 (163mW)**	**61 (305mW)**	**2.6 (13.3mW)**	**482**

Table 10: Power supply measurement results when idle (CLK=25MHz).

Device ID	VDDD_33 [mA]	VDDA_5 [mA]	VDDD_5 [mA]	Power [mW]
1A	57	77	38	763
1B	55	79	32	737
1C	56	82	41	800
Average	**56 (185mW)**	**79.3 (396mW)**	**37 (185mW)**	**767**

Table 11: Peak current measurement results when capturing images (CLK=25MHz).

Device ID	VDDD_33 [mA]	VDDA_5 [mA]	VDDD_5 [mA]	Power [mW]
1A	52	49	45	642
1B	50	41	44	590
1C	49	45	46	617
Average	**50.3 (166mW)**	**45 (225mW)**	**45 (225mW)**	**616**

Table 12: The mean power consumption while capturing images (CLK=25MHz).

Above measurements were repeated for a clock speed of 12.5MHz.

Device ID	VDDD_33 [mA]	VDDA_5 [mA]	VDDD_5 [mA]	Power [mW]
1A	24	60	4	399
1B	25	62	3	407
1C	23	58	3	381
Average	**24 (79 mW)**	**60 (300mW)**	**3.3 (16.7mW)**	**396**

Table 13: Power supply measurement results when idle (CLK=12.5MHz).

Device ID	VDDD_33 [mA]	VDDA_5 [mA]	VDDD_5 [mA]	Power [mW]
1A	26	75	26	591
1B	28	74	28	602
1C	28	76	33	637
Average	**27.3 (90mW)**	**75 (375mW)**	**29 (145mW)**	**610**

Table 14: Peak current measurement results when capturing images (CLK=12.5MHz).

Device ID	VDDD_33 [mA]	VDDA_5 [mA]	VDDD_5 [mA]	Power [mW]
1A	26	43	12	361
1B	28	37	17	362
1C	28	45	16	397
Average	**27.3 (90mW)**	**41.6 (208mW)**	**15 (75mW)**	**374**

Table 15: The mean power consumption while capturing images (CLK=12.5MHz).

3.9 ADC Missing Codes

3.9.1 Procedure

At the input of the ADC, a triangular waveform is applied with amplitude and DC offset such that the input signal slightly overlaps the useful ADC range. The ADC clock frequency is nominal (12.5MHz) and the signal frequency is about 50 times lower than the clock frequency (250kHz) and asynchronous to it. All bias levels are kept as for normal operation.

The resulting data was saved as a full frame image (768x1024 pixels) and a histogram was calculated over the whole image. Any missing codes are detected by analysis of the histogram.

3.9.2 Measurement Results

No missing codes were found on the test devices, see Figure 4.

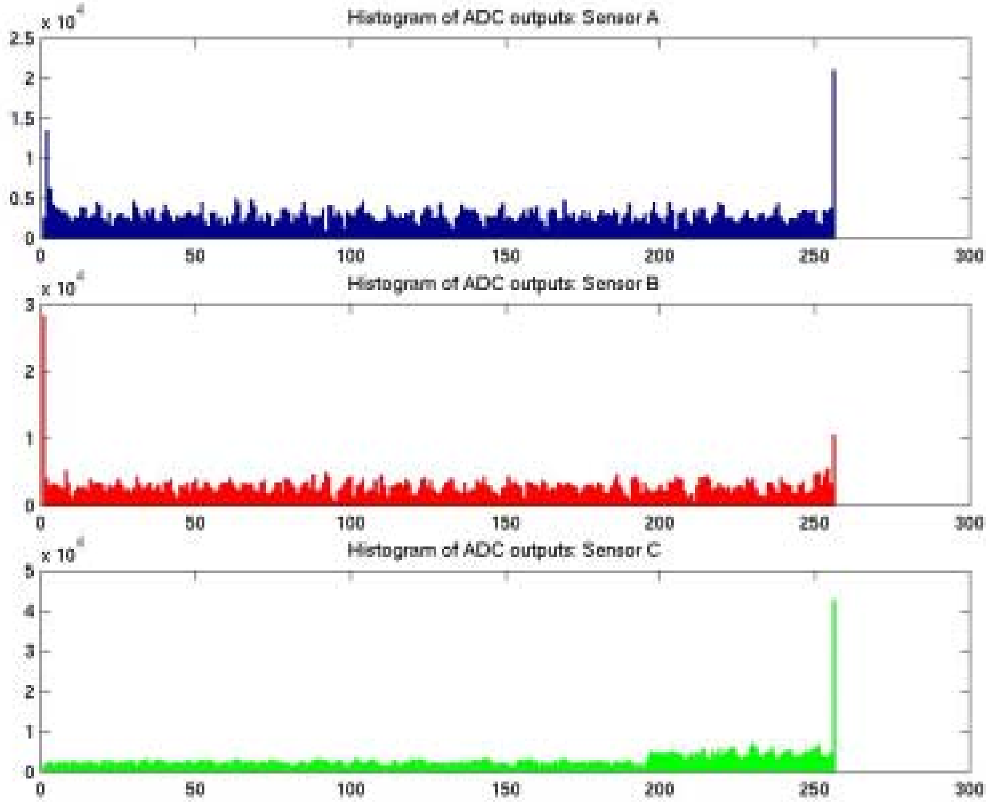

Figure 4: Histograms of ADC output levels for three sensors to detect missing ADC codes.

3.10 ADC Linearity

The ADC linearity measurement indicates the usable ADC range and its accuracy.

3.10.1 Procedure

For the ADC linearity measurement, the ADC is separately fed with a DC voltage using the AIN input. The biasing and input range setting is nominal: as indicated in Table 1.

A DC voltage is applied to the input terminal and the input voltage is measured using a DC voltmeter. At each step of DC input sweep 2048 samples are saved as an image. The average of these samples is taken as the output code for the applied voltage.

The linearity, expressed as a number of LSBs, is defined as the maximum difference between the measured data and a straight line fit through these data.

3.10.2 Measurement results

Device ID	Linearity [ADU]
1A	3.307
1B	1.148
1C	3.792

Table 16: ADC linearity

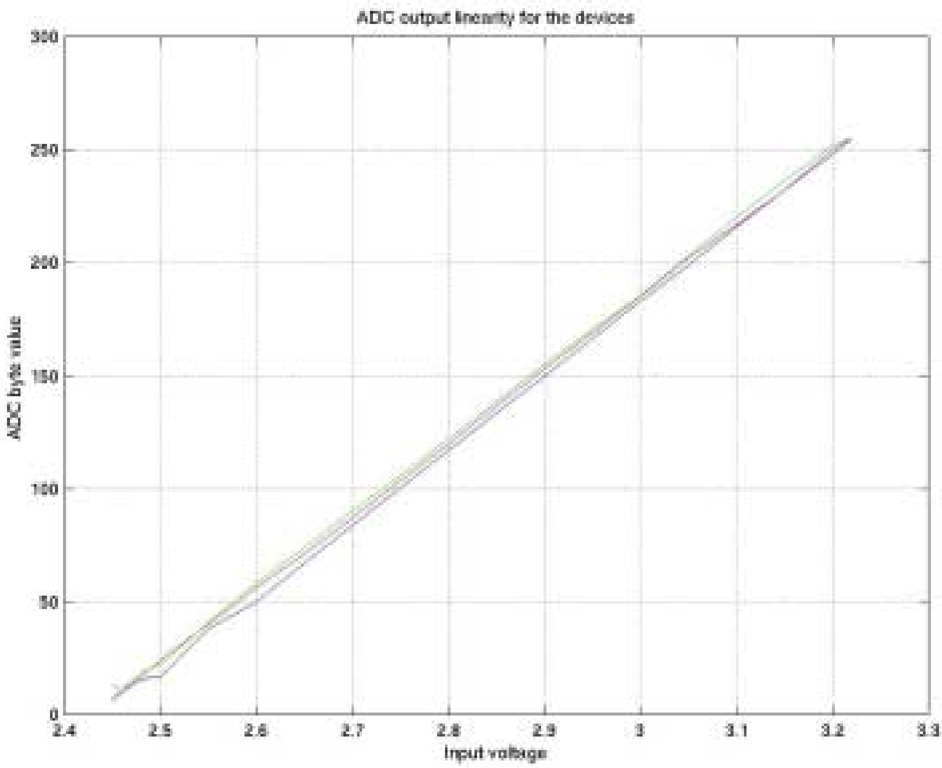

Table 17: The measured ADC output plotted against the input voltage.

3.11 ADC Delay Time

The ADC delay time is a measure of the speed of the digital part of the ADC. Due to the fact that no direct optimised path exists from the ADC outputs to an IO pad these measurements will not be a true representative of the actual delay.

3.11.1 Procedure

For the ADC delay time measurement, the ADC is separately fed with the biasing and input range settings nominal; as for normal operation with the image core.

A square wave signal is fed to the ADC using the AIN input, the ADC clock is monitored by outputting on the SDRAM control signals. Due to the architecture of the digital core only the two MSB bits were monitored by outputting it on the RC bus. Due to the long, non-optimised routing and the RC delay on the PCB tracks, this could lead to larger delays than expected.

A square wave of 2MHz was used as input and the ADC was running at its nominal operational speed, 12.5MHz. To allow accurate conversions in the analogue part, readings were only taken where the setup time of the input signal exceeded 50ns relative to the falling edge of the ADC clock. Delay times for both low-to-high and high-to-low transitions were monitored.

3.11.2 Measurement Results

Table 18 shows the measured delay times for three devices. These delays includes the internal delays in the chip as well as the delays due to the PCB tracks and should only be seen as a relative indication of the ADC performance. In reality these delays should be less.

Device ID		**Maxim delay [ns]**	**Average Delay [ns]**
1A	High-to-Low	46.6	45.4
	Low-to-High	92.0	71.6
1B	High-to-Low	48.0	46.5
	Low-to-High	77.4	71.5
1C	High-to-Low	46.5	44.6
	Low-to-High	86.2	70.5

Table 18: Delay time measurement results.

3.12 Higher Operating Speeds

This test is done to determine the performance of the devices at speeds higher than the nominal rated speed. A device is clocked at a higher speed than the rated 25MHz. Images were captured at clock speeds of 28MHz and 30MHz and examined.

28MHz	No visible image degradation
30MHz	Black pixel starting to appear

3.13 Characterisation over temperature range

The dark current, Fixed Pattern Noise (FPN) and Dark Current Non-Uniformity (DCNU) tests were repeated at a higher temperature.

3.13.1 Procedure

Thermostream equipment was used to blow heated air of 55^{o}C over the packaged imager chip while measuring the DUT. To make sure the DUT was temperature stabilised 30 minutes was allowed for the heating of the device. Three devices were tested.

The dark current, Fixed Pattern Noise and Dark Current Non-Uniformity was measured at these conditions using the same method as for the room temperature characterisation.

3.13.2 Measurement Results

Device	Local FPN [% of FS]	Global FPN [% of FS]	Local DCNU [% of FS]	Global DCNU [% of FS]
1A	0.115	0.600	2.514	4.651
1B	0.073	0.542	2.218	4.049
1C	0.090	0.598	2.393	4.679
Average	**0.092**	**0.580**	**2.375**	**4.459**

Table 19: FPN and DCNU results measured in an air stream of 55^{o}C.

Device ID: Pixel	Dark Current: mV/s	Dark Current: e-/s	Dark Current: pA/cm^2
1A (256, 256)	231	2 2148	1575
1A (768, 256)	285	2 7325	1943
1A (256, 512)	227	2 1764	1548
1A (768, 512)	192	1 8408	1309
1B (256, 256)	263	2 5216	1793
1B (768, 256)	277	2 6558	1889
1B (256, 512)	218	2 0901	1486
1B (768, 512)	236	2 2627	1609
1C (256,256)	190	1 8217	1295
1C (768, 256)	193	1 8504	1316
1C (256, 512)	222	2 1285	1514
1C (768, 512)	179	1 7162	1220
Average	**226**	**2 1676**	**1 541**
Maximum	**285**	**2 7325**	**1 943**
Minimum	**179**	**1 7162**	**1 220**

Table 20: Dark Current results measured in an air stream of 55°C.

4 Conclusion

The electro-optical evaluation of the IRIS-3 image sensor allowed to confirm or to update the specifications that were set forward during the design phase. The data sheet of the image sensor device is updated accordingly.

Table 21 shows an overview of the measurement results and indicates whether specifications were met or not. The last column of the table indicates conformity with the design specifications.

This overview shows that most of the design specifications were met. Exceptions to this are the analogue output voltage swing. Resulting from the low output voltage swing also the saturation charge specification is not met. The lack of saturation charge is however compensated by the low noise figure, resulting in a dynamic range that is still within specification. Keeping in mind that a 10-bit ADC is used; this result is therefore adequate.

From the measured electro-optical results it is clear that an excellent performance could be reached despite the large amount of digital electronics integrated on the same chip.

Parameter	Design Specification	Measured specification	Conformity
Spectral range	400 – 1000 nm	400-1100nm	OK
Quantum Efficiency x Fill Factor	>= 26%	>= 20%	±
Full Well capacity	247K electrons	121550 e-	Under Spec
Saturation capacity to meet non-linearity within ± 1%	82K electrons	84 533 e-	OK
Output signal swing	2 V	1.278 V	±
Conversion gain	8.89 µV/e- -	10.43 µV/e-	OK
kTC noise	54 e-	52 e-	OK
Dynamic Range	73 dB (4500:1)	67.8 dB (2454:1)	OK
Fixed Pattern Noise	3% of full well	Local:0.092% Global: 0.57%	OK
Photo Response Non-uniformity at Qsat/2 (RMS)		Local:0.62% Global: 1.67%	OK
Average Dark Current at 293 K	< 600 pA/cm^2	155 pA/cm^2	OK
Dark current signal	10800 e- / s	2186 e-/s	OK
Optical cross-talk at 600 nm	16 %	Horizontal: 17.5% Vertical: 16%	OK
Anti-blooming capacity	x 1000	Not measured	
Pixel output rate	12 MHz	ADC delay time < 90 ns	±
Output amplifier gain	1, 2, 4 or 8	Gains: 2.47,4.59 and 8.64	OK
Analogue input bandwidth	10 MHz	9.98MHz	OK
Analogue input signal range	+2V to + 4V	+2.431V to 3.250V	Under spec
ADC Differential Non-Linearity (DNL)	<= ±3.5.bit	Not measured	
ADC Integral Non-Linearity (INL)	<= 1% of full range	<=3.8 LSB	OK
Power Dissipation	Not listed	616 mW	OK

Table 21: Overview of measured electro-optical results.