Functional and Performance Validation of the 80S32 µC

Datasheet Update

Deliverable D5.2 – Dissemination Material

Workpackage 5 – Evaluation Kit

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1 Introduction

This document is an errata section based on the 80S32 fault description with respect to the published ADV 80S32 V 2.5 datasheet.

1.1 Reference Documents

RD-1 "MCS51 MICROCONTROLLER FAMILY USER'S MANUAL", INTEL – (can be downloaded from http://developer.intel.com/design/mcs51/manuals/272383.htm)

RD-2 ADV80S32 Datasheet V2.5, ADV Engineering, 22.05.2001

RD-3 "80S32 Validation Plan", D2.3/ISD/80S32 V1.2, ISD SA, 15-02-2009

2 Errata

2.1 Block diagram

At the block diagram (see RD-2, page 1) the USART 4 should have signals sx4clk, sx4val and sx4dt instead of sx1clk, sx1val, and sx1dt as shown in the block diagram.

2.2 Parallel Port P0

Parallel port P0 cannot be configured for general purpose I/O. According to the datasheet (see RD-2, §3.4.5, §8) setting register EXTBUS to 0x00 should reserve the port for I/O. Setting register P0DIR to 0xFF should configure the port as output, however no data are transmitted when the port is written. This has been observed through a logic analyzer by taping directly on the P0 pins. The port is also incapable to receive data (P0DIR set to 0x00) since it always holds value 0x00 although a different value is sent to the pins (also confirmed through the logic analyzer).

The port operates correctly in alternative function mode (address expansion) as it has demonstrated in test 2.1.

Ports P1, P2 & P3 have been found to operate correctly in both modes (see Timers & USART tests).

2.3 External Interrupts 2, 3 & 4

According to documentation (see RD-2, §6, page64) interrupts IE2, IE3 & IE4 can be triggered/cleared by software by setting appropriate bits in register TXCON1. However it has been found that once triggered the interrupt cannot be cleared (ISR is called over and over again) and instead it has to be disabled through register IXEP3. This applies to all three external interrupts.

2.4 USART Interrupts

It has been observed through the use of a logic analyzer that the USART interrupt is raised (due to TI bit being set) as soon as the SXxBUFL register is written. Thus, when multiple bytes are to be sent, depending on the delay between consecutive writes some bytes will be overwritten and will not be transmitted. For example when 5 bytes were written (one at a time after interrupt had been raised), only the first and the last were actually transmitted. When a small delay was introduced between each write, then the third byte was also transmitted.

A similar problem exists when the USART is receiving, i.e. the interrupt is raised before the whole byte is received and the contents of SXxBUFL are 0x00.

2.5 Register Default Values

2.5.1 EXTBUS, P1CON, P2CON & P3CON

According to documentation (see RD-2, §8) after power-up or reset, all parallel ports should be configured in alternative function mode, instead they are configured as bi-directional ports.

2.5.2 P0DIR, P1DIR, P2DIR & P3DIR

According to documentation (see RD-2, §8)) after power-up or reset, the direction of the parallel ports when in bi-directional mode should be output, instead they are configured for input.

2.5.3 TXCON2

According to documentation (see RD-2, §6 figure 6-5) if the register is written with value 0xAA, then we should get the same value when we read it. Instead we get value 0x00.

2.5.4 TXCON3

According to documentation (see RD-2, §6 figure 6-5) if the register is written with value 0xAA, then we should get the value 0x80 when we read it. Instead we get value 0x00.

3 Pin Description

3.1.1 CODE0_BUSCTL0, CODE1_BUSCTL1, SCANEN_BUSCTL2, FALLCLK_BUSCTL3

According to the documentation (see RD-2, Pin Assignment on page 76) the following physical pins are defined as outputs which should be left floating:

- CODE0_BUSCTL0 (pin 97)
- CODE1_BUSCTL1 (pin 98)
- SCANEN_BUSCTL2 (pin 99)
- FALLCLK_BUSCTL3 (pin 100)

For proper operation these pins should be connected directly to VSS, as discovered during the initial debugging phase of the design.

The first tests were performed by pulling all the above pins down via 10KΩ resistors, but glitches with duration shorter than 1 clock cycle have been observed on 'RD_n' & ' WR_n' lines. Inspection of the VHDL code and netlist revealed that the relevant pins are designed to be registered-out using a single scan-out multiplexer after the Flip-Flops. A voltage level of 0.5VDC was observed using laboratory measurements across the 10KΩ termination pull-down resistors. This voltage may appear due to the leakage current value of 50uA as specified in the Atmel datalog. This voltage level is considered to be close to the VIL threshold of the input pad. Additional noise could cause spurious activation of the pin and unwanted glitches as a consequence. The problem was addressed by short-circuiting the

10KΩ resistors. For normal operation these pins should be tied directly to the VSS plane of the PCB.

3.1.2 RESET

According to the documentation (see RD-2, Interface Signals on page 71) the input pin 'RST' is erroneously specified as a reset suggesting active low triggering. The trigger mode of this pin is active high, as discovered during the initial debugging phase of the design.

4 Electrical Characteristics

Table on RD-2 §11.2 page 77 should be updated with the following one.

Symbol	Parameter	Min	Typ.	Max	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.2	-	Vcc	V
VIL	Input Low Voltage	-0.3	0	0.8	V
Tclock	Clock period Duty Cycle	45.5	45.5	45.5 45	ns %
Pd	Power consumption	266	339,2	427	mW

The power consumption field has been measured up under the following operating conditions.

1. Tclock = 45,5 ns
2. 80S32 on running state
3. Operating Voltages min=4.5 - typ.=5.0 and max=5.5V accordingly.