ASTRIUM's Mixed-Signal Asics Development Methodology

M. Dollon, A. Wagner, M. Vandenbossche, M. Moroni

matthieu.dollon@astrium.eads.net, arnaud.wagner@astrium.eads.net, mathieu.vandenbossche@astrium.eads.net, , didier.moroni@astrium.eads.net

EADS Astrium, 1 Boulevard Jean Moulin, ZAC de la Clef-St-Pierre, 78990 Elancourt, France

1. INTRODUCTION

To cover **ASTRIUM's needs** for the next 15 years more than 15000 mixed signals Asics (Application-Specific Integrated Circuit) have to be produced. To perform this successfully a sustainable **development and production process** must be elaborated now.

A selection of a technology which both fulfils the designer's requirements for the expected performance of the Asics and allows all the intended future Asics to be manufactured has to be carried out. The section "Technology" develops these points.

It is crucial for the user **to master the overall development process** of the ASIC in order to achieve a successful development, but also for the product follow-up over the next 20 or 30 years.

Two teams, the user and the design house, work together on all stages of the development: architecture, detailed design, validation by simulation and ASIC characterization. This is the subject of the section "Co-design".

Having **representative and precise simulation models of basic parts of the library (i.e. transistors, resistors, capacitors)** which embed, as far as possible, all potential environments is essential. The design of these models is detailed in the section "Design of an ASIC".

The use of **building-blocks**, which are analogue functions that have been characterized electrically and whose behaviour with respect to radiation and heavy ions has been tested, allows development times and risks to be reduced. This is also further explained in the section "Design of an ASIC".

2. ASTRIUM NEEDS

To reduce volume, mass and cost of ASTRIUM's units and to increase its functionalities some Asics have been identified the functions which may be implemented in an asic are:

- Generation of high power pulses ,
- Analogue voltage acquisition and conversion,
- 1553 analogue transceivers,
- DC/DC converter and motor control,
- Power converters for RF emitter,
- Video chains,
- Control loop and cell power command and monitoring,
- Point Of Load ,
- RF front-end,

Large quantity has been forecasted: up to 1000 or 2000 per type for 10 years production.

These Asics are of medium complexity, except for RF front-end, and need a 15 V analogue supplies voltage, except for high power pulses generator which maximum analogue voltage is 40V.

These Asics are mainly composed of same functions, called building blocks.

3. DEVELOPMENT AND PRODUCTION PROCESS

The design and manufacturing flow of an analogue or mixed ASIC for space application is depicted in figure 1.

Six main tasks are identified in the design flow:

- The Customer/Astrium generates the need specification of the product and can perform a part of the design and layout tasks according to the available tools and skills. Astrium performs also most often the radiation tests.
- The Design House is in charge of the design and layout of the ASIC.
- The Foundry receives the GDSII tape from the Design House and performs the wafer manufacturing. For analogue and mixed ASIC, the delivery of the foundry is most often un-sawed and untested wafers associated to log files recording the process parameters of the lot. The foundry guarantees only that these parameters are nominal.
- The Assembly House performs the wafer sawing, the visual inspection, the packaging and the packaging control (die attach, wire bonding, bond strength, die shear, sealing, marking…).
- The Test House is in charge of the test of the packaged parts and of the probe test at wafer level if this option has been selected.
- Qualification: This qualification is carried out at component level by a qualified package manufacturer. Astrium has the ability to perform this task.

The 6 tasks can be performed by different companies. In addition, a given company can take the responsibility of several tasks performed by sub-contractor.

To improve control of design and production the whole process can be managed by Astrium.

4. CHOICE OF TECHNOLOGY

The choice of the technology and its associated library is based on multiple parameters: functions that the designer wants to incorporate, maximum voltages of analogue transistors, frequency, power, logic gates supply voltage, number of logic gates, availability of characterized building-blocks, expected performance, durability of the technology/foundry, overall cost, prototyping service proposed, export regulations constraints…

One of the characteristics of the space environment is the radiation and particle flow which degrades electronic components over time. Consequently, the choice of a technology and its library must take into account the radiation constraints. Up to now, space mixed-signal Asics have been made with different technologies. To do so, either the Asics have been hardened by using specific rules for the layout, or a few elements of the library of the technology used have been hardened. These hardened elements are often covered by intellectual property and therefore not directly accessible. Similarly, only a few building-blocks have been made and they are generally not distributed. In addition, finding a suitable technology with high analogue voltages is difficult.

At least, the selected technology should enable Astrium to build the maximum number of potential Asics which have been identified. The aim is to become more and more experienced and to have more and more building-blocks in the chosen technology in order to reduce cycle times and risks for future developments.

Today, several technologies already have either favourable intrinsic characteristics or encouraging first results for a complete hardening. These technologies could probably be hardened successfully.

Different technologies have been examined and it seems that today, **a 0.35 µm technology from Xfab foundry** is a g trodade-off between integration and analogue voltage.

5. CO-DESIGN

An ASIC is a complex part, whose specifications may be difficult to write, having a lot of interactions with board environment and with long lifetime between the design and the end of utilisation.

An ASIC is complex: Many of the functions performed by a board/unit could in fact be integrated in an ASIC. Most potential Asics identified by Astrium are a collection of various analogue functions of different complexity. The interactions of these functions inside the ASIC are numerous, and so are the couplings with their environment. Asics will be at the heart (and the heart) of electronic units, therefore it is important to entirely master the design and validation.

To follow production during more than 20 years, it is important to control design.

For these reasons, it is critical for the user to master completely a product over the course of its development today, and its production tomorrow. One solution, already in application, consists in co-developing a product with a design house.

The user specifies the needs for the ASIC. This specification includes thermal and mechanical aspects, EMC, reliability, failure cases and supply / signals interfaces. Concurrent engineering done with the design house enables development risks and performance optimization.

Cooperation in architecture and detailed design leads to a more exhaustive development: the design house is typically in charge of developing building-blocks (with the user giving specifications) and the architecture and organization is usually a task for the user.

During the whole development, the two different expertises are important for analysis completeness.

Fig. 2~~Fig. 2~~ shows the development and production flow of Asics.

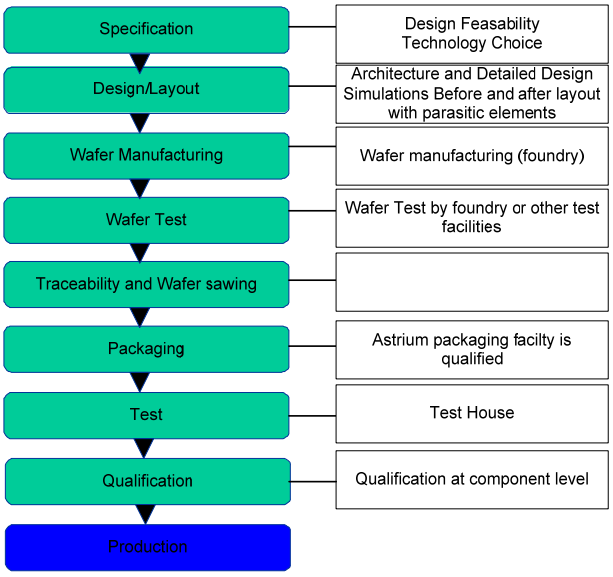

Fig. 1 – Development and production flow

6. DESIGN OF AN ASIC

The design of a mixed-signal ASIC is mainly based on simulations since it is very difficult – almost impossible – to make direct measurements on internal signals. Even though Asics are characterized both electrically and in their environment, this only concerns their inputs/outputs: internal margins such as noise immunity and stability are guaranteed by simulation solely. The same applies for the end-of-life worst-case behaviour (including the effect of both ageing and the Total Ionization Dose (TID)) which is a prediction based on simulations.

These simulations, which have to guarantee the functionality and performances of the chip, use a schematic which possibly includes parasitic elements. All internal margins are provided by those simulations whose accuracy depends on device models and parasitic elements.

How can the development of an ASIC be organized in order to optimize the coverage and accuracy of the design?

Having **representative and precise simulation models of basic parts of the library (i.e. transistors, resistors, capacitors)** which embed, as far as possible, all potential environments is essential.

The use of **building-blocks**, which are analogue functions that have been characterized electrically and whose behaviour with respect to radiation and heavy ions has been tested, allows development times and risks to be reduced.

The methodology is based on simulations, worst-case performance analysis or statistical predictions. These simulations must cover a range as wide as possible. This is further explained in the paragraph “Simulations”.

In order to have experimental results about worst-case performance, it may be possible to test irradiated and burned representative samples at different temperatures. In addition, to identify internal margins, characterization outside specifications may be performed on these samples. Of course these validations happen lately in the development.

6.1 SCHEMATIC DESIGN

Complex analogue functions are difficult to study by simulation due to simulations duration and weakness of some models.

To reduce the development risks, a solution is to use building-blocks which are the ASIC equivalent of ICs. A building-block is a schematic and a layout which have been completely characterized. A data sheet gives the performances and all the usage conditions

A building-block is a function designed to meet a range of applications. It is considered as a product. The development of a building-block is identical to the one of an ASIC. Samples are designed, simulated and then manufactured, and different tests are carried out: thorough electrical tests, TID and heavy ion tests, ageing tests… In particular, the search for operating limits – and therefore margins with respect to actual operating conditions – allows the internal margins to be checked.

Without the use of building-blocks, the development of an ASIC could lead to a long and tricky process. So it would be preferable to design, manufacture and characterise these building blocks before asic development.

As they become available, these building-blocks allow development cycles to be drastically reduced, with the restriction to use the same technology.

6.1.1 Architecture

This design stage includes the same activities as those carried out for discrete electronics, but applied to Asics here. The ICs are replaced by building-blocks and general rules are set to avoid coupling between building-blocks which would degrade their performances (sensitive signals / destabilizing signals, coupling by supply and ground impedance…).

6.1.2 Schematic simulations

Simulations are done with the following elements:

- The transistor models of the ASIC are physical and therefore very close to reality.
- TID and ageing effects are either included in the models (which is not the case today), or added by hand by the designer in some simulations.
- Parasitic elements calculated from the routing of the chip and the package, track resistances, parasitic capacitances and inductances which create couplings, filtering, delays, supply common mode…

It is critical to estimate during the design stage ALL parasitic elements which may, above their critical values, disturb the nominal operation, including start-up. These critical values come from simulations and they may be iterated at the design stage.

The same remarks apply to the routing of the package which must meet the constraints derived at the design stage.

6.1.3 Post-Layout simulations

Once the layout is done, two types of simulations are possible:

- Schematic simulations with a choice of parasitic elements extracted from the "flattened" routing file. These simulations are fast and may be numerous. They allow multiple design points to be checked.
- "Flattened" simulations which include a large number of parasitic elements: they are very long and hence not so numerous…but they are exhaustive.

6.1.4 Chip/ASIC validation

Characterisation phase is critical.Although it is essentially input/output signals measurements that lead to improve performances guarantees and some margin determination.

ASIC characterisations: has to be done on a representative number of samples, in various conditions of temperature and power supply. The ASIC setup, including input signals and power supplies, has to be representative of the specified conditions of use. It should also be readily adjustable to test the worst-case conditions. The behaviour with cumulated doses and particles is studied. Ageing tests are also performed. In order to make measurements in end-of-life conditions, it is possible to test burned and irradiated samples at different temperatures. The behaviour outside the conditions of specifications and functioning limits may be checked on these samples. This long validation phase helps .to secure it.

Discrepancies between simulations and measured performance must be understood and simulations must be improved to allow other investigations to be performed but also to be more efficient for future designs.

- Fig. 2~~Fig. 2~~ shows a diagram of the process followed for the design of an ASIC.

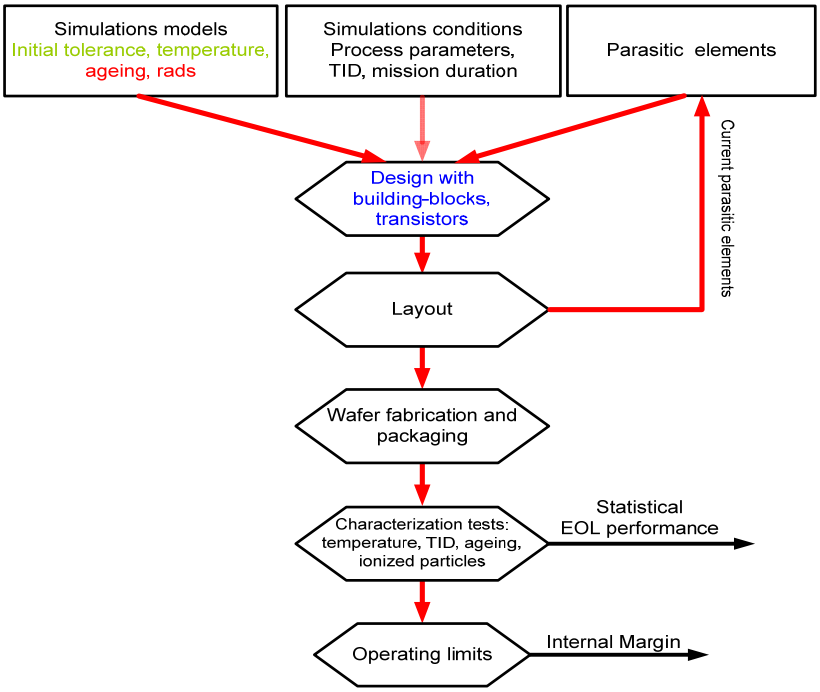

Fig. 2 – Building-blocks or ASIC development process for a given library

6.2 SIMULATION METHODS

Schematic is designed only by simulations. To improve design accuracy it is necessary to improve simulation models including, if possible, TID and ageing. Development of these models is described in Fig. showing how the transistor models are derived in a radiation-hardened library.

.

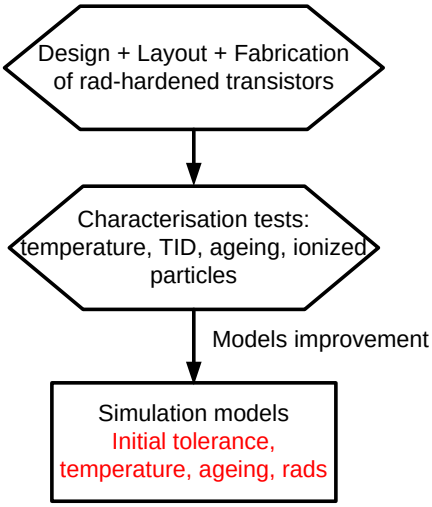

Fig. 3 – Transistors development in a radiation-hardened library

In addition, to analyse a performance, in beginning of life or worst case conditions, the designer sets up some simulation conditions and decides which simulations are the most relevant. Simulating everything is impossible.

The choice of what must be simulated to obtain a “bug-free” ASIC as using a minimum number of simulations is difficult.

A methodology must be developed, as for digital Asics, to permits a better control of design.

7. CONCLUSION

The main difficulties in developing an ASIC for Space come from the specific environmental conditions, TID and ionized particles and the low number of Asics expected to be made with respect to development costs.

A perennial production flow must be built. This flow allows the user to make his targeted Asics.

The choice of technology is strategic: hardened or “hardenable” library. This choice is not obvious given the numerous attempts which have been (or are) tested with several technologies and/or foundries.

First a completion of the foundry’s models by adding TID and ageing aspects has to be carried out.

The next step consists in developing building-blocks which will be used as basic bricks for the Asics. By separating problems, these building blocks also permit a secured ASIC development and enable the designer to move towards high-performance functions.

All these points are very costly and require an important investment.

The development process, mainly centred on simulations, has to be structured/organized to improve the robustness and completeness of the design.

Lastly, co-development contributes largely to this need for completeness. Crossing approaches, points of view and concerns makes it possible to obtain a “bug-free” ASIC as fast as possible and to reach the fully mastered performance the Space industry requires.