AMICSA 2012.

Challenges of Mixed Signal Space Grade ICs operating at Microwave frequencies.

A focus on Package design and Characterisation

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The challenges to succeed in Mixed Signal IC design at Microwave frequencies

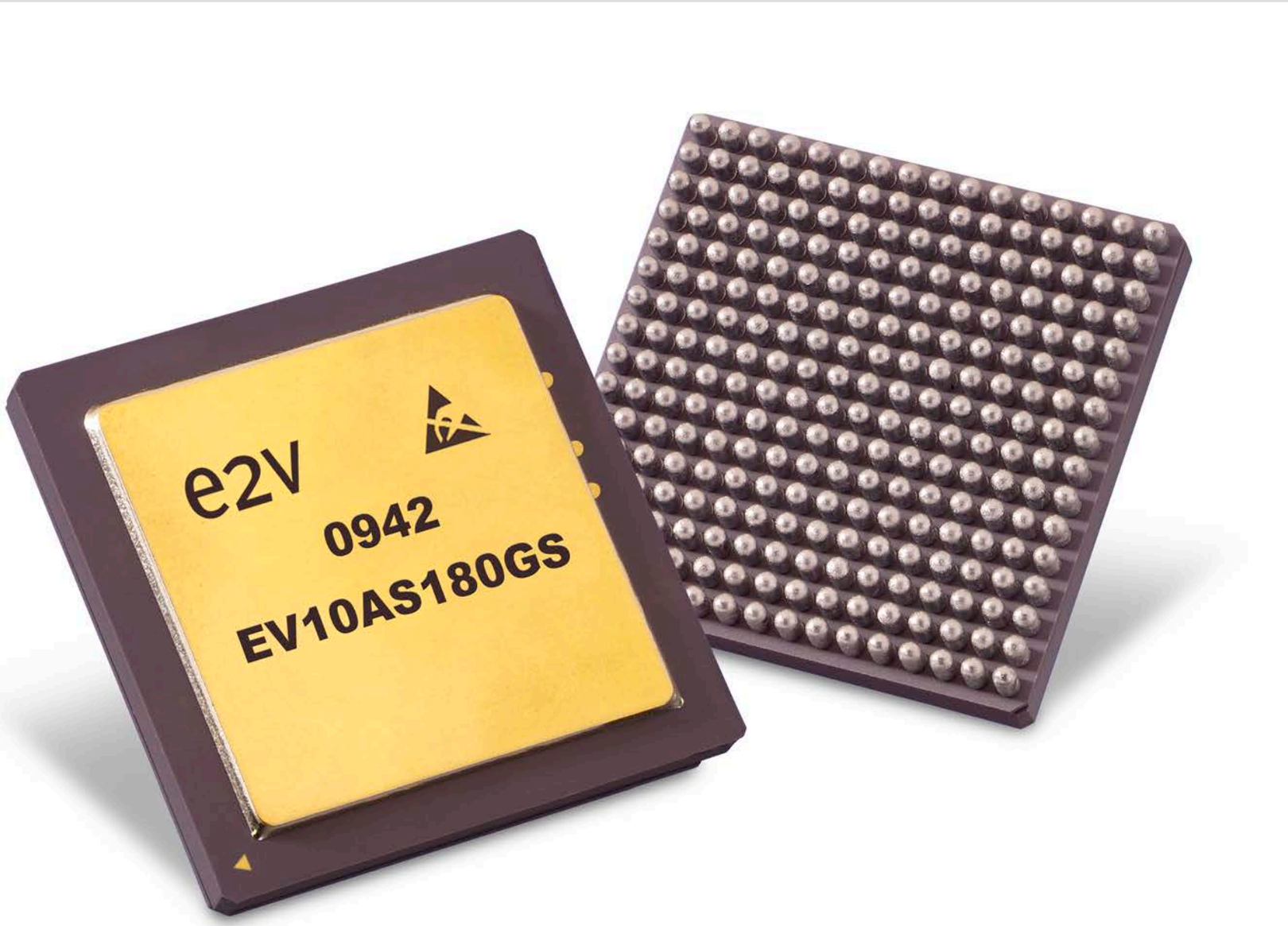
4 major areas require investments with specific focus for Microwave Mixed Signal ICs:

- ☑ Chip design.
- ☑ Package design.
- ☑ Characterisation.
- ☑ ATE Platform, Test tools development and test programme development specifically for Hi-Rel Temperature ranges.

Package design.
255-CCGA, Two e2v product use the same package.

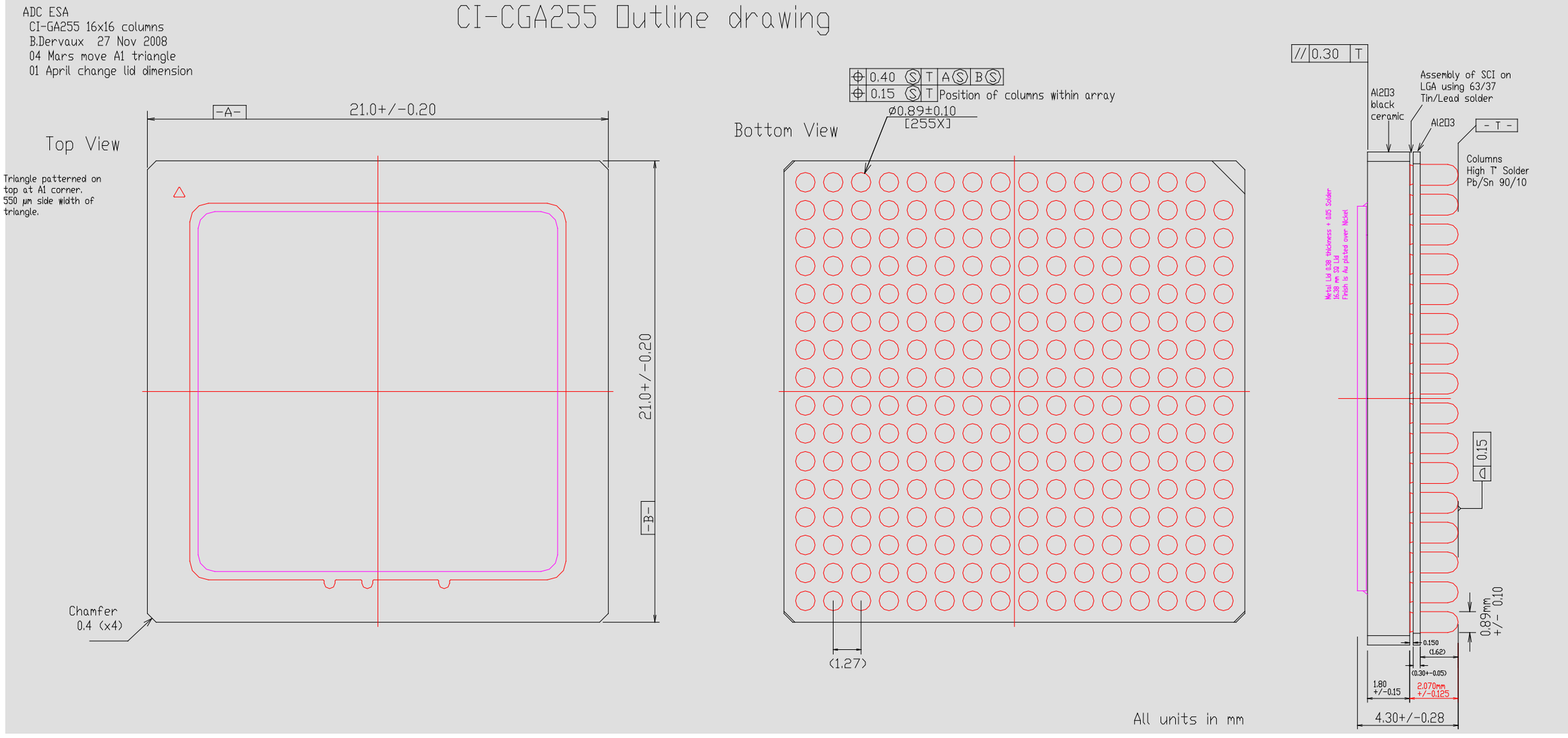
EV10AS180 : ESA ITT 10bit 1.5GSPS L-Band ADC.

EV12DS130 : CNES Sponsored 12bit 3GSPS L/S/C-Band DAC.

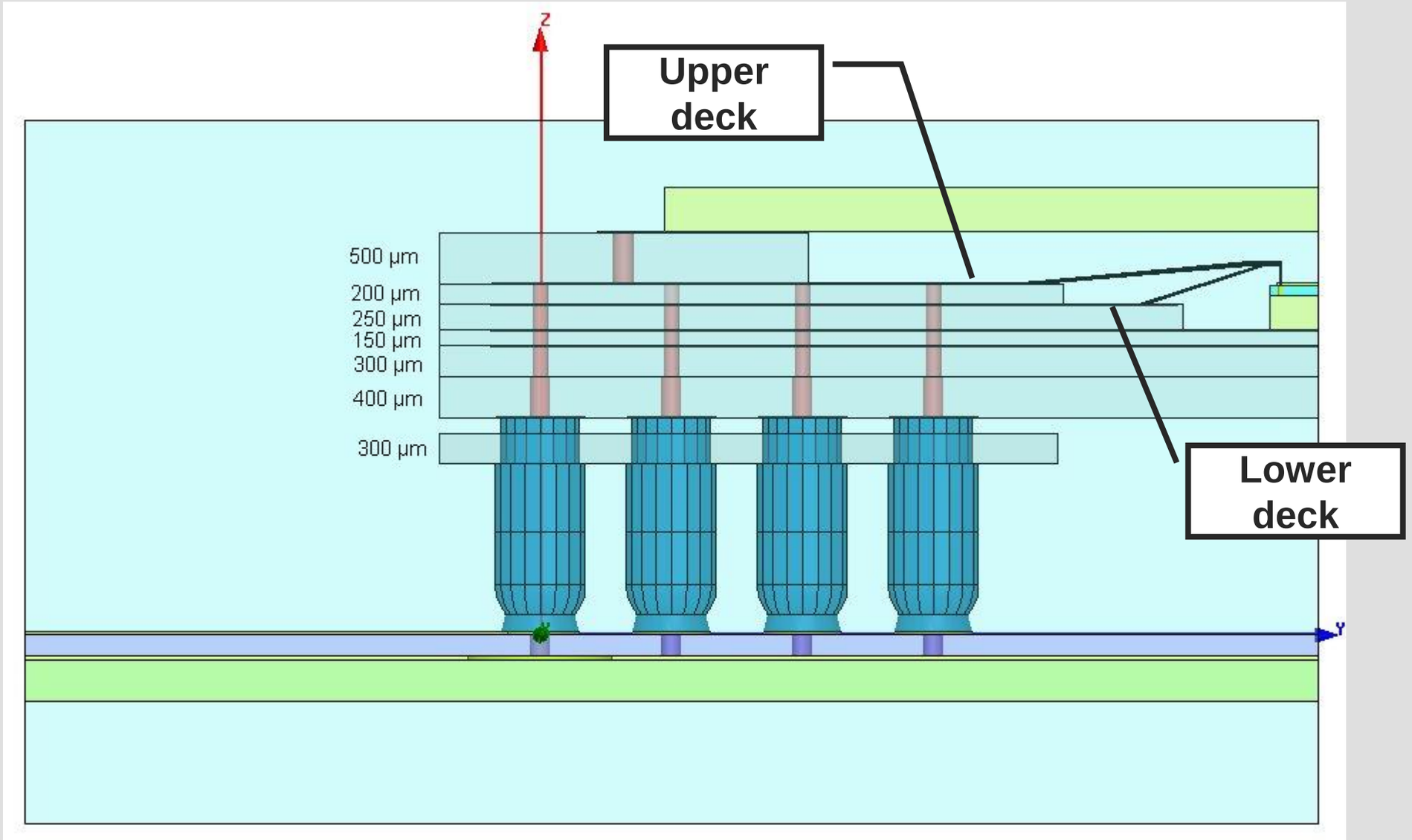


Package design.
Form factor and structure

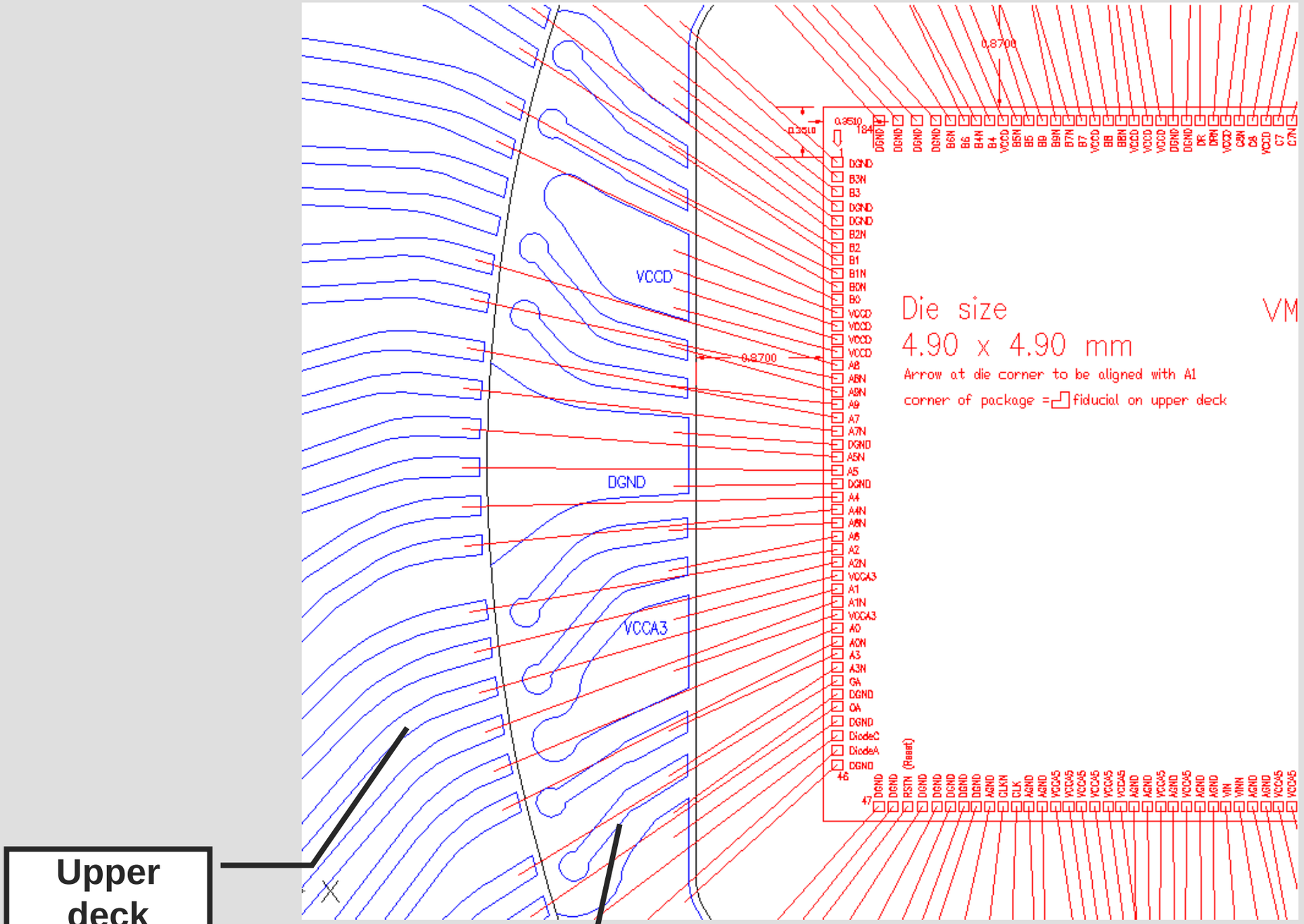
- **Case of EV10AS180 L-Band ADC and EV12DS130 L/S/C-Band DAC.**
- **255pin and a min pitch of 1.27mm led to a form factor of 21x21mm.**
- **A double deck package structure was necessary.**



Package design.
View on the double deck structure.



Package design.
View on the double deck structure.



Package design.
Pinout overview.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		VCCO	NC (DGND)	B4	B5	B7	B8	NC (DGND)	**DR**	C8	C7	C5	C4	NC (DGND)	VCCO	DGND	A
B	DGND	VCCO	NC (DGND)	B4N	B5N	B7N	B8N	NC (DGND)	**DRN**	C8N	C7N	C5N	C4N	NC (DGND)	VCCO	DGND	B
C	NC (DGND)	NC (DGND)	VCCO	DGND	B6N	B6	B9	B9N	C9N	C9	C6	C6N	DGND	VCCO	NC (DGND)	NC (DGND)	C
D	B3	B3N	DGND	VCCO	VCCO	DGND	DGND	DGND	DGND	DGND	DGND	VCCO	VCCO	DGND	C3N	C3	D
E	B2	B2N	B1	DGND	DGND	DGND	VCCO	VCCO	VCCO	VCCO	DGND	DGND	DGND	C1	C2N	C2	E
F	B0	B0N	B1N	DGND	VCCO	DGND	DGND	VCCO	VCCO	DGND	DGND	VCCO	DGND	C1N	C0N	C0	F
G	NC (DGND)	NC (DGND)	A9N	DGND	VCCO	VCCO	AGND	AGND	AGND	AGND	VCCO	VCCO	DGND	D9N	NC (DGND)	NC (DGND)	G
H	A8	A8N	A9	DGND	DGND	VCCO	AGND	AGND	AGND	AGND	VCCO	DGND	DGND	D9	D8N	D8	H
J	A7	A7N	A6N	DGND	DGND	VCC3	AGND	AGND	AGND	AGND	VCC3	DGND	DGND	D6N	D7N	D7	J
K	A5	A5N	A6	VCC3	VCC3	VCC3	AGND	AGND	AGND	AGND	VCC3	VCC3	VCC3	D6	D5N	D5	K
L	A4	A4N	A3	DGND	DGND	DGND	VCC5	VCC5	VCC5	VCC5	DGND	DGND	DGND	D3	D4N	D4	L
M	A2	A2N	A3N	DGND	DGND	NC (DGND)	AGND	VCC5	AGND	VCC5	NC or DGND	NC or DGND	DGND	D3N	D2N	D2	M
N	A1	A1N	DIODE C	OA	DGND	NC (DGND)	AGND	VCC5	AGND	VCC5	DGND	DGND	DGND	DECN	D1N	D1	N
P	A0	A0N	DIODE A	GA	DGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	DGND	SA	D0N	D0	P
R	DGND	DGND	DGND	NC (DGND)	NC (DGND)	**CLKN**	AGND	AGND	AGND	AGND	AGND	SDAEN	RS1	TM1	DGND	DGND	R
T	DGND	DGND	DGND	RSTN	NC (DGND)	**CLK**	AGND	AGND	**VIN**	**VINN**	AGND	SDA	RS0	TM0	DGND	DGND	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

TOP VIEW

supply1	VCCO	2,5V
supply3	VCC5	5-5,2V
VCC3	VCC3	3,3V

Package design.
Electrical lengths (ps)

This analysis becomes necessary for ICs operating in GHz range.

Optimisation through routing trade-offs needs to be done.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		VCCO	67	63	59	58	55	50	50	55	58	59	63	67	VCCO	DGND	A
B	DGND	VCCO	55	52	48	45	44	38	38	44	45	48	52	55	VCCO	DGND	B
C	70	56	VCCO	DGND	51	42	40	40	40	40	42	51	DGND	VCCO	56	70	C
D	60	49	DGND											DGND	49	60	D
E	57	46	52											52	46	57	E
F	54	43	43											43	43	54	F
G	54	42	42											42	42	54	G
H	54	42	41											41	42	54	H
J	54	43	41											41	43	54	J
K	60	48	42											42	48	60	K
L	60	49	43											43	49	60	L
M	63	52	52											52	52	63	M
N	68	57	51												57	68	N
P	73	61	53												61	73	P
R	DGND	DGND	DGND	48	44	43									DGND	DGND	R
T	DGND	DGND	DGND	59	55	55			54	55					DGND	DGND	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

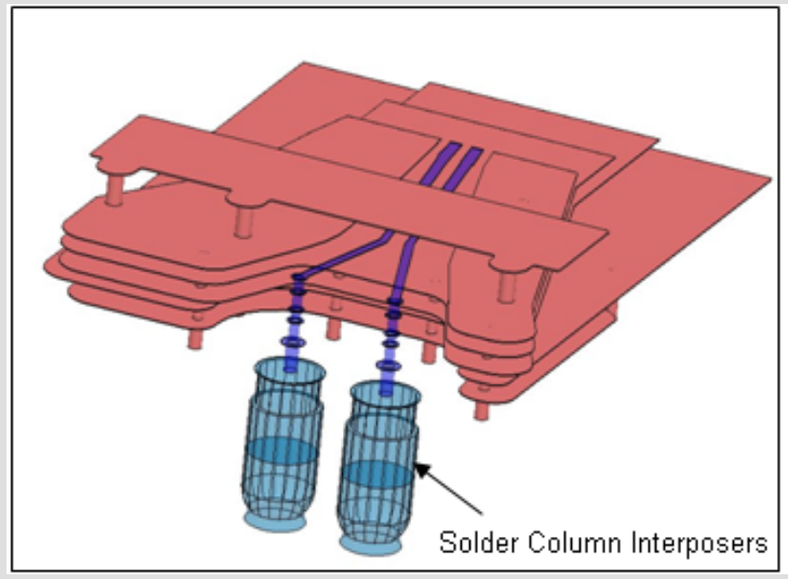
Package Design
3D Electromagnetic Simulation

3D EM simulation was done using HFSS v11.

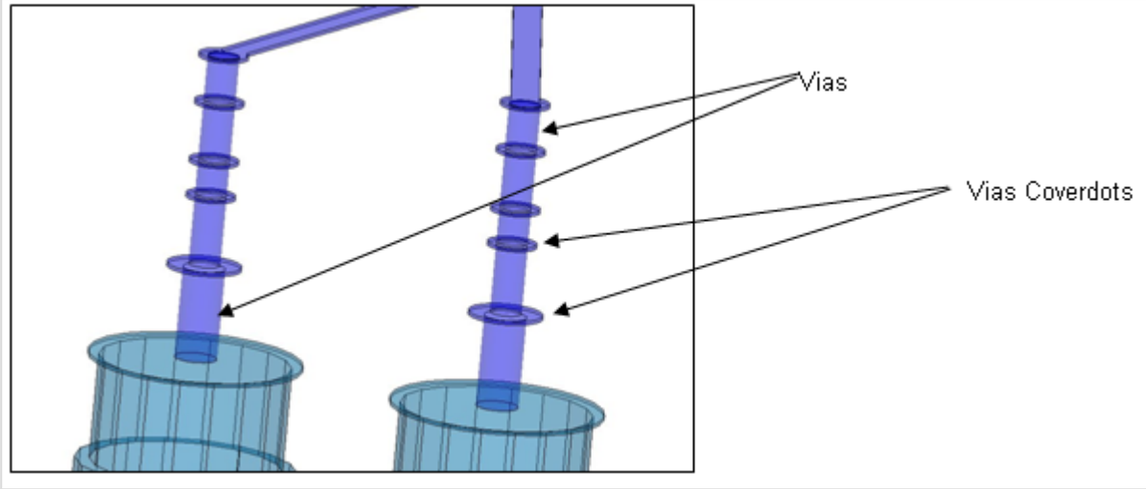
It allows exhaustive and accurate calculation of S-parameters of the full package structure.

This was necessary to achieve accurate optimisation of the package design at microwave frequencies.

The HFSS tool divides the detailed and accurate geometric model into a large number of tetrahedra where a single tetrahedron is a four-sided pyramid.



S11 and S21 parameters have been the subject of deep analysis and optimisation work to achieve the best possible signal transmission through the package and secure the guaranteed electrical performance of EV10AS180 ADC.

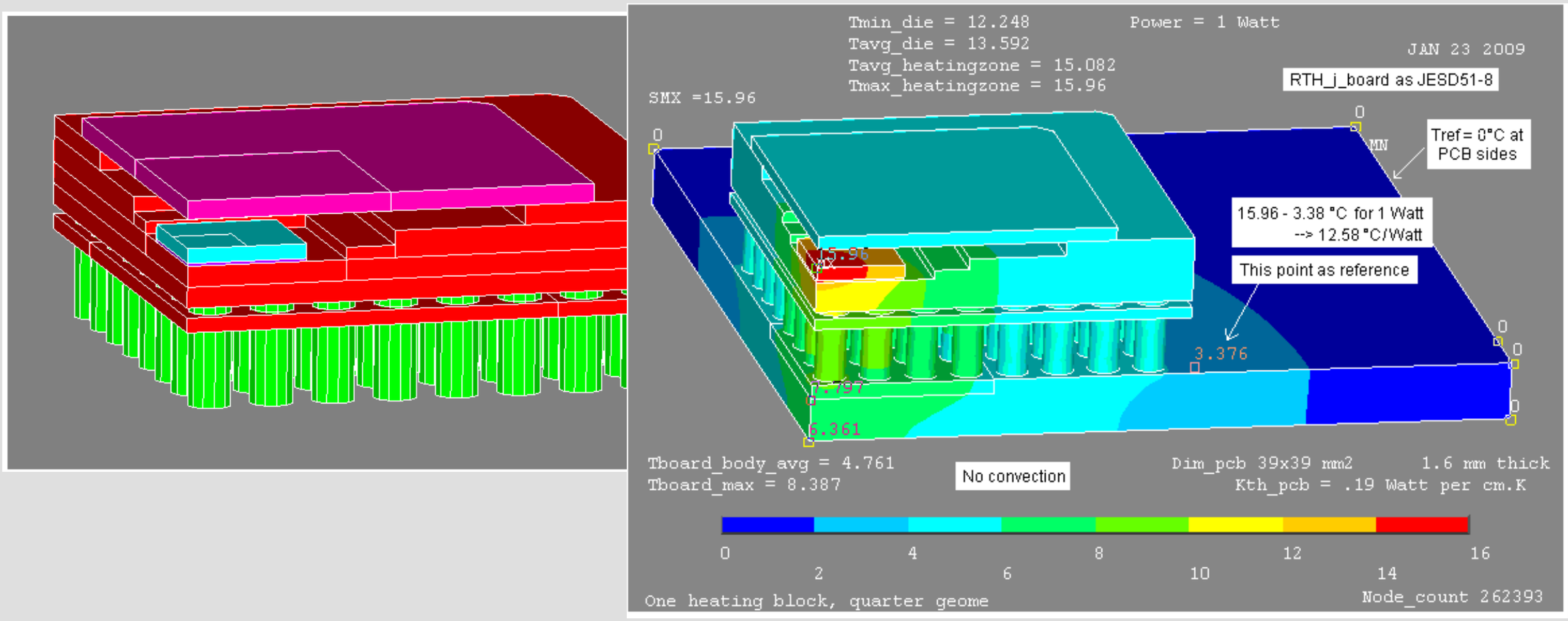


The objective was achieved with S11 of -15 dB and a transmission S12 of -0.3 dB at 2.0 GHz.

Package Design
Thermal modelisation

Step 1 – Initial work based on assumptions prior to completion of silicon design.

Simplified model based assuming that heating occurs on a square surface equal to 25% of overall die surface. Positioned at the center of the die.



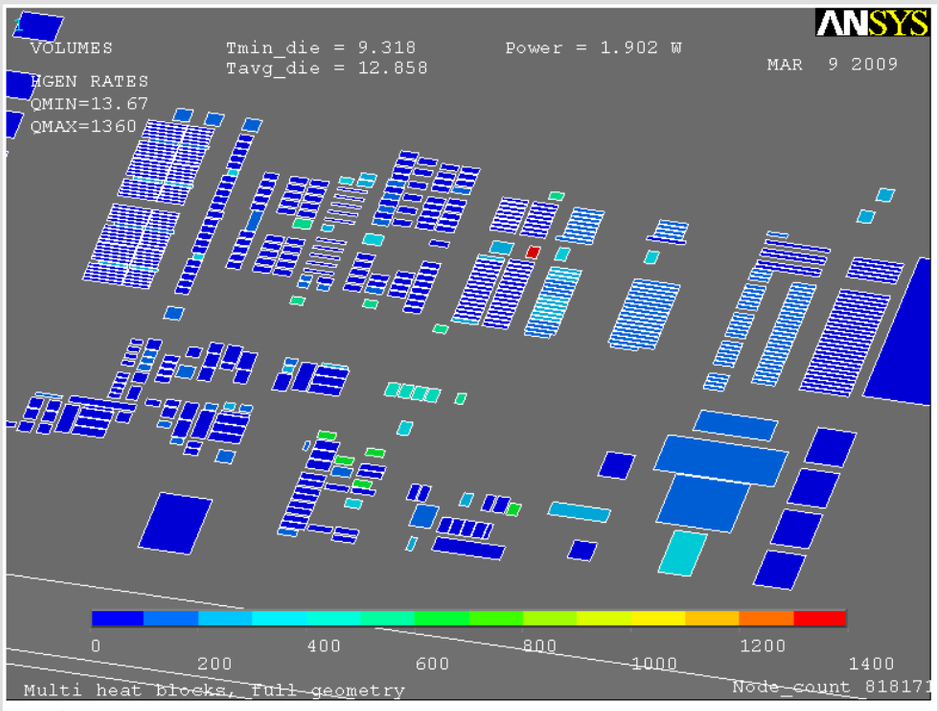
Thermal simulation of the package was done using ANSYS v11 simulation tool.

This software allows for accurate finite elements calculations of thermal performance of the full package structure.

Package Design
Thermal modelisation

Step 2 – Accurate mapping of heating blocks on the die.

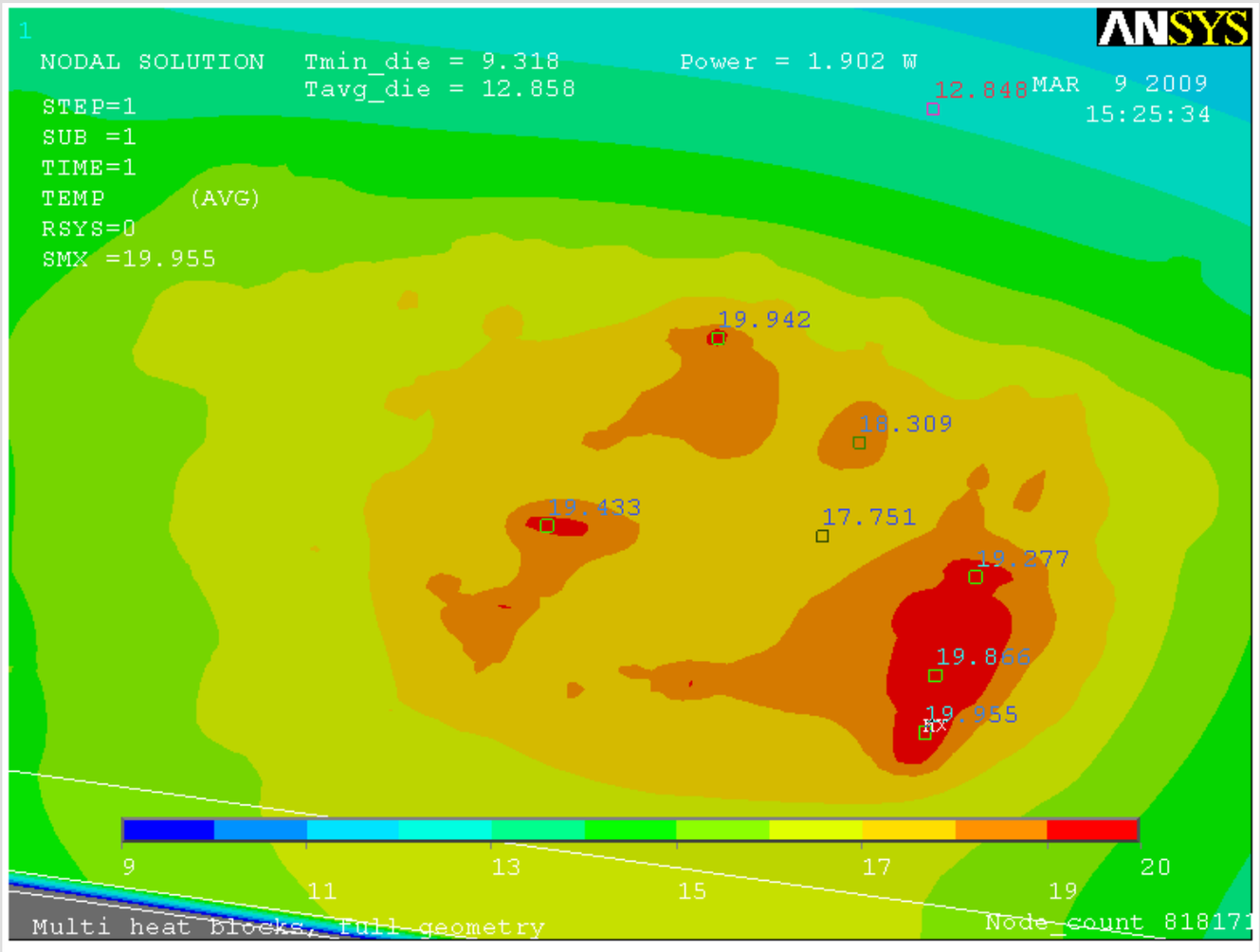
This allows for comprehensive and accurate thermal simution of the full package assembly.



Densité de puissance des blocs / Power density in each bloc

2 max hotspots found with only 20°C difference with Temperature at solder joints.

Rth Junction to PCB = 12.58°C/W JEDEC JESD51-8.



CI-CGA255 Tref = 0°C at bottom of columns. Ptotal = 1.902 Watt.

Characterisation
Top level characterisation plan for EV12DS130 - 1/2

Characterisation is a vital part of each project.

The goal is to perform exhaustive series of tests to validate every feature of the device, every performance point described in the product specifications, and how these interact with each other when the device is exposed to a Space environment.

For Advanced Mixed Signal ICs at Microwave frequencies, the duration of the characterisation work can be several months.

It varies typically from 3 months to 1 year depending on the level of innovation of the product, its complexity, the number of product derivatives planned as part of the project and the complexity of the measurements to be made at Microwave frequencies.

Characterisation
Top level characterisation plan for EV12DS130 - 1/2

Characterisation work is fundamental, especially for projects which specifications represent a performance breakthrough, i.e. first 12bit DAC covering L, S and C Band at Fout.

The Quality of Characterisation determines the following:

- The chip designers' level of understanding of the µW MS design.
- The quality of the datasheet (avoiding loose min and max values).
- The quality of the ATE test plan. i.e. how to set the right min and max test values to deliver good products and prevent risks of "No-Yield" situations.

Experience has shown that in order to secure project schedule, and in order to keep project budget under control, for µW MS ICs it is worth investing on Characterisation capabilities:

- Seek for highly experienced engineers.
- Lab equipment investment.
- ATE Characterisation time slots.

Characterisation
Top level characterisation plan for EV12DS130 - 1/2

DC CHARACTERISATION MEASUREMENTS

- DC PERFORMANCE
  - Gain DC Performance in nominal conditions
  - DC Gain distribution
  - DC Gain versus power supplies
  - DC Gain versus temperature
- DIGITAL FUNCTIONS
  - VIL and VIH in typical conditions
  - VIL and VIH versus power supplies
  - VIL and VIH versus temperature

AC PERFORMANCES

- OUTPUT POWER VERSUS OUTPUT FREQUENCY
  - 45 different measurement items under different combinations of operating conditions.
- TYPICAL SPECTRUMS
  - Multiple modes in multiple Nyquist zones
- HIGH SPUR LEVEL, SFDR, FC/2 AND FC/4 FOR DIFFERENT MODE AND OUTPUT DATA
  - Fc: 3GHz versus mode at different Fout
  - High Spur level, SFDR versus mode at different Fout <MUX 4:1 and 2:1>
- SFDR VERSUS POWER SUPPLIES
  - Fc: 3GHz versus mode at different Fout
  - SFDR versus mode at different Fout <MUX 4:1 and 2:1>
- SFDR VERSUS TEMPERATURE
  - Fc: 3GHz versus mode at different Fout
  - SFDR versus mode at different Fout <MUX 4:1 and 2:1>
- SFDR VERSUS DATA INPUT LEVEL
  - Fc: 3GHz_Fout:1.6GHz0dBFS for min; typ and max power supplies
  - Fc: 3GHz_Fout:1.6GHz0dBFS for min; typ and max temperature
- IUCM ACTIVATED: SFDR VERSUS POWER SUPPLIES
  - Fc: 3GHz versus mode at different Fout
- IUCM ACTIVATED: SFDR VERSUS TEMPERATURE
  - Fc: 3GHz versus mode at different Fout
- NPR, SNR AND ENOB
  - NPR, SNR and ENOB versus mulitple combionations of operating conditions

OUTPUT BANDWIDTH

- Output Bandwidth versus power supplies
- Output Bandwidth versus temperature

CLOCK INPUT

- Clock input power
- Common mode
- Differential input resistor

ANALOG OUTPUT LEVEL

- Analog output level in typical conditions
- Analog output level versus power supplies
- Analog output level versus temperature
- VSWR

Characterisation
Top level characterisation plan for EV12DS130 - 2/2

SWITCHING PERFORMANCE
- CLOCK INPUT
  - Fc min and max in typical conditions
  - Fc min and max versus power supplies and temperature
- MINIMUM ANALOG INPUT FREQUENCY IN TYPICAL CONDITIONS
- RISE TIME FALL TIME DATA OUTPUT
  - TR & TF in typical conditions
  - TR & TF versus power supplies
  - TR & TF versus temperature
- PSS (PHASE SHIFT SELECT FUNCTION)
  - PSS in typical conditions
  - PSS versus power supplies
  - PSS versus temperature
- OCDS (OUTPUT CLOCK DIVISION SELECT FUNCTION)
  - OCDS versus power supplies
  - OCDS versus temperature
- TDSP, PIPELINE DELAY AND SYNC TO DSP
  - MUX4:1
  - MUX2:1
- TOD IN TYPICAL CONDITIONS
- SYNC TO DSP

MAX RATINGS
- POWER SUPPLY: VCCA5
- POWER SUPPLY: VCCA3
- POWER SUPPLY: VCCD
- INPUT CLOCK: CLK
- DIGITAL CONTROL: OCDS MODE

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Characterisation.
Multi-dimensional measurements data sets
Example of EV10AS180 ADC dynamic performance.

Conditions:

Nominal Power supplies

Typical Temperature

FClock = 1.5GSps - PClock=10dBm

Functionalities = nominal setting

DMUX Ratio = 1:4

Combining different sets of conditions with all possible sets of variables leads to large amounts of measurements.

This is sometimes best performed on ATE test machines in a way that is representative of production test.

Variable:

Part = on soldered evaluation board

Fin = 10MHz, 100MHz, 500MHz, 750MHz, 1000MHz, 1500MHz &1800MHz

Ain = -1, -3, -8, -12dBFs

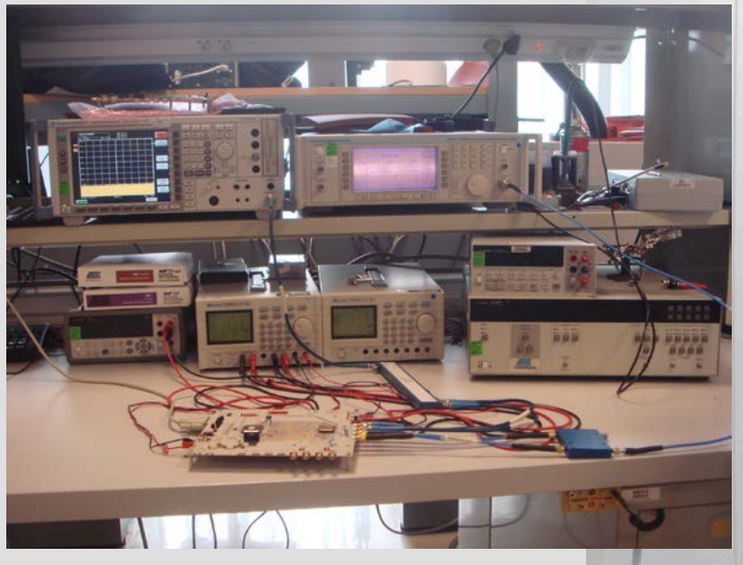
Fin (MHz)	Ain (dBFs)	THD (dBFs)	SINAD (dBFs)	SFDR (dBFs)	SNR (dBFs)	ENOB Bit_Fs	SFSR dBFs
10	-1	-54,12	51,34	-56,14	54,59	8,24	-0,97
	-3	-58,30	53,10	-65,62	54,66	8,53	-2,96
	-8	-59,37	53,52	-65,88	54,83	8,60	-7,99
	-12	-59,90	53,80	-63,13	55,03	8,64	-11,98
100	-1	-54,95	51,69	-57,06	54,47	8,29	-0,98
	-3	-58,98	53,28	-66,02	54,65	8,56	-2,97
	-8	-58,77	53,27	-65,84	54,71	8,56	-8,01
	-12	-59,63	53,65	-62,37	54,92	8,62	-12,03
500	-1	-54,47	51,19	-56,63	53,94	8,21	-1,01
	-3	-58,27	52,78	-64,71	54,22	8,48	-3,00
	-8	-58,89	53,30	-66,08	54,70	8,56	-7,93
	-12	-59,43	53,62	-62,02	54,94	8,61	-11,91
750	-1	-55,22	51,26	-57,94	53,49	8,22	-0,98
	-3	-58,76	52,67	-65,33	53,90	8,46	-2,95
	-8	-58,78	53,22	-65,01	54,64	8,55	-7,93
	-12	-59,77	53,70	-62,97	54,93	8,63	-12,57
1000	-1	-56,91	51,34	-61,97	52,75	8,24	-1,00
	-3	-58,34	52,19	-65,68	53,40	8,38	-2,91
	-8	-58,31	52,89	-64,09	54,36	8,49	-7,96
	-12	-59,34	53,43	-62,13	54,71	8,58	-11,97
1500	-1	-57,67	50,39	-62,08	51,29	8,08	-1,01
	-3	-57,88	51,20	-65,04	52,25	8,21	-2,92
	-8	-59,15	52,73	-66,19	53,86	8,47	-7,93
	-12	-59,69	53,39	-62,55	54,55	8,58	-11,92
1800	-1	-52,44	48,22	-54,90	50,29	7,72	-1,04
	-3	-54,79	49,75	-58,96	51,38	7,97	-2,97
	-8	-58,37	52,25	-64,50	53,46	8,39	-7,93
	-12	-59,30	53,08	-62,15	54,26	8,52	-11,91

From characterisation lab to the test floor… Checking consistency of measurements.

Characterisation and test of Microwave MS ICs requires are demanding for equipment and methodology.

Production testing of µW MS ICs often require customised ATE Test tooling and test setups.

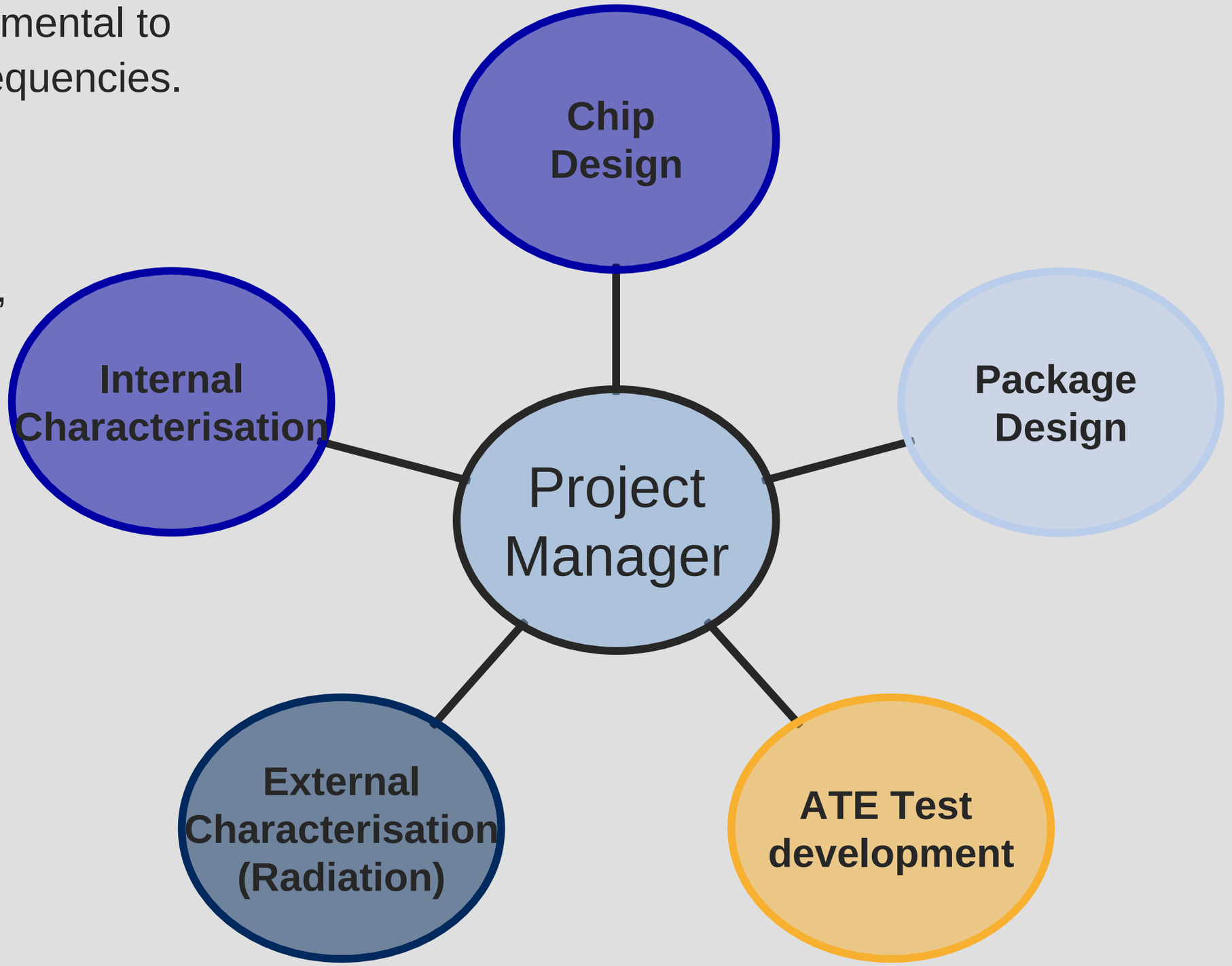
It is highly recommended to ensure consistency of measurements between lab characterisation and ATE test datasets.



Conclusion

Team interaction is fundamental to success at Microwave frequencies.

To achieve breakthrough Innovation in µW domain, Experience shows that thorough understanding of µW phenomenon greatly benefits from combined views of the different teams.



Conclusion

Investing in package development and characterisation was necessary to achieve performance breakthroughs, and to have better control of project schedule and costs.

Future research areas include - but are not limited to – space grade flip-chip assembly technology.

From a performance point of view,

The goal is to expand leadership in data converter speed, microwave bandwidths and dynamic range to enable the deployment of Software Defined Microwave applications and to enable further innovation in the following applications areas:

- MPA digital feedback loops.
- Telecommunication payload’s transceivers.
- Spaceborne SAR payloads.
- Spaceborne LIDARs.
- Satellite Navigation Signal Control loops.
- Encrypted downlink modems (>20Gbps) for earth observation spacecrafts.

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