Challenges of Mixed Signal Space grade ICs operating at Microwave frequencies.

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1. ABSTRACT AND INTRODUCTION

When developing space grade mixed signal ICs such as data converters operating at Microwave frequencies, significant challenges appear during the silicon design part of the project.
But in order to secure the implementation of operational, mature and reliable manufacturing processes such that the Space industry can be confident about sourcing this component for a minimum period of time of approximately 2 decades, technical challenges become significant and require advanced planning within the framework of the project for the following aspects:

a. The design of an optimised space grade package which both meets space reliability requirements and mixed signal analogue performance targets at microwave frequencies.

b. The characterisation plan of the device so to have a thorough measured performance assessment of each silicon revisions created by the design team during the project, and provide reliable measurements to make decision about whether a silicon revision is mature enough to be taken into production or whether a re-design is necessary.

This paper addresses the above topics with the goal of providing some useful insights into the technical challenges which determine a company's ability to successfully conclude a mixed signal IC project for space applications when operating at Microwave frequencies.
To support the concepts, examples of the work done by e2v on ESA/ESTEC ITT for a 10bit 1.5GSPS ADC [1], [5] , as well as a 12bit 3GSPS DAC [1] , [2], [3], [4] sponsored by CNES will be used.

2. DESIGN OF AN OPTIMISED SPACE GRADE PACKAGE

Case study of the package design for ESA ITT ADC EV10AS180 10bit 1.5GSPS L-Band ADC [1], [5].

2.1. Objectives and constraints.

Following to initial evaluations as part of the project, the decision was made to design a CI-CGA 255 package (Column Interposer – Column Grid Array type of package with 255 columns).
The package specifications were : hermetic package, dimensions 21mm x 21mm, 1.27 mm pitch.

The product's key electrical specifications which the package had to accommodate were as follows:

- ADC low jitter Clock frequency : 1.5GHz.
- 3dB Analog Input Bandwidth : 3GHz.
- 1st Nyquist zone gain flatness : ≤ 0.5dB.
- 2nd Nyquist zone gain flatness : ≤ 0.5dB.
- 3rd Nyquist zone gain flatness : ≤ 1.0dB.

Data output format : 10 bits - LVDS format - Demultiplexed output to accommodate I/O speeds with lower data rates on the signal processing unit than on the ADC output, supported DMUC ratios are 1:4; 1:2 and 1:1

LVDS Data, clock input and analog inputs are all differential signals, single ended signals are not supported by this device.

Routing inside the package needed to be designed to achieve 50Ω differential impedance inside the package. Consequently routing segments with differential impedance in excess of 50Ω need to be considered as inductive segments and those with differential impedance lower than 50Ω need to be considered as capacitive segments.

Because of the microwave frequencies that the device was designed to operate at, the use of electrolytic Nickel & Gold plating using plating tie bar was to be excluded.
The reason for excluding this option is that plating tie bars behave like stubs at microwave frequencies and create capacitive effects which would significantly degrade the overall specified dynamic performance of the device.

Final package drawing can be found in the datasheet of EV10AS180 ADC [5]

2.2. Package routing and design challenges.

Based on the initial routing works and past experience it appeared not possible to route all the traces on single deck.
Several reasons led to this conclusion among which is the fact that HTCC (High Temperature Cofired Ceramic) technology does not support very narrow traces, also in order to meet space grade requirements it was necessary to adopt conservative rules in order to meet the quality requirements of the largest possible number of users of the EV10AS180 ADC [1], [5].

Consequently the chosen pitch value was the smallest pitch which could still be considered as safe and acceptable by the project team as well as the project partners: that is 260µm.
The combination of chosen pitch, chosen package dimensions and the number of traces to implement led to double-deck package structure.

The double deck structure is designed in such a way that traces of the upper deck do not overlap the traces of the lower deck. See Fig 1. below.
But it is necessary to seek for the best trade-offs at microwave frequencies between avoiding upper deck and lower deck trace overlaps and achieving short enough trace lengths on the upper deck.

In this case, typical "long" wires length on the upper deck is 2.55mm long, and while short wires on the lower deck are 1.27 to 1.28mm long and should be used to route sensitive signals such as analog inputs at microwave frequencies.

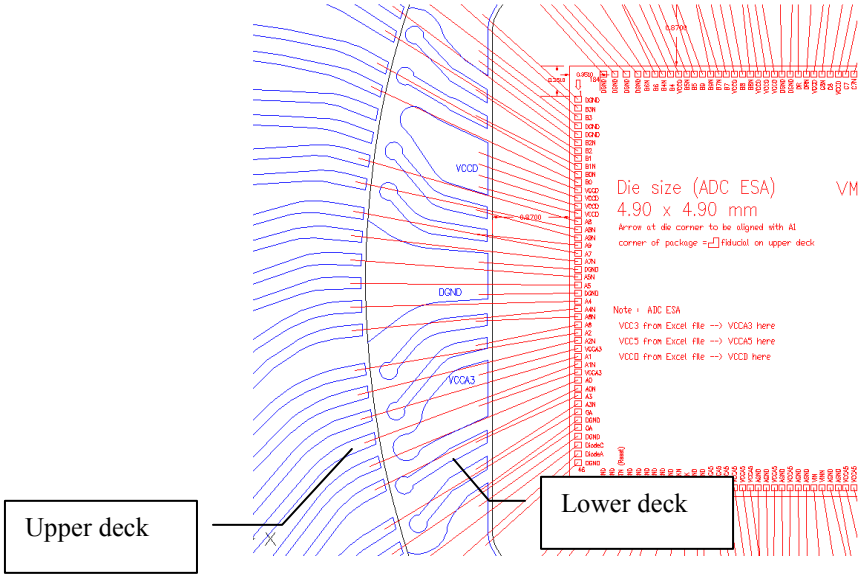

Fig 1.: Illustration of upper deck and lower deck routing on West side.

In order to accommodate valid and proper visual inspection after wire bonding, there needs to be constraints on wire placement and wire angle with the edge of the die.

Special care needs to be taken to route the analog input of the ADC which is specified to operate at the above mentioned microwave frequencies.
Both differential lines called VIN and VINN are protected both and trace level and wire bonding level by GND wires and GND traces or large GND areas on each side.
At column level, Vin and VINN are surrounded by 6 Analog GND columns.
This ensures optimum protection of the analog microwave line from the solder joint on the PCB all the way to the wire bonding pads at die level.

Some technical challenges can also be expected to manage good coplanarity as well as different gold thicknesses for wire bonding on the top side and for industry standard column attach at the bottom side. This requires experience and proper planning to make the right choices, the right design and preparation that are needed to achieve a reliable and sustainable production flow.

2.3. Package electrical performance and simulations.

Extensive electrical simulations of the package design are required in order to secure a package design which will support the targeted electrical performance at microwave frequencies.

As part of this project 2 different simulation tools have been used. Linpar and HFSS (High Frequency Structure Simulator) version 11.

At the frequencies of interest, modelisation of the skin effects happening inside the package traces and the wire bond are necessary.

About the importance of 3D electromagnetic simulation:
This type of simulation was done using HFSS v11 and has been very useful for exhaustive and accurate calculation of S-parameters of the full package structure. This was necessary to achieve accurate optimisation of the package design at microwave frequencies.
The HFSS tool divides the detailed and accurate geometric model into a large number of tetrahedra where a single tetrahedron is a four-sided pyramid.
The resulting collection of tetrahedra is referred to as the finite element mesh.
This tools is useful and necessary to compute the generalised S-matrix from the amount of reflection and transmission that occurs in and around the structure.
The resulting S-matrix allows to reduce the full 3D electromagnetic behaviour of the package structure to a set of high frequency circuit parameters.

In this project, the HFSS v11 tool has been used to investigate and to find the best package configuration to take the analog input signals at Microwave frequencies from the solder joint at PCB level to the ADC die pads through multiple differential line segments inside a space grade ceramic package.
S11 and S21 parameters have been the subject of deep analysis and optimisation work to achieve the best possible signal transmission through the package and secure the guaranteed electrical performance of EV10AS180 ADC in its space grade version without noticeable degradation.

The same package design was used for the EV12AS130A 12bit 3GSPS C-Band DAC with satisfactory microwave performance.

About capacitance and inductive effects on power lines:
A challenge with the Vcco line on the above mentioned ADC is noise on the digital power plane.
Although the chosen technology for this ADC design being purely bipolar is strongly favourable on this aspect current transient being reduced in magnitude by a factor ranging from 5 to 10 compared to similar ADC architecture built on a CMOS technology, it is still important to seek for optimisation even at package level.
The goal with capacitance on power lines being to smoothen the propagation of current transients on the digital supply so that they do not affect the analog part of the circuit.
The risk would be the appearance of the unwanted spurs at frequencies that are multiple of a quarter of the clock frequency.
To reach optimised levels of decoupling, there are capacitances built on-chip as well as at package level.

Reduction of inductive effects on the supply and GND lines are very important.
In this project, inductive and resistive effects at package level are very low due to the use of 62 Digital ground columns and 34 Analog ground columns. Cf package drawing and pinout details in the datasheet of EV10AS180 [5].

2.4. Package thermal modelisation and simulations.

Thermal simulation of the package was done using ANSYS v11 simulation tool.
This software allows for accurate finite elements calculations of thermal performance of the package structure.

At the initial stage while the silicon design was not yet completed and the elementary silicon heating blocks were not yet known, the first package thermal simulations were done assuming a single square heating area at the centre of the die. Based on past experience at e2v this assumption has proven to be close to the real behaviour of final silicon if it is assumed that the heating area is equal to 25% of the overall die surface and if it is located at the centre of the die.

In the above mentioned ADC project, the die size is 4.88 x 4.88 mm, therefore initial thermal simulation and calculations were done assuming a single heating area of 2.44 x 2.44 mm.
These calculations revealed that the thermal resistance of the chosen package design would provide a thermal resistance from junction to bottom of columns ranging from 9.23°C/W in the case of 380µm silicon thickness to 9.68°C/W in the case of 380µm silicon thickness.

Later in the project, the design team was abel to release a detailed list of heating blocks on the die.
This has allowed to perform detailed thermal simulations and calculatins of thermal resistance using 610 elementary heating blocks.
The detailed analysis performed using a fine and accurate mapping of elementary heating blocks revealed that this ADC in this package has 2 maximum hot spots with die temperature of only 20°C higher than the temperature of the bottom of the columns at PCB level. This leads to the conclusion that this ADC in its space grade package will have no thermal issues.
Accurate calculations of the thermal resistance from junction to board according to JEDEC JESD51-8 reveal a value of 12.58°C/W.

4. CHARACTERISATION

Characterisation is a vital part of each project, it is the mission of a dedicated team called the characterisation team.
The goal is to validate every feature of the device, every performance point described in the product specifications, and how these interact with each other.
i.e. using a combination of different features in specific operating conditions may deteriorate the overall dynamic performance or cause unexpected and unwanted spurs at microwave frequencies.

The characterisation team can be viewed as being as vital as the test pilots performing aircraft qualifying test flights for aircraft manufacturers.

During the design stage, designers do everything that is possible to create a product matching the original specifications, and to predict what the real silicon behaviour of their design will be. This includes of course extensive simulation work in order to eliminate as many unknown and uncertainties as possible prior to foundry stage.
Then once the design team has completed its work, as soon as the silicon is released by the foundry and is assembled in a package, the characterisation team will start a series of exhaustive test and measurements which goal is to demonstrate how does the overall silicon behaviour compares with the original specifications.

This work results into a very detailed characterisation report with a typical length in excess of 100 pages.
The characterisation report is a reference document of primary importance for the design team.
It allows IC designers to know what is the real behaviour of each feature and performance parameter that they intended to build in the silicon.

After each silicon release, a detailed review of the characterisation work is the basis for very important project decisions such as designing a new silicon revision or deciding that the current silicon revision is approved to be taken into a production status.

The duration of the characterisation work can be several months and varies typically from 3 months to 1 year depending on the level of innovation of the product, its complexity, the number of product derivatives planned as part of the project and the complexity of the measurements to be made at Microwave frequencies.

In addition, for early silicon revisions of a product which specifications are performance breakthroughs compared to existing devices, it should be expected that the characterisation team discovers some functional bugs and noticeable performance gaps versus the original specifications.
In such cases the design team and characterisation team need to work very closely together and need to interact effectively in order to identify, to perform and to analyse the necessary additional series of measurements which will allow the project teams to understand and address the root causes of each problem.
This leads to additional project time spent for characterisation and design which is difficult to plan during the early stages of the project, but it is a challenge that the project team needs to undertake and to overcome in order to release new ICs with significant increase of performance compared to previous products available on the market.

This thorough and detailed analysis of the device behaviour is then required for every new silicon revisions within the life of the project.

Performing thorough silicon characterisation for mixed-signal Microwave ICs requires significant investment in lab equipment. The first expenditures to plan for are high-end signal generators, spectrum analysers, oscilloscopes, logic analyzers, but also other interacting equipment needs to be carefully selected in order not to degrade the quality and validity of the complex measurements that the characterisation team needs to make at Microwave frequencies.

The characterisation challenges are similar for commercial versions and space versions, both require extensive multi-dimensional sets of measurements, but with the following additional aspects applying to space grade ICs:

a. Space versions require ceramic packages which are bigger than commercial plastic versions, this leads to increased inductive effects in the package which can hinder the dynamic performance at Microwave frequencies. Test tools, evaluation boards and characterisation benches often need to be specifically designed, prepared and built to accommodate these differences.
b. Thermal performance of ceramic packages can be noticeably different compared to plastic versions
c. Space versions of any ICs operate over wide temperature ranges. For the characterisation team this creates challenges to make complex measurements at microwave frequencies while exposing the device under test to different temperatures which are within and beyond the specifications of the IC. Long series of measurements need to be repeated at multiple frequencies, then the results that are already multi-dimensional at single temperature due to the combinations of various frequencies (clock and signal),

various operation modes, various supply voltages etc... need to be correlated compared taking into account a new and additional dimension that is temperature.

In summary, for microwave mixed-signal IC projects, characterisation plays a key role providing extensive series of sets of measurements which are fundamental to the project milestones.
It is the project phase where all bugs and performance mis-matches are revealed, analysed and de-bugged while working under tight project deadlines.
Characterisation provides factual data used as a basis for decision to either start a new silicon revision or to take the current silicon revision to production for flight models.
Characterisation should be given a level of importance that reflects the importance of the decisions that are made based on the characterisation results, that is either to go into production or to re-design with the associated additional projects costs and delays.

While conducting a project of any new high performance mixed-signal microwave ICs, it is important to gather a characterisation team composed of experienced engineers who have previously performed similar work.
Similarly to the design team, if the goal of the project is to release a new IC with unprecedented levels of performance, then it is a necessity that the team be made of highly skilled characterisation engineers who have gained sufficient lab know-how and experience to perform this work thoroughly, revealing and documenting systematically each silicon performance gaps or bugs and leading the project team to new debugged silicon revisions under short schedules.

As an example, below is typical characterisation plan that reflects what has been done on e2v's EV10AS180 10bit 1.5GSPS L-Band ADC [1], [5] and EV12DS130A 12bit 3GSPS S-BAND DAC [2], [3], [4].

Table : Top level characterisation plan typical of EV12DS130 – Please refer to the datasheet of EV12DS130 [4] for details of the product terminology.

DC CHARACTERIZATION MEASUREMENTS

DC PERFORMANCE

Gain DC Performance in nominal conditions
DC Gain distribution
DC Gain versus power supplies
DC Gain versus temperature

DIGITAL FUNCTIONS

VIL and VIH in typical conditions
VIL and VIH versus power supplies
VIL and VIH versus temperature

AC PERFORMANCES

OUTPUT POWER VERSUS OUTPUT FREQUENCY

45 different measurement items under different combinations of operating conditions.

TYPICAL SPECTRUMS

Multiple modes in multiple Nyquist zones

HIGH SPUR LEVEL, SFDR, FC/2 AND FC/4 FOR DIFFERENT MODE AND OUTPUT DATA

Fc: 3GHz versus mode at different Fout
High Spur level, SFDR versus mode at different Fout <MUX 4:1 and 2:1>

SFDR VERSUS POWER SUPPLIES

Fc: 3GHz versus mode at different Fout
SFDR versus mode at different Fout <MUX 4:1 and 2:1>

SFDR VERSUS TEMPERATURE

Fc: 3GHz versus mode at different Fout
SFDR versus mode at different Fout <MUX 4:1 and 2:1>

SFDR VERSUS DATA INPUT LEVEL

Fc: 3GHz_Fout:1.6GHz0dBFS for min; typ and max power supplies
Fc: 3GHz_Fout:1.6GHz0dBFS for min; typ and max temperature

IUCM ACTIVATED: SFDR VERSUS POWER SUPPLIES

Fc: 3GHz versus mode at different Fout

IUCM ACTIVATED: SFDR VERSUS TEMPERATURE

Fc: 3GHz versus mode at different Fout

NPR, SNR AND ENOB

NPR, SNR and ENOB versus mulitple combionations of operating conditions

OUTPUT BANDWIDTH

CONCLUSION

Package design and extensive product characterisation have proven to be fundamental project phases of microwave mixed signal ICs in space grade versions.

In the future, e2v will continue to build on the experience gained through time and through the ESA and CNES programmes for the development of space grade ADCs and DACs.
The goal being to seek for further innovation breakthroughs at microwave frequencies.
Research areas include - but are not limited to – space grade flip-chip assembly technology.

From a performance point of view the goal is to expand the European leadership in data converter speed, microwave bandwidths and dynamic range to match the most demanding needs for telecommunication payloads, spaceborne SAR payloads, Spaceborne LIDARs, Satellite Navigation Signal Control loops and Gbps encrypted downlink modems for earth observation spacecrafts.

REFERENCES

[1] A. Glascott-Jones, M. Wingender, F. Bore, N. Chantier, "Using e2v's High Speed Space Grade ADC and DAC to achieve direct conversion of L band Signals", in Proc. 12 International Radar Symposium, Leipzig, Germany, 8-10 September 2011,pp 829-834.

[2] F. Boré, N. Chantier "3 GS/s S-Band 12 Bit MuxDAC on SiGeC Technology",in *Proc. 18th International Conference on Microwave Radar and Wireless Communitation*, MIKON 2010,Vilnius, Lithuania 14-16 June 2010, pp 600-603

[3] F. Boré, M. Wingender, N. Chantier, A. Glascott-Jones, E. Dumaine, C. Lambert, S. Calais, "3 GS/s 7GHz BW 12 Bit MuxDAC for Direct Microwave Signal Generation over L, S and C Bands",in *Proc. 2011 IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems*, Tel Aviv, Israel 7-10 November 2011 (IEEExplore Digital Object Identifier: 10.1109/COMCAS.2011.61055887)

[4] EV12DS130AMGS Datasheet "12bit 3GSPS Digital to Analog Converter" - e2v - 2012.

[5] EV10AS180A Datasheet "10bit 1.5GSPS Analog to Digital Converter" – e2v - 2011.

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