EVALUATION OF THE *AMS* 0.35 μM CMOS TECHNOLOGY FOR USE IN SPACE APPLICATIONS

AMICSA 2012

26-28 August 2012

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INTRODUCTION

The design of mixed-signal application specific integrated circuits (ASICs) requires a detailed knowledge of the behavior of the technology which exceeds the needs of digital designs. For space applications, with its extended-temperature and radiation environment, the job of the mixed-signal designer is made even more difficult as in most cases commercial foundries do not have or make available data on the behavior of their devices under those non-standard conditions.

Instituto de Microelectrónica de Sevilla and Universidad de Sevilla (IMSE-US) have started a long term collaboration with the Spanish Instituto Nacional de Técnica Aeroespacial (INTA) to extend its experience on mixed-signal design to the field of ASICs for space applications. The initiative is partially funded by the Spanish National Research Program.

The first step has been to develop a plan to assess and characterize a commercial (*ams*) 0.35μm CMOS technology when exposed to radiation or to temperatures below the standard industrial or automotive ranges. Development of a Radiation-Hardened-By-Design (RHBD) digital library is also in progress. The results are being initially applied in the design of two instrumentation ASICs for missions to Mars.

THE CHARACTERIZATION PLAN

The activities being carried out for characterization of the technology intend to cover all aspects which are relevant for space applications:

- Development of a test setup, including the design of test ASICs
- Behavior of devices at temperatures down to -110ºC
- Equivalent device width for enclosed layout geometries
- Total Ionization Dose (TID) influence on threshold voltage and leakage current
- Single-event effects (SEE), including single-event upsets (SEU) and latch-up
- Design of a basic RHBD digital library

Test Plan

To fulfill the objectives of the characterization plan, a number of tests are being carried out. Those experiments have needed the design and development of test chips, test hardware and software, protocols, and software for data processing and analysis. The two main experimental lines have been directed to evaluate the impact of low-temperature, and radiation (TID and SEE).

Test Chips

Three different test chips have been designed. A multipurpose test chip (CHIP#1) has been prototyped and characterized to obtain a preliminary experimental evaluation of all aspects covered by the characterization plan. Its design has been reused to manufacture a second chip (CHIP#2) with additional transistor sizes. The third test chip (CHIP#3) only has digital blocks to characterize and compare SEEs in the standard and RHBD digital libraries.

CHIP#1 contains five arrays of 4 x 4 CMOS transistors with different layout geometries and sizes; resistors of all the types available in the technology; digital circuits (ring oscillators and shift-registers) for evaluation of SEU and latch-up; structures to verify the efficiency of guard rings to protect against latch-up; lateral and vertical bipolar devices; and two instantiations of a band-gap circuit, one with standard layout and another using radiation-hardened NMOS transistors. The transistor arrays are multiplexed to allow access to a maximum of 80 transistors using only 17 package pins. The chip design is reusable by replacement of the transistor arrays in the layout. The transistors in the arrays are connected to the test equipment by proper driving of their terminals through transmission-gate multiplexers built with thick-oxide PMOSM and enclosed-layout NMOSM devices. Fig. 1 shows a simplified schematic of one of the arrays. One of the pins in the chip sets the bias of all transistors to worst-case conditions for irradiation (gate to V_{dd} and all other terminals grounded).

Fig. 2 shows the four different transistor layout geometries for NMOS transistors of thin- (NMOS, PMOS) and thick-oxide (NMOSM, PMOSM) that have been evaluated: standard (S), ringed-source (RS), double ringed-source (DRS) and annular or enclosed (E) [1, 2].

For accurate measurements, the effect of the parasitic resistance of the on-chip multiplexers has to be compensated,. In addition, when small currents have to be measured, the ESD protection pads and the on-chip multiplexers contribute to parasitic leakage that distorts the results. Dummy devices (open/short) are included in the arrays for compensation of those parasitic effects. Nevertheless, the accuracy that can be achieved in the very low current ranges needed for characterization of leakage currents is still limited by experimental errors (wiring) and by the leakage currents flowing trough devices placed in parallel with the DUT in the same column of the transistor arrays. Accuracy in leakage current measurements can be improved by placing multiple instances of transistors with lower transconductance, and by placing in the same array column transistors with similar levels of expected leakage current.

Test Hardware

Hardware For TID Tests

A test setup has been designed having in mind the need to perform measurements in locations outside IMSE laboratories. The central element for device characterization is an HP-IB controlled HP-4155 Semiconductor Parameter Analyzer. A custom-designed matrix switch board controlled through a USB link reconfigures the connections of the HP-4155 measuring terminals, and also holds the configuration bits for the test ASIC. A PC controls the HP-IB and USB buses and generates the test sequence commands for characterization of all individual devices in the chip (CMOS

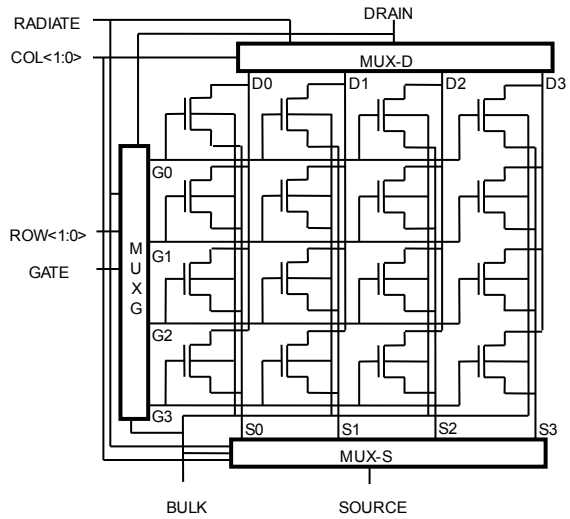

Fig. 1: Column selection connecting Sx and Dx to SOURCE and DRAIN. Row selection connecting the Gy to GATE. RADIATE controls irradiation biasing.

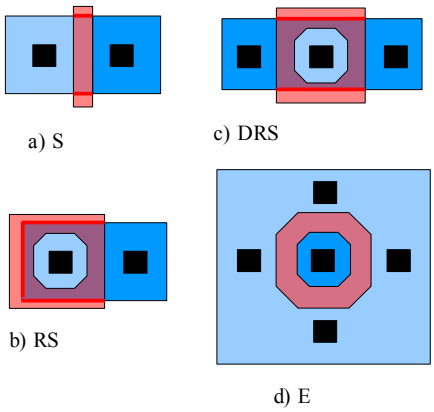

Fig. 2 : NMOS Layout Styles. a) Standard; b) Ringed-Source; c) Double Ringed-Source; d) Enclosed

transistors, bipolar transistors, resistors). The same PC is used to capture, store and analyse the data needed for off-line extraction of the CMOS parameters using specifically developed routines.

Two levels of signal multiplexing are used for the characterization of the devices. One is internal to the test chip, as described above; the second is external to the chip, using a custom-designed reed-relay switch-matrix board, connected to a PC through an USB line. The characterization of each device makes measurements to extract the following parameters: threshold voltage (V_{th}) in saturation and linear regions, gain factor, mobility, body-effect factor, saturation current and leakage current. The complete measurement of all devices in an ASIC needs 90 minutes to complete.

Hardware For SEE Tests

To test the devices with heavy-ion beams, a custom FPGA-based test board was developed as well as the associated control software running on a PC. All communication with the PC is made through a USB port.

For SEU, the FPGA provides the excitation in parallel to several long shift registers in the test chip. The outputs of the shift-registers are then monitored for errors, one at a time, by comparison with a delayed version of the applied input. Errors are accumulated in the FPGA and transmitted periodically to the PC.

For latch-up evaluation, the board contains six channels of latch-up detection and release circuits. The FPGA manages autonomously the latch-up occurrences in up to six different power supplies, stores the detected latch-up events, and transmits them periodically to the PC.

Test Software

A large amount of test-bench automation software has been developed for control of the test boards, the parameter analyzer and the acquisition of data both for TID and SEE experiments (using Visual Basic). Additional functionality is provided by the developed software to postprocess captured data, extract device parameters, and visualize in graphical form results from different sets of devices, dates and test conditions (using MATLAB-based routines).

Test Facilities

The irradiation of the devices for evaluation of total dose effects has been carried out in the facilities of the Laboratorio de Radiofísica of the Universidad de Santiago de Compostela (Spain). The laboratory has a fully equipped Co-60 source, including dosimetry equipment to monitor the actual amount of radiation received by the samples. Achievable dose rates, controlled by changing the source-target distance, fall in a range of 40 rad/hr (0.012 rad/s) to 10 krad/hr (2.7 rad/s).

Temperature tests have been performed at IMSE-US, and INTA. Low-temperature tests at IMSE's laboratories are limited to -55ºC, by the equipment available (Thermonics T-2650BV). Tests at lower temperatures have been performed at INTA, where SUN-Systems thermal chambers cooled by liquid nitrogen are available.

The SEE tests have been made at the Heavy-Ion Irradiation Facility in the University of Louvain-la-Neuve (HIF-UCL), Prior to the tests at UCL, the SEE test system was debugged using a Californium (Cf-252) source at the Centro Nacional de Aceleradores of the University of Sevilla (CNA-US).

LOW-TEMPERATURE CHARACTERIZATION

In applications for missions to the outer planets, ASICs used in instruments that are located in the outside of the spacecraft are exposed to temperatures that fall out of the standard range for which the device models are characterized by the foundries. A solution to this problem is to heat the device to bring it within the standard temperature range, but this is complex to assemble and package, and expensive in terms of power consumption. An alternative approach is to characterize the devices down to the expected temperatures, and design the circuits taking into consideration the additional variation in device parameters.

Low-Temperature Tests

The devices in the *ams* technology have been measured at temperatures down to -110ºC. The measurements were performed with a test board holding the DUT placed inside a thermal chamber, and connected to the Parameter Analyzer by the custom switch-matrix through the port-holes in the chamber.

Low-Temperature Results

The experiments show that the coefficients from the standard design kit model adequately the behaviour of V_{th} and leakage current of thin- and thick-oxide CMOS transistors over the extended temperature range. Except for some resistor types a first order approximation is sufficient to model the change of resistance with temperature.

EQUIVALENT DEVICE WIDTH FOR ENCLOSED LAYOUT TRANSISTORS (ELTS)

The use of layout styles that eliminate or reduce leakage currents along the edge of the bird's beak oxide uses transistor shapes that are not covered by the standard models and extraction tools. As can be seen in Fig. 3 the additional overlap of the gate over the active area creates extra channel paths for the current to flow from source to drain producing an increase in the transconductance that can be modelled by calculation of an equivalent device width based on geometry parameters. Reference [3] presents an approximation to deal with the change in geometry for ELTs. Comparison of the predictions of [3] with our experimental results give a maximum error in the order of 15%, for the smaller transistors contained in CHIP#1.

For transistors with small dimensions using enclosed layouts, when working in saturation mode and biased at maximum V_{GS}, the drain curent (I_d) due to the increased transconductance can exceed the recommended current capability limit of a single drain/source contact and affect long-term reliability. This can be remedied by additional contacts rows in the drain and source areas, as shown in Fig. 3, but the additional extension of the side channel has to be taken into account in the extraction of the equivalent width.

We have developed a new approximation based on [3] that gives a better fit with our results and is also able to deal with multiple contact rows. For the ringed-source type, the effective width is given by:

$$W_{eff} = W + 2 \cdot L \cdot [\frac{W_2}{L_2} + (\frac{2 \cdot n_c + 3}{4}) \cdot \frac{W_3}{L_3}] \quad (1)$$

with n_c being the number of contact rows in the source terminal, and W_x, L_x as indicated in Fig. 3.

In the case of the double ringed-source device, our approximation is:

$$W_{eff} = 2 \cdot W + 4 \cdot L \cdot [\frac{W_2}{L_2} + (\frac{n_c + 5}{6}) \cdot \frac{W_3}{L_3}] \quad (2)$$

both formulae reduce the error in the estimation of the saturation current for small thin- and thick-oxide devices to less than 5% for the transistors included in CHIP#1. Evaluation of the accuracy for the devices contained in CHIP#2 is pending.

For annular devices the approximation given in [4, 5], with $\alpha = 0.05$, and K equal to 4 if $L > 0.5$ μm or $K = 3.5$ in all other cases, gives results that agree with our experiments within 2%.

These approximations have been implemented in a modified version of the design kit's transistor models and in the extraction tools.

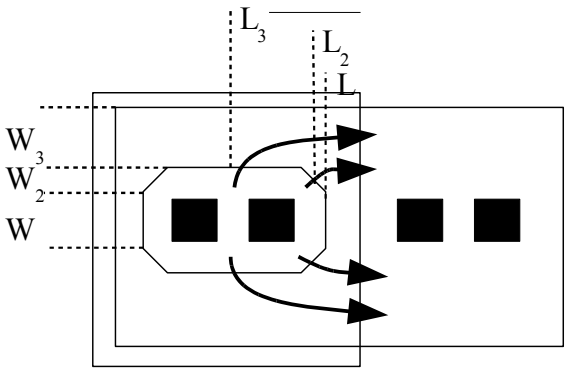

Fig. 3: Side-channels in ringed-source NMOS

TID CHARACTERIZATION

TID Tests

Before commiting a costly TID measurement campaign, a one-day preliminary test, reaching 65 krad in four steps (5, 15, 35, 65 krad), was performed to quickly decide if the technology was robust enough to justify investing further resources in more detailed testing. The results were promising, and it was decided to proceed with a complete TID characterization.

CHIP#1

The experiment, carried out over nine days, reached a TID of 350 krad in 8 steps, maintaining constant the irradiation time (~20 hours), and doubling the dose rate for each consecutive step. The dose rate was 70 rad/hr (0.019 rad/s) for the first step

and 8960 rad/hr (2.5 rad/s) for the last step. During irradiation all CMOS transistors were biased for worst-case conditions, with their gates connected to the positive supply and all other terminals grounded. Four samples of CHIP#1 were used. They were irradiated simultaneously during 17 hours at night-time (from 17:00 until 09:00). Then, during daytime the samples were taken one-by-one out of their sockets in the irradiation board and measured in a thermal chamber held at a constant temperature of 25ºC. During the time (90 minutes) needed to measure a sample, the other three continued to be irradiated. Each irradiation /measurement step thus took 24 hours to complete.

Once the irradiation was completed, the four irradiated samples continued to be measured once a week, to monitor its evolution with time at room temperature. After six weeks at room temperature, the samples were annealed 168 hours at 100ºC, the first half of that time unbiased, and the other half with the same bias used during irradiation.

CHIP#2

A second TID campaign was carried out to test the devices in CHIP#2 to a higher total dose, up to 1 Mrad. Given the small effect on parameters of delaying the measurements a few hours, observed in the first TID experiment, this time the devices were sent back and forth by express-courier between IMSE (characterization) and LR-USC (irradiation). A total of six irradiation steps were applied to the devices. In each step the irradiation time was 42 hours. The TID after each step was: 75, 175, 305, 480, 710 and 1010 krad .

The samples have also been measured after three annealing steps. The first step was 16 days at room temperature; second step, 95 hours at 100ºC unbiased; and third step, 73 additional hours at 100ºC, also unbiased.

TID Results

Threshold Voltage Shift

For devices with thin gate-oxide (NMOS, PMOS), the average threshold voltage shift (ΔV_{th}), up to 300 krad, is small (less than 30 mV). Thick gate-oxide transistors (NMOSM, PMOSM) show a significant ΔV_{th} at a dose of 300 krad; an average of +180 mV for PMOSM, and -30 mV (-90 mV worst-case, for minimum dimension transistors) for NMOSM. There is little difference in ΔV_{th} between standard and enclosed layout transistors. However, ΔV_{th} is dependent on device dimension, smaller length and/or width giving larger changes in V_{th}. Fig. 4 presents the ΔVth for NMOSM transistors in CHIP#2, after irradiation to 1 Mrad, and three annealing steps. It clearly shows the dependence with length (0.5, 1 and 3 μm) and with transistor width within each length group.

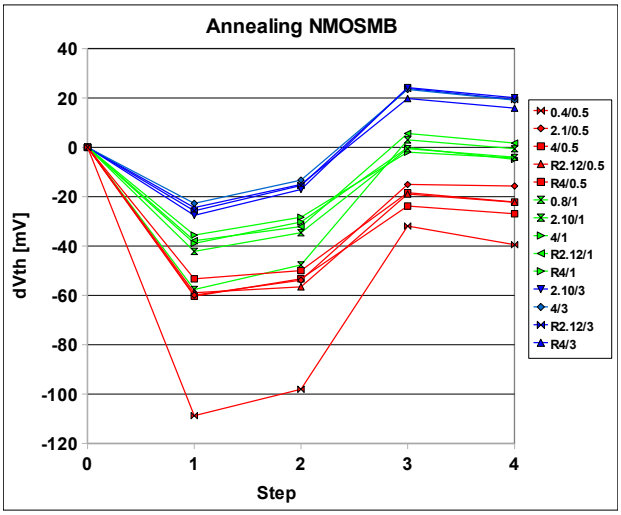

Fig. 4: Dependence of threshold voltage drift on transistor dimensions: 0) before irradiation; 1) 1010 krad; 2) 16 days at 25ºC, unbiased; 3) 95 hours @ 100ºC, unbiased; 4) 73 hours @ 100ºC, unbiased

Leakage Currents

The sub-threshold leakage current (*SLEAK*) is obtained as the linear intercept with the vertical axis of the $log(I_{ds})$ vs. V_{gs} characteristic at maximum V_{ds}. For PMOS and PMOSM, radiation has a noticeable effect on narrow transistors, with *SLEAK* increasing by more than one order of magnitude at 350 krad. In wide PMOS transistors the effect is negligible. NMOS devices show a similar behaviour for narrow transistors, the *SLEAK* increase being smaller for enclosed layout geometries, and for wide transistors. For wide and long NMOS transistors there is practically no increase in *SLEAK* at 350 krad, for either standard or enclosed layouts. Data for zero gate-bias drain-source leakage (*ILDS*) are more difficult to obtain, because, as mentioned before, the increase of *ILDS* in one device affects all devices placed in parallel in the same column of the array. Post-processing permits to partially compensate the effect of paralleled devices, and confirms the efficiency to reduce leakage of enclosed layouts. Improved distribution of the transistors of the arrays was made in the second test chip.

Saturation Current

Changes in the saturation current (*ISAT*) are to be expected because of its dependence on V_{th} and carrier mobility. At 350 krad, *ISAT* shows an average decrease of 20% for PMOSM and 10% for PMOS transistors. Corresponding calculated changes in mobility are -8% and -3%. The average change of *ISAT* at 350 krad for N-channel transistors is negligible, in the order of +2% (NMOSM), and 1% (NMOS).

Bipolar Transistors

At 350 krad, bipolar transistors show a 25% degradation of beta for vertical PNP and 50% for the lateral PNP.

Resistors

There is an increase in the resistance of N-well and high-resistivity poly devices, reaching approximately 6% for N-well and 1.5% for Hi-Poly at 350 krad.

Annealing

Annealing of the CHIP#1 samples was performed in three steps. In the first step, the irradiated samples were kept unbiased at room temperature, and parametric measurements taken once a week during 44 days. In the second annealing phase, the samples were stored unbiased at 100ºC during 70 hours, and parameters measured at the end of that period. Finally, in a third step, the samples were annealed at 100ºC, biased in the same conditions as during irradiation and the parameters measured after 90, 112, 133 and 157 cumulative hours. The most notable behaviour is seen in the thick-oxide NMOSM transistors. At the end of the annealing, short-channel NMOSM devices show a complete recovery of threshold drift with a slight rebound, and almost complete recovery from the increase of leakage currents; but long-channel transistors, for which V_{th} drifted by a small amount during irradiation, present a strong rebound after annealing, stabilizing at a positive threshold shift of 50 mV. For PMOSM, the ΔV_{th} drift recovery is only partial, its average value decreasing from 130 mV after irradiation to 100 mV after annealing.

SINGLE EVENT EFFECTS CHARACTERIZATION

SEE Tests

CHIP#1

CHIP#1 contains a small amount of digital logic, using different layout styles, to get a preliminary evaluation of their SEE performance. The digital part with a total area of approximately 2 mm^2, had three different versions of ring oscillators with 512-stages, and also four different styles (S, RS, E and DICE [6]) of 128-bit shift-registers.

CHIP#3

CHIP#3 has been designed exclusively for the evaluation of SEE and latch-up in the rad-hard library of digital cells. The circuit has been manufactured and the test board debugged. Heavy-ions irradiation is planned at UCL in October 2012.

The chip, with a total area of approximately 9 mm^2, has structures to test for SETs in combinational and sequential circuits (long shift-registers chains). The glitch-capture in the combinational circuits uses the autonomous detection method described in [7]. The standard-library combinational block is formed by eight chains of 130 NAND gates each, giving a total combinational area of ~0.07 mm^2. The inputs to all chains are fixed to logic low. Glitches caused by heavy-ions appearing at the outputs of any of the eight chains are combined by additional gates to give a single glitch at the input of the capture circuit. The combinational block of the rad-hard library is made of 64 chains of 30 NAND gates each, with a total area of 0.055 mm^2. Again, the outputs of the 64 chains are combined to give a single glitch output at the input of the glitch capture circuit. The capture circuit is a 32-stage digital delay-line with the capability to store the transient in a register bank from where it can be retrieved under control of the FPGA.

CHIP#3 also has three shift-register chains to evaluate SEUs in sequential circuits. They have been sized taking into account the SEU results from CHIP#1. One shift-register (CMOS) is made with standard-library cells. Because they have the highest SEU probability, the chain does not need to have a very large area. It has 255 stages, with an area of 0.1 mm^2. The second shift-register is built with ringed-source NMOS transistors. Its SEU error rate is smaller than for

CMOS, and therefore a larger are will be needed to obtain a statistically significant number of errors; it is made of 510 stages, and occupies 1.6 mm2. The third shift register is made with ringed-source NMOS transistors and with a DICE architecture. Because of the very low error rate measured even at the highest *LET*, this chain has been made as large as practical, with 1020 stages and an area of 3.9 mm2. During the tests of this chip, slant incidence angle will be used to increase the maximum LET and to fill the gaps in the *LETs* of the ions in the cocktail.

SEE Results

SEU Results

The SEU results obtained from CHIP#1 are presented in Fig. 5. The graph presents the probability of flip-flop upset when an ion of a given *LET* hits the flip-flop area. For the lower ion energies there is a considerable uncertainty in the estimated *LET* threshold (L_{th}) values because of the large gaps in the *LET* of the different ions used in the cocktail and the statistical error due to the small number of registered events (Table 1). Values of L_{th} and saturation level were obtained by fitting results to a cumulative Weibull distribution function [8].

The standard library logic shows a SEU L_{th} of approximately 5.5 MeV/mg/cm^2, reaching a probability saturation level of 1 (every ion hitting a FF will produce an upset). Ringed-source flip-flops have a higher L_{th} of 16 MeV/mg/cm^2, with saturation at $1.7 \cdot 10^{-2}$. For FFs with fully-enclosed layout, L_{th} rises to around 35 MeV/mg/cm^2, although saturation remains practically the same as for ringed-source FFs. The improvement in L_{th} between both types of layout can be explained by the 2.6 times larger width of the transistors in the enclosed layout, which increases the critical charge needed to upset a node. Best results are obtained for FFs using the DICE architecture. In this case L_{th} is close to the maximum *LET* at normal incidence of the ions in the cocktail (67.7 MeV/mg/cm^2). Data were not sufficient to estimate their saturation since it would have required ions with higher *LET* or very long test time. The DICE architecture, built with the ringed-source layout style contributes a 4 times improvement in L_{th} over the ringed-source layout, and nearly 45 times error-probability reduction at 67.7 MeV/mg/cm^2.

Table 1. Results of SEU tests. Errors for each type of shift-register at different LET and fluences.

		Number of recorded errors			
LET [MeV/mg/cm^2]	Fluence [cm^{-2}]	Standard	Ringed	Enclosed	DICE
6,4	$5{,}6 \cdot 10^7$	3	0	0	0
15,9	$2{,}8 \cdot 10^7$	178	1	0	0
40.4	$7.5 \cdot 10^6$	233	127	15	0
67.7	$5.5 \cdot 10^6$	617	179	104	4

Latch-Up Results

Latch-ups were observed only in the logic implemented using the standard-library, and in the latch-up test structure without guard-rings. The cells designed using RHBD style layouts, with added guard-rings substrate contacts, did not suffer any latch-up event in the tests performed. For the standard-library logic, L_{th} is in the order of 9 MeV/mg/cm^2. This value is lower than the 14 MeV/mg/cm^2 reported in [9] for the same technology. Latch-up probability saturation level is at $2 \cdot 10^{-2}$

The latch-up test structures could not be characterized completely, as the off-chip over-current protection was not fast enough and the bonding wire supplying power to the unguarded test structure melted early in the experiment. In the surviving test structure with guard rings, no latch-ups were observed up to a LET of 67.7 MeV/mg/cm^2.

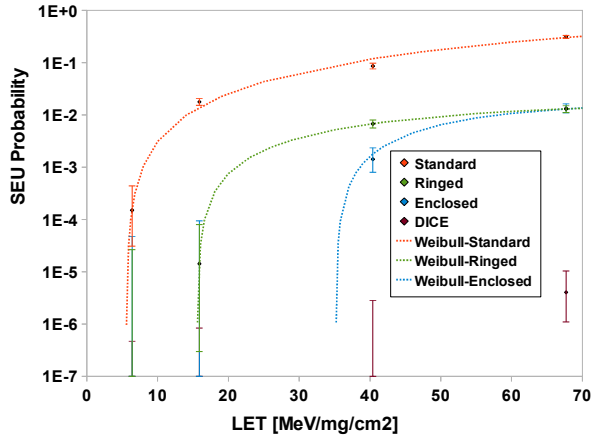

Fig. 5: SEU probabilities

CONCLUSIONS AND FUTURE WORK

Test results show that with standard enclosed-layout procedures for leakage reduction in NMOS transistors, the leakage and voltage drifts caused by radiation up to 300 krad are acceptable with slightly increased design margins for threshold voltage. Threshold drift is more pronounced in transistors with close to minimum dimensions, and in transistors with thick oxide, intended to operate with 5 V supply.

The behavior at low temperatures did not show significant deviations from that predicted by the foundry models.

SEU L_{th} for the standard library cells was in the order of 5.5 MeV/mg/cm^2. For the RHBD cells, with improved substrate and guard connections, L_{th} increased to 16 MeV/mg/cm^2 (ringed-source NMOS) and to 35 MeV/mg/cm^2 (fully-enclosed layout). Latchups with a L_{th} in the order of 9 MeV/mg/cm^2 were observed in the logic implemented with the standard library. No latch-up was detected in the custom-designed rad-hard digital cells up to a *LET* of 67.7 MeV/mg/cm^2. Activities are in progress for the radiation characterization of the rad-hard digital library.

Future work foresees: the SEE test of the digital library; inclusion of additional digital cells and improvement of the layout to get more compact digital designs; in the analog part, the modelling of the dependence of threshold shift with radiation level and transistor geometry; and the continued use of the technology in the design of mixed-signal ASICs for space applications.

ACKNOWLEDGEMENTS

This work has been partially supported by the Spanish Plan Nacional de Investigación of the Ministerio de Ciencia e Innovación (MICINN), under project MEIGA (AYA2009-14212-C05-04 and AYA2008-06420-C04-02).

We want to thank the technical staff of *ams* for their help in the development of the test chips; and the personnel from the Laboratorio de Radiofísica – USC, Centro Nacional de Aceleradores – US, and Centre de Ressources du Cyclotron, Louvain-la-Neuve. Special thanks to INTA for its continued support, including free use of their facilities to perform the low-temperature tests.

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