Radiation Test of TFSMART2 Technology using Extended Common Mode LVDS and DC-DC Converter Components

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Outline

- Introduction
- TFSMART2 Technology Overview
- Tested Components
- Test Method
- Results and Discussions
- Conclusion
- Outlook
Introduction

Motivation
- Extend customer base towards high quality niche markets
- Recognition of European aerospace market demand to overcome ITAR restrictions
- Take advantage of specialty SOI technology - suitable for harsh and radiation environments
- A number of developed commercial components interesting for the aerospace market

Experiment
- Perform low-cost TID experiments up to 100 krad
- Use existing commercial components
Advantages of SOI

- Full dielectric isolation with deep trench
  - Enhanced integration density i.e. smaller chip size (more than 50% is possible)
  - Superior leakage control
  - Inherent prevention of latch-up

- Reduced substrate coupling
  - Enhanced device performance due to reduced parasitic coupling
  - High voltage capability, device stacking and even negative well voltages
  - Straight forward process flow and integration
Radiation Effects on SOI

- SOI devices are known to be immune to SEL, which is a typical latch-up event triggered by prompt ionizing particles (ions, protons) entering into silicon.
- The body tie improves the single event immunity of SOI by providing the possibility to divert generated charges to the device ground.
- Other like SET and SEU can also be mitigated by the use of SOI due to much smaller charge collection volume compared to bulk devices.
- TID effects are mainly relevant to the insulator properties (gate oxide, buried oxide, trench isolations), which may impact various devices.
The TFSMART2 is a 0.35µm BCDMOS technology platform combining bipolar, 3.3V CMOS logic and high voltage DMOS device components on SOI.
## Technology Features

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum feature size</td>
<td>0.35 µm</td>
</tr>
<tr>
<td>Substrate</td>
<td>SOI; p-type handle wafer &lt;100&gt; with 2 µm p-type &lt;100&gt; active layer</td>
</tr>
<tr>
<td>Isolation</td>
<td>shallow trench, deep trench, buried oxide</td>
</tr>
<tr>
<td>Well type</td>
<td>SV-NWell, SV-PWell; LV-NWell, LV-PWell</td>
</tr>
<tr>
<td>Gate oxide</td>
<td>LV gate oxide 7.4 nm, HV gate oxide 17.5 nm</td>
</tr>
<tr>
<td>Source/drain</td>
<td>LDD</td>
</tr>
<tr>
<td>Metallization</td>
<td>3 + 1 (metal 3 optional) level AlSiCu, tungsten contacts and vias, silicided contact areas, stacking of vias and contacts allowed</td>
</tr>
<tr>
<td>Devices</td>
<td>Lateral NPN and PNP transistors</td>
</tr>
<tr>
<td></td>
<td>CMOS (3.3V, 5.0V)</td>
</tr>
<tr>
<td></td>
<td>HVNMOS (25V, 30V, 45V, 65V, 80V, 100V)</td>
</tr>
<tr>
<td></td>
<td>HVPMOS (30V, 45V, 65V, 80V)</td>
</tr>
<tr>
<td></td>
<td>6.2V Zener and 80V freewheeling and zapping diodes</td>
</tr>
<tr>
<td></td>
<td>11 different well, diffusion, low- and high-ohmic poly and metal resistors</td>
</tr>
<tr>
<td></td>
<td>5 different capacitors including GOX, poly and MIM</td>
</tr>
<tr>
<td>Mask levels</td>
<td>24 masks for base process with 3 metal layers</td>
</tr>
</tbody>
</table>
Tested Components

- Extended Common Mode LVDS
  - Driver TF90LVDS031
  - Receiver TF90LVDT032
  - Device utilization:
    - 3.3V high-speed and 5V MOS devices
    - Bipolar devices
    - ESD protection
- DC-DC converter
  - TF6002
    - 3.3V and 5V MOS devices
    - HVMOS devices
    - Bipolar devices
    - ESD protection
Extended Common Mode LVDS

>1V of noise or ground potential difference at Rx causes fault !!!

LVDS spec guarantees operation between ground and 2.4V.

Box to box, command & control

Ideal for box-to-box communication or noisy industrial, aerospace, signage & automotive applications

RS-485 noise immunity but far superior LVDS performance, power and EMI!
TF90LVDS031

- 400Mbps Quad LVDS Line Driver
- 250ps max pulse skew
- 300ps max channel-to-channel skew (any edge)
- 23mA max supply current (loaded)
- -40°C to +85°C extended temperature range
- 16-pin SOICN package
TF90LVDT032

- 400Mbps Quad LVDS Line Receiver
- -7V to +12V extended common mode
- 100Ω on-chip termination resistors
- 300ps max pulse skew
- 400ps max channel-to-channel skew (any edge)
- 7mA max supply current
- -40°C to +85°C extended temperature range
- 16-pin SOICN package
TF6002

- DC-DC converter
- 2A output load current
- 4.5V to 26V input voltage
- 0.923V to 23V output voltage
- 130mΩ MOSFETs
- >90% efficiency
- 2.5% variation of feedback voltage
- 340kHz fixed switching frequency
- 8-pin SOICN package
- -40°C to +85°C extended temperature range
Test Method

- Standard plastic packages
- Without applied bias
- 25 parts of each type
- 5 TID groups
  - 5krad
  - 10krad
  - 20krad
  - 40krad
  - 100krad
- Comparison groups
- Irradiation at ESTEC on 6-Mar-2012
- $^{60}$Co source
  - dose rate: 75 rad/min (distance 70cm)
- Room temperature annealing
- Hot temperature annealing 100°C for 5 h
Results Overview

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dominant Dependency</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOZ</td>
<td>Process variation (MOS)</td>
</tr>
<tr>
<td>VOD</td>
<td>Mismatch</td>
</tr>
<tr>
<td>VOCM</td>
<td>Mismatch</td>
</tr>
<tr>
<td>IOS</td>
<td>Mismatch</td>
</tr>
<tr>
<td>ICCZ</td>
<td>Process variation and mismatch</td>
</tr>
<tr>
<td>ICCL</td>
<td>Process variation and mismatch</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Symbol</td>
<td>Dominant Dependency</td>
</tr>
<tr>
<td>----------</td>
<td>--------------------------------------------------------</td>
</tr>
<tr>
<td>IOS</td>
<td>Process variation (MOS)</td>
</tr>
<tr>
<td>RIN</td>
<td>Process variation ($R_{pol}$)</td>
</tr>
<tr>
<td>IIN</td>
<td>Process variation ($R_{pol}$)</td>
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<td>ISS</td>
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</tr>
<tr>
<td>VFB</td>
<td>Mismatch</td>
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<tr>
<td>FOSC</td>
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<tr>
<td>ISD</td>
<td>Process variation</td>
</tr>
<tr>
<td>IIN</td>
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</tbody>
</table>
Results

Voltage Reference

- Bipolar mismatch
- Resistor mismatch
- Current mirrors

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**TF90LVDS031**

**TF6002**

**Steady-state output common mode**

<table>
<thead>
<tr>
<th>Radiation Level</th>
<th>TF90LVDS031</th>
<th>TF6002</th>
</tr>
</thead>
<tbody>
<tr>
<td>5krad</td>
<td>-0.10%</td>
<td>-0.20%</td>
</tr>
<tr>
<td>10krad</td>
<td>-0.05%</td>
<td>-0.10%</td>
</tr>
<tr>
<td>20krad</td>
<td>0.00%</td>
<td>0.00%</td>
</tr>
<tr>
<td>40krad</td>
<td>0.05%</td>
<td>0.10%</td>
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<tr>
<td>100krad</td>
<td>0.10%</td>
<td>0.20%</td>
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**Feedback threshold**

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**Differential output voltage**

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</table>
Results

Current Reference
- LV MOS mismatch
- 2 different circuit topologies

TF90LVDS031

TF6002
Results

Global Properties

- Rpoly is stable
- RDSon is stable
- Vth and probably other MOS parameters are drifting

TF90LVDT032
Results

Power Consumption

- Depends on different parameters
- Leakage increases

TF6002

TF90LVD1032

- Power Consumption
- Leakage decreases

TF6002

TF90LVD1032

- Power Consumption
- Leakage decreases

TF6002

TF90LVD1032

- Power Consumption
- Leakage decreases
Conclusion

• Minor shifts in key data sheet parameters after TID irradiation up to 100 krad

• None of the key component specifications are violated and remained well beyond the unacceptable limits; all tested parts keep their complete functionality

• TFSMART2 process and the tested circuit concepts have a great potential for the future aerospace applications
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