RADIATION TEST OF TFSMART2 TECHNOLOGY USING EXTENDED COMMON MODE LVDS AND DC-DC CONVERTER COMPONENTS

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ABSTRACT

A preliminary unbiased radiation test has been performed with the TELEFUNKEN Semiconductors LVDS driver TF90LVDS031, the extended common mode LVDS receiver TF90LVDT032 and the DC-DC converter TF6002, which are processed with the TFSMART2 BCD SOI technology. Suitability of the TFSMART2 technology platform for radiation hard environment is evaluated at the product level. Existing capabilities of the technology platform are introduced and advantages of SOI technologies are discussed in the light of the collected measurement results.

INTRODUCTION

Radiation hardness is one of the most stringent requirements applied to IC components for aerospace use, which is normally not subject to standard IC qualification for industrial or consumer applications. Thus, the suitability of the IC-manufacturing technology is of the utmost importance for the dedicated circuit design aiming aerospace applications, or for spin-in of existing non-aerospace IC components. Due to highly demanding specifications, expensive and tedious qualifications, the number of space-qualified technologies for aerospace applications, which can alternatively be used for development of European aerospace IC components, is very limited.

Unrestrictedly available in Europe, the TFSMART2 IC-manufacturing technology offered by TELEFUNKEN Semiconductors is a good candidate for aerospace applications, thanks to Silicon-On-Insulator (SOI) technology, which is inherently resistant to parasitic effects such as latch-up and substrate leakage. Extended temperature range, high performance and broad voltage spectrum offer a high potential not only for consumer applications but also for aerospace applications. Maturity of the technology has been justified by previous commercial use, number of power management / LVDS components and existing qualification results.

This work aims to test radiation hardness of the TFSMART2 technology at the product level by performing low-cost Total Ionizing Dose (TID) experiments up to 100krad. The findings of this investigation provide us implications for the radiation tolerance of the circuit design concept of the selected products as well.

TFSMART2 Technology Platform: 0.35µm BCDMOS on SOI

As the name implies, BCD technologies stem from analog and bipolar world where higher voltage capability is supplemented to standard CMOS nodes. Therefore, BCD technologies offer an attractive platform for wide variety of analog/mixed-signal and power management applications from consumer appliances to automotive/industrial.

The TFSMART2 is a 0.35µm BCDMOS technology platform combining bipolar, 3.3V CMOS logic and high voltage (HV) DMOS device components on SOI. The platform features a broad range of HV device portfolio from low on-resistance 25V devices to HV options of 100 to 120V. The HV capability, which is being extended to 200V, offers a full-deep-trench isolation and high integration density. As shown in Table 1, high-performance low voltage (LV) 350nm CMOS devices, low on-resistance power devices and wide variety of active/passive device elements together with 4 metal layers designate the technology.

Table 1 Key technology features of TFSMART2

Characteristic	Details
minimum feature size	0.35µm
substrate	SOI; p-type handle wafer with 2µm p-type active layer; 6 inch
isolation	shallow trench, deep trench, 0.5µm buried oxide
well type	Super voltage (SV)-NWell, SV-PWell; LV-NWell, LV-PWell
gate oxide	thickness LV gate oxide 7.4nm, thickness HV gate oxide 17.5nm
source/drain	Lightly doped drain (LDD)
metallization	3 + 1 (metal 3 optional) level AlSiCu, tungsten contacts and vias, silicided contact areas, stacking of vias and contacts allowed, optional back-side-contact
devices	Lateral NPN and PNP transistors CMOS (3.3V, 5.0V) HVNMOS (25V, 30V, 45V, 65V, 80V, 100V) HVPMOS (30V, 45V, 65V, 80V) 6.2V Zener and 80V freewheeling and zapping diodes 11 different well, diffusion, low- and high-ohmic poly and metal resistors 5 different capacitors including gate oxide (GOX), poly and metal-isolation-metal (MIM)
mask levels	24 masks for base process, 26 mask steps with optional metal 3 layer

In SOI technology, active and passive devices are formed in a thin silicon layer, which is isolated from the main body of the substrate by an insulating layer, mostly silicon dioxide called buried oxide (BOX). With appropriate manufacturing techniques, devices can be fully isolated from the rest of the silicon resulting in significant reduction and/or prevention of leakage currents, substrate coupling and latch-up, which would otherwise degrade the expected circuit performance. SOI offers a significant benefit in terms of structure density that can be integrated on a single die. This is particularly true for HV devices since bulk silicon technologies utilize standard junction isolations, which requires large areas on the chip area. Typically, isolation of 100V requires lateral junctions that are larger than 10µm, which is easily managed by 0.77µm trenches filled by silicon dioxide in TFSMART2. (See [1] for more details.)

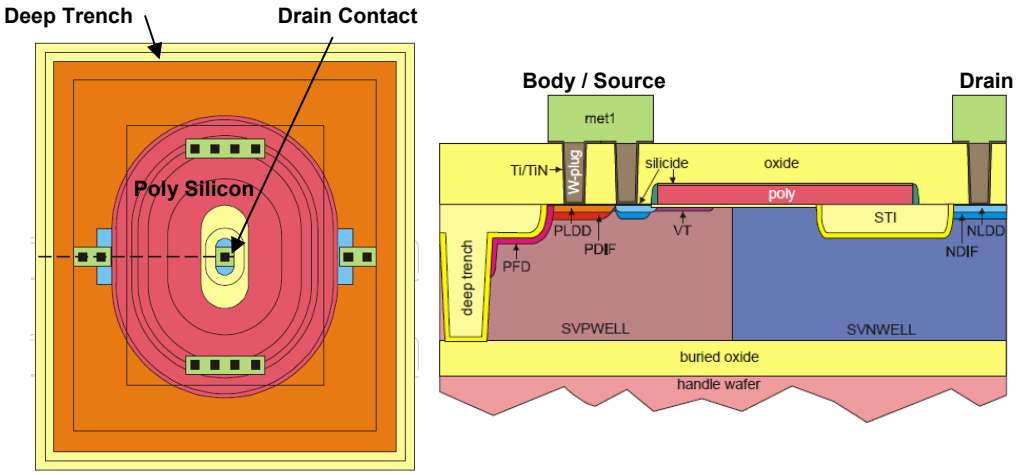

Fig. 1 Typical top-view (left) and the cross-section (right) of a DMOS device of TFSMART2 technology which is scalable in the width direction. Dashed line shown on the left depicts the device cross-section on the right sketch.

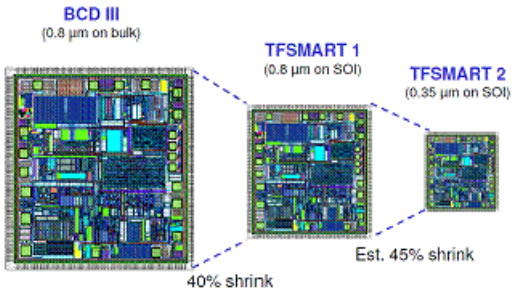

Fig. 2 Estimated shrink that can be achieved with 0.35µm SOI technology

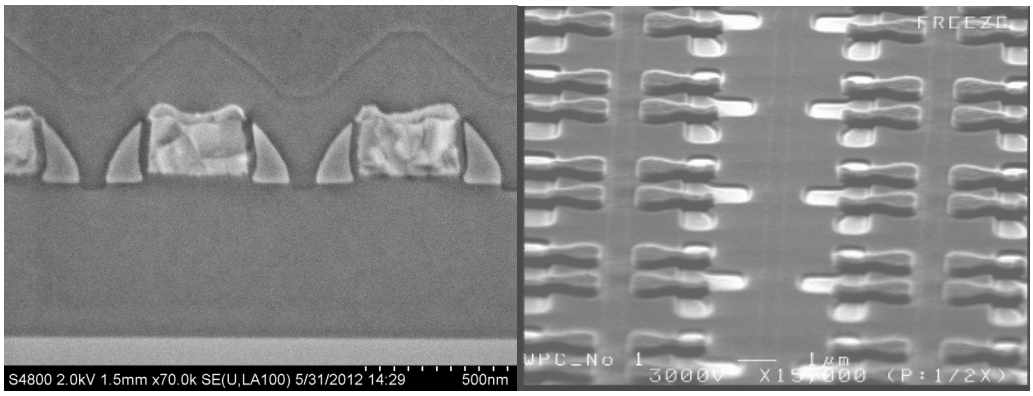

Fig. 3 Low voltage (3.3V) gate array and the cross-sections 350nm poly-gates of TFSMART2

Another known inherent advantage of SOI is that the device performance can be enhanced due to the BOX layer, which reduces the parasitic junction capacitances as the junctions are fully isolated with a dielectric.

Aforementioned inherent advantages of SOI technology are even more pronounced when the application field is expanded to harsh environments like aerospace ICs. Exposure of ICs to various radiation sources may lead to fatal errors in circuits like TID and Single Event (SE) effects, which originate from interactions between the high energy particles and the silicon at the single device level. For instance, SOI devices are known to be immune to SE Latch-Up (SEL), which is a typical latch-up event triggered by prompt ionizing particles (ions, protons) entering into silicon. Other SEs like SET (Single Event Transient) and SEU (Single Event Upset) can also be mitigated by the use of SOI due to much smaller charge collection volume compared to bulk devices. TID effects are however mainly relevant to the insulator properties (gate oxide, BOX, trench isolations), which may impact various devices in different way. Upon incident radiation, generated electron hole pairs in silicon can be captured in insulating oxide (GOX, STI or BOX) or their interfaces to silicon, which in turn may modify the device characteristics and their reliability behavior.

We believe that the TFSMART2 technology possesses default advantages for aerospace applications, although no dedicated mitigation techniques are employed for the sake of radiation hardness. In this work, we have evaluated the TID behavior of TFSMART2 at the product level in order to gain insight into radiation hardness of the technology.

MOS devices in TFSMART2 are neither fully depleted nor partially depleted since a body tie is placed by default which can be placed either as source-body shorted or separated. Integration of body contacts avoids the circuit design complexity caused by the floating body and history effects of partially depleted SOI devices. The body tie is also known to improve the SE immunity of SOI by providing the possibility to divert charges to the ground.

As pointed above, TID effects are expected to modify mostly the gate oxide characteristics, which may directly impact the threshold voltage of MOS devices. It is also likely that electrical characteristics of n-channel devices are modified due to hole trapping at the STI/p+ interfaces leading to parasitic corner devices. Such traps at the isolation corners might also increase the base leakage in bipolar devices and lead to loss in gain. On the other hand, it has been shown in [2] that TID effects on gate oxide scale with the gate oxide due to reduced charge trapping and interface states. Since TFSMART2 employs gate oxide thinner than 20nm, no serious threshold voltage shifts in MOS devices are expected.

Depending on the design, another benefit of the TFSMART2 technology could intuitively be the smaller features and geometries, which enable one to layout smaller susceptible volumes reducing the probability to be struck by a particle.

Tested Components

Three component types relevant for space applications have been selected for the preliminary radiation test - an extended common mode LVDS receiver and complementary driver, for which the necessity in aerospace is addressed in [3], and a step-down DC-DC converter, which is strongly demanded by space equipment manufacturers. These components are utilizing the most important silicon devices of the TFSMART2 technology. The LVDS driver and receiver are LV designs containing 3.3V LV high-speed and 5V middle-voltage (MV) MOS devices, bipolar devices and ESD protection circuits for LV and extended common mode range. The DC-DC converter is a HV design containing, bipolar devices LV, MV and HV MOS devices and ESD protection circuits.

For proper interpretation of test results it is important to clarify IC datasheet parameter dependencies. There are two types of persistent effects caused by ionizing radiation, which influence IC datasheet parameters:

1) *global changes* in the value of silicon device parameters, which are simultaneous for all silicon devices of the whole component; they influence process variation related datasheet parameters.
2) *local changes* in the value of silicon device parameters, which are stochastic and apply to differences between single silicon devices; they influence mismatch related datasheet parameters.

In the following sections, descriptions of these components and the lists of examined datasheet parameters are given. In the given datasheet parameter lists, assignments are made if the parameters mainly depend on process variation, mismatch or both process variation and mismatch.

LVDS Driver TF90LVDS031

The TF90LVDS031 is a 400Mbps Quad LVDS Line Driver optimized for high-speed, low power, low noise transmission over controlled impedance (approximately 100Ω) transmission media (e. g. cables, printed circuit board traces, backplanes). The TF90LVDS031 accepts four LVCMOS signals and translates them to four LVDS signals. Its differential outputs can be disabled and put in a high-impedance state via two enable pins. Low 300ps (max) channel-to-channel skew and 250ps (max) pulse skew ensure reliable communication in high-speed links that are highly sensitive to timing error. Supply current is 23mA (max). LVDS outputs conform to the ANSI/EIA/TIA-644-A standard. The TF90LVDS031 is offered in 16-pin SOIC package and operates over an extended -40°C to +85°C temperature range. Table 2 shows the list of the examined datasheet parameters. For more details and specification see [4].

Extended Common Mode LVDS Receiver TF90LVDT032

The TF90LVDT032 is a 400Mbps Quad LVDS Line Receiver optimized for high-speed, low power, low noise transmission over controlled impedance (approximately 100Ω) transmission media (e. g. cables, printed circuit board traces, backplanes). The TF90LVDT032 accepts four LVDS signals and translates them to four LVCMOS signals. Its outputs can be disabled and put in a high-impedance state via two enable pins. The TF90LVDT032 input receiver supports wide input voltage range of -7V to +12V for exceptional noise immunity. The TF90LVDT032 features on-chip 100Ω input termination resistors that minimize input return loss, component count and board space. Supply current is 7mA (max). LVDS inputs conform to the ANSI/EIA/TIA-644-A standard. The TF90LVDT032 is offered in 16-pin SOIC package and operates over an extended -40°C to +85°C temperature range. Table 3 shows the list of the examined datasheet parameters. For more details and specification see [5].

Table 2 TF90LVDS031 examined datasheet parameters

Symbol	**Parameter**	**Dominant Dependency**
IOZ	LVDS high-impedance output current	Process variation (MOS)
VOD	Differential output voltage	Mismatch
VOCM	Steady-state output common mode voltage	Mismatch
IOS	Output short circuit current	Mismatch
ICCZ	Power supply current with disabled outputs	Process variation and mismatch
ICCL	Power supply current with output loads	Process variation and mismatch

Table 3 TF90LVDT032 examined datasheet parameters

Symbol	Parameter	Dominant Dependency
IOS	Output short circuit current	Process variation (MOS)
RIN	LVDS input termination resistor	Process variation (R_{poly})
IIN	LVDS input current at -7V	Process variation (R_{poly})
IIN	LVDS input current at +12V	Process variation (R_{poly})
ICCZ	Power supply current with disabled outputs	Process variation and mismatch
ICC	Power supply current (not switching)	Process variation and mismatch

Table 4 TF6002 examined datasheet parameters

Symbol	Parameter	Dominant Dependency
ISS	Soft-start current	Mismatch
VFB	Feedback voltage threshold	Mismatch
FOSC	Oscillation frequency	Process variation and mismatch
ISD	Shutdown supply current	Process variation
IIN	Supply current	Process variation and mismatch

Step-Down Converter TF6002

The TF6002 is a monolithic synchronous buck regulator featuring integrated 130mΩ MOSFETs that provide continuous 2A output load current. It operates over a wide 4.5V to 26V input voltage range and provides output voltage from 0.923V to 23V at up to 93% efficiency. Its current mode control circuitry provides fast transient response and cycle-by-cycle current limit. The TF6002 has the feedback voltage threshold variation of only 2.5% providing tight output regulation. The TF6002 operates at fixed 340kHz switching frequency. It features programmable soft-start which prevents inrush current at turn-on. In the shut-down mode it draws only 3μA (max). The TF6002 is offered in 8-pin SOIC narrow package. It operates over an extended -40°C to +85°C temperature range. Table 4 shows the list of the examined datasheet parameters. For more details and specification see [6].

TEST METHOD

Since this preliminary radiation test was supposed to be low-cost, the IC components have been tested in standard plastic packages without applied bias. There was a shipping period of 2 days between irradiation and post-radiation measurements.

Test Specimens

From all three IC types 60 respectively 45 and 48 pieces each were included in this test campaign:

- 25 ICs TF6002, 25 ICs TF90LVDT032 and 25 ICs TF90LVDS031 (test group) were actually irradiated with increasing dose during the test.
- 35 ICs TF6002, 23 ICs TF90LVDT032 and 20 ICs TF90LVDS031 (comparison group) travelled with the other components, but were not irradiated and served as reference samples.

Test Preparation

- All ICs of the test group and the comparison group were individually numbered.
- All ICs underwent an automated test of all their parameters, which is traceable to the individual specimens.
- All ICs for irradiation were mounted on 5 coupons of size 30mm×50mm each, made from conductive foam, so that all IC contacts were grounded. Each conductive foam coupon therefore contained:
    - 5 ICs TF6002
    - 5 ICs TF90LVDT032
    - 5 ICs TF90LVDS031
- The irradiated test coupons were clearly numbered 1…5.

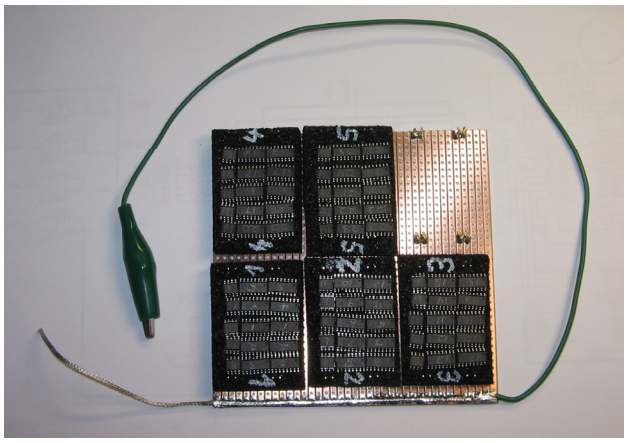

Fig. 4 Test specimens mounted on the plate

- The test coupons were mounted together on a common conductive base plate of size 100mm×100mm, so that they could be easily removed from the base plate.
- The base plate had a ground wire for discharging.

The complete test build is shown on Fig. 4.

Test Procedure

- The base plate with its 5 test coupons was mounted in front of the ^{60}Co source.
    - Distance: 70cm
    - Dose rate: 75rad/min
- A ground connection to the base plate was made for discharging.
- Irradiation sequence:
    - Irradiated all coupons to 5krad total dose, removed coupon no. 1.
    - Irradiated remaining coupons to 10krad total dose, removed coupon no. 2.
    - Irradiated remaining coupons to 20krad total dose, removed coupon no. 3.
    - Irradiated remaining coupons to 40krad total dose, removed coupon no. 4.
    - Irradiated remaining coupons to 100krad total dose, removed coupon no. 5.
- Returned all goods to test site in the original packing for evaluation (2 days shipping period).

Post-Radiation Activities

- All ICs again underwent an automated test of all their parameters, which was traceable to the individual specimens.
- After 7 days of shelf period at room temperature, all ICs underwent an automated test once again.
- All ICs were annealed at the temperature of 100°C for 5 hours.
- All ICs once again underwent an automated test.
- Parameter drifts and their dependency on total dose were calculated and documented.

RESULTS AND DISCUSSIONS

The test results of all three components are shown in Fig. 5. The drifts of all examined datasheet parameters are shown relative to their pre-radiation values. The data points “5krad” to “100krad” are calculated from the mean values of the five different groups of ICs irradiated to the corresponding total dose. The data points “after room temperature anneal” and “after hot temperature anneal” belong to the group of ICs irradiated to 100krad total dose.

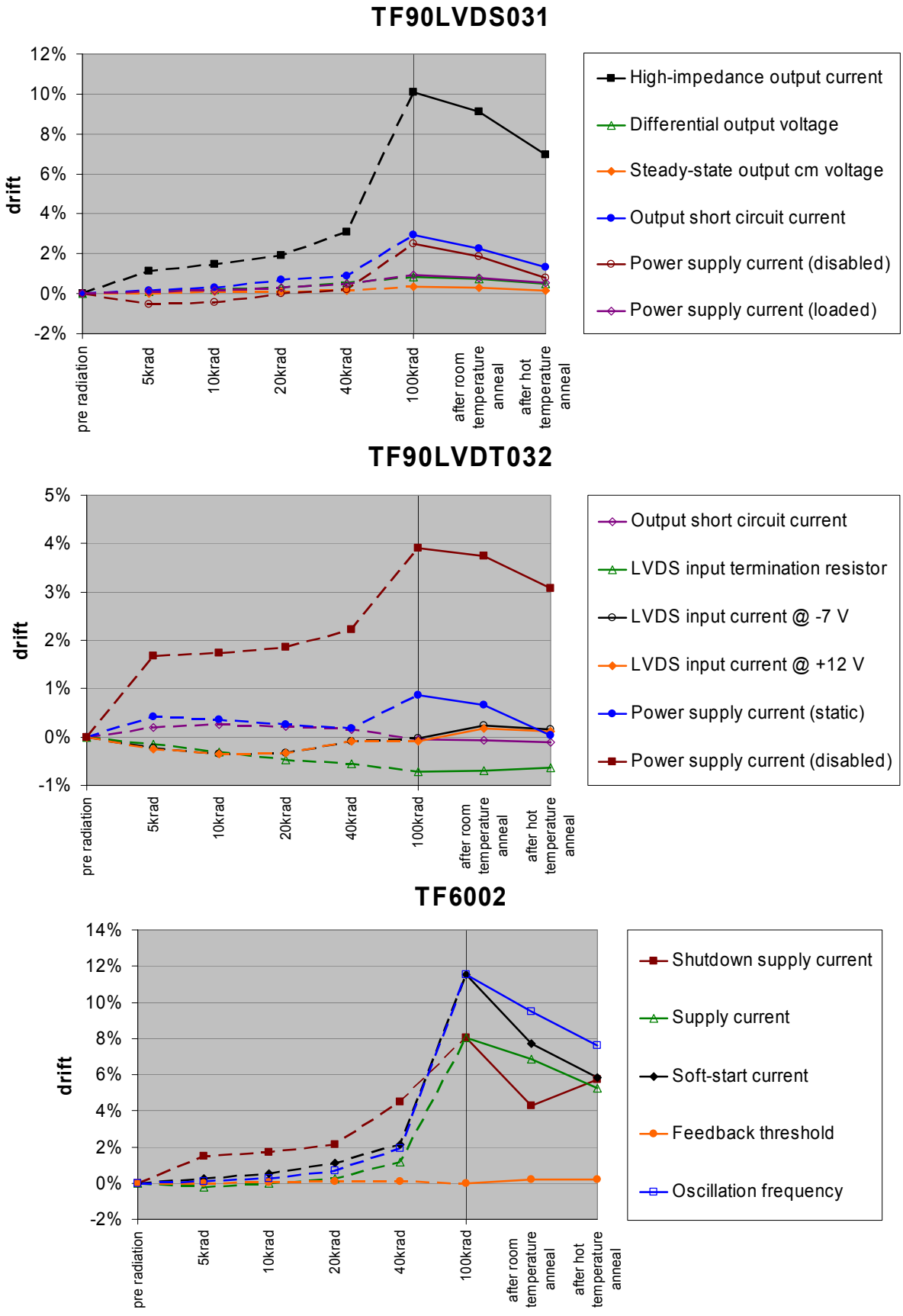

Fig. 5 Test results of TF90LVDS031, TF90LVDT032 and TF6002

The shown test results are looking feasible, since the observable drift tendency is constant through the total dose steps. The data points near 0% might be more influenced by measurement tolerances. The highest parameter drifts count to 12% whereas majority of the parameters don't show measureable drifts.

The mismatch related parameters showing low drifts are "Feedback threshold" (TF6002), "Differential output voltage" and "Steady-state output common mode voltage" (both TF90LVDS031). They indicate that the voltage reference circuits were not impacted by the radiation. Therefore it can be concluded that no matching concerns arise in bipolar, MOS devices and polysilicon resistors. Since two different voltage reference circuits are used, high robustness of such circuits manufactured in TFSMART2 technology against TID effects can be conceivably assumed. The process related parameters showing low drifts depend on polysilicon resistance and drain-source on-resistance of MOS-devices.

The parameter "High-impedance output current" (TF90LVDS031) depends on various LV MOS parameters like threshold voltages and shows 10% drift at 100krad total dose which might indicate some degree of degradation in GOX properties.

The parameter "Soft-start current" (TF6002) originates from the current reference circuit, which has also linear influence on "Oscillation frequency" (TF6002). This explains equivalent 12% drifts of these parameters at 100krad total dose. An interesting detail is that the "Output short circuit current" of TF90LVDS031 stems also from the current reference circuit and shows only 3% drift due to different circuit topology. This fact is a subject to future investigations in circuit design for radiation tolerance.

Finally, all measured shifts in presented parameters are not critical and all tested parts keep their complete functionality after the given TID radiation doses.

CONCLUSION

The TID radiation applied to three different TELEFUNKEN IC products manufactured in the TFSMART2 SOI technology shows minor shifts in key data sheet parameters. None of the key component specifications are violated and remained well beyond the unacceptable limits, after the TID exposure of up to 100kRad. Presented preliminary radiation hardness results suggest that the TFSMART2 process and the circuit concept have a great potential for the future aerospace applications.

The future work will be dedicated to full technology qualification in harsh environments not only at the circuit/ component level but also at the single device level, which can shed more light on the potential physical degradation mechanisms.

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REFERENCES

[1] TELEFUNKEN Semiconductors, "TFSMART2" Process technology description, http://www.telefunkensemi.com/index.php/specialty-foundry/process-technologies/hv-family/tfsmart2
[2] A. Samaras, "JUPITER Mission and Strong Environment" Radiation Specification for System conception, JUICE Mission, CNES, July 2012
[3] J. Ilstad, "ESA's Requirements for future LVDS devices", LVDS Application Workshop, Noordwijk, June 2011
[4] TELEFUNKEN Semiconductors, "TF90LVDS031 Quad LVDS Line Driver" Datasheet, October 2011, http://telefunkensemiconductor.com/dwh/ds/if/ecmlvds/tf90lvds031.pdf
[5] TELEFUNKEN Semiconductors, "TF90LVDS032 / TF90LVDT032 Quad LVDS Line Receivers with Extended Common Mode" Datasheet, April 2012, http://www.telefunkensemiconductor.com/dwh/ds/if/ecmlvds/tf90lvds032.pdf
[6] TELEFUNKEN Semiconductors, "TF6002 / TF6002A 2A, 26V Synchronous Rectified Step-Down Converter" Datasheet, December 2011, http://telefunkensemiconductor.com/dwh/ds/pwr/tf6002.pdf
[7] H. Henkel , W. Rabe, A. Rocke, V. Burkhay, "Total-Dose Test of Step-Down Converter and LVDS Driver and Receiver ICs from Telefunken Semiconductors", ESA unclassified for internal use only, April 2012