ADVANCES IN RADIATION HARDENED MIXED-SIGNAL TECHNOLOGY

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INTRODUCTION

Mixed-signal integrated circuits are used in a variety of applications where ionizing radiation is present, including satellites, space vehicles, nuclear reactor monitoring, medical imaging, and cancer therapy. While total ionizing radiation is present in each of these environments, the type of radiation (e.g. heavy ions vs. high-energy x-rays) and other environmental factors present unique challenges to the mixed-signal designer. This paper discusses three radiation hardened, mixed-signal integrated circuits (ICs) designed in three different wafer foundry technologies. A block diagram and summary of operation of each of the devices is presented, along with the key features of the technology used in the design. We discuss some of the design challenges due to the environments, the design tools, processes, and laboratory tests used to mitigate and characterize environmental effects. We conclude each case study with the results of radiation testing of each design.

CASE STUDY 1: UT08SC14ADV045 Smart Sensor Integrated Circuit

Fig. 1 shows a block diagram of a mixed-signal System-on-a-Chip (SoC) ASIC designed originally for nuclear power monitoring. The UT08SC14ADV045 Smart Sensor Integrated Circuit forms the basis for an instrumentation system, providing the interface between various sensors and a digital controller. This IC includes circuitry to excite and precisely measure the response from 11 sensor types. It is radiation-hardened to low dose rate and high dose rate gamma irradiation and neutron irradiation, and is suitable for operation in harsh environments up to 200°C. The excitation generator includes a 14-bit DAC with a high current, high-voltage differential output. Eight high-voltage differential signal inputs are provided, with configurable signal conditioning. The signal conditioner output is converted to digital form by a 14-bit delta-sigma analog-to-digital converter (ADC), and the digital data word is made available on a Low-Voltage Differential Signaling, Serial Peripheral Interface (LVDS SPI) port. Another LVDS SPI port is available for configuration, control, parameter trim, and access to internal registers within the Smart Sensor. A clock generator block generates the necessary internal clocks from a low-frequency reference. Internal regulators derive necessary supply voltages and references from +/-6V and +3.3V power supply inputs. A fuse-based One-Time Electrically Programmable Read-Only Memory (OTEP ROM) is also included, providing non-volatile storage for reference trim data, as well as default configuration and user configurable program storage. The UT08SC14ADV045 is useful for wide variety of sensor types with and without excitation, such as resistance thermometer, thermocouple, LVDT, strain gauge/load cell, inductive and transformer-based position, absolute and relative pressure, Hall Effect probe, photodiode, accelerometer, tachometer, and other types of sensors.

Table I lists the key environmental requirements for the Smart Sensor IC. The environment requires operation in a total ionizing dose (TID) of 100krad(Si), with temperatures up to 200°C, at a low gamma dose rate of 2.8 mrad(Si)/sec. The IC must also be immune to neutron-induced latch-up (NIL), and have a neutron-induced upset (NIU) rate of < 1E-11 errors/bit/day. Key performance specifications are provided in Table II.

Table III shows key technology features of the 0.35 μm Bipolar-CMOS-DMOS (BCD) process used. The process technology has a rich feature set for analog/mixed-signal design including vertical PNP bipolar devices, two types of linear capacitors, high and low value resistors, and extended drain 12V devices.

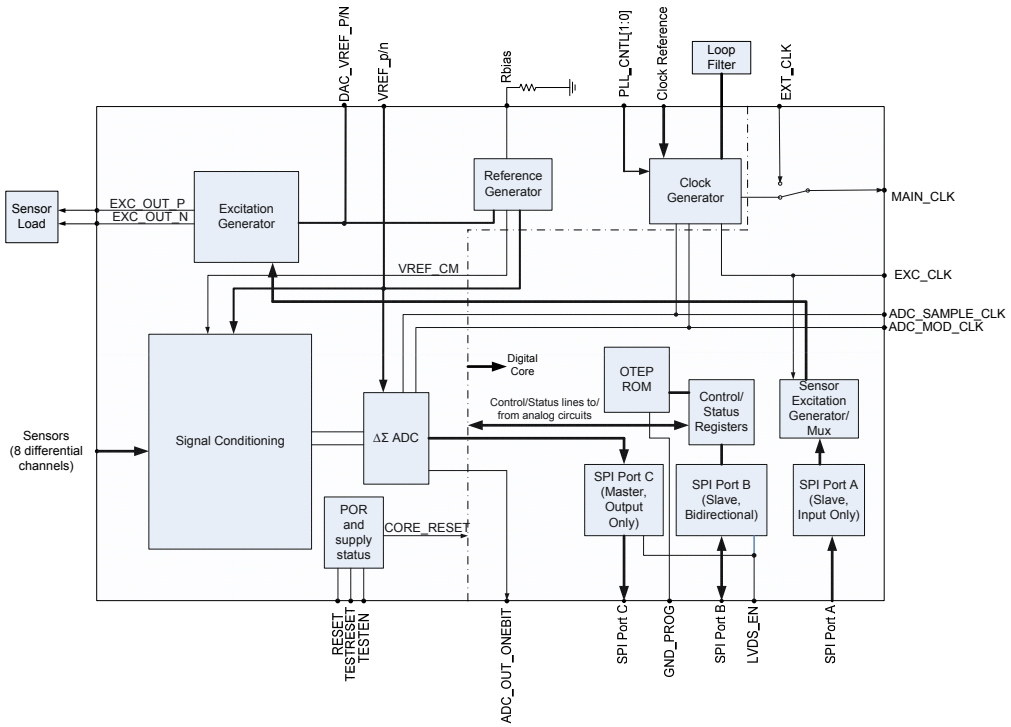

Figure 1: Block Diagram of UT08SC14ADV045 Smart Sensor Integrated Circuit

Table I: Operating Environment for the UT08SC14ADV045

Environment	Requirement
Gamma Ray Total Ionizing Dose (TID)	100krad(Si) at a dose rate of 2.8mrad(Si)/sec
Neutron Induced Upset (NIU)	< 1E-11 errors/bit/day
Neutron Induced Latch-Up (NIL)	Immune (5E11 neutrons/cm^2, peak energy < 2MeV)
Temperature	200°C max. operating

Table II: Key Performance Specifications for the UT08SC14ADV045

Excitation Output	14-bit DAC with differential voltage-mode output up to 20Vp-p, up to 140mA. Sine/square/triangle or arbitrary function outputs.
Sensor Inputs	8 multiplexed differential high-impedance user inputs; input range -5V<Vin<+5V
Signal Channel	Programmable gain range 0.18 to 100, 15 kHz bandwidth, includes alias filter
A/D Converter	14-bit, 3rd-order delta-sigma
Typical channel mismatch	0.04% to 100°C, 0.07% to 200°C
Typical absolute measurement error	1% to 100°C, 4% to 200°C

Table III: Key Fabrication Technology Features

Technology Type	0.35µm BCD (Bipolar-CMOS-DMOS)
Minimum Feature Size	0.35 µm
Well Structure	Triple-Well (Substrate Isolated)
Transistors Used	3V Enhancement Mode NMOS & PMOS (self-aligned) 8V Enhancement Mode NMOS & PMOS (self-aligned) 12V Enhancement Mode Drain-Extended NMOS & PMOS 20V PNP BJT (vertical)
Metallization and Interconnects	4LM, Tungsten Plugs, CMP Planarization
Resistors	Diffusion Resistors, Poly Resistors (non-salicided), Hi-Poly Resistors
Capacitors	PiP, MiM, MOS-caps
Aeroflex Enhancements	RH OTEP Metal Fuse

Design Challenges & Mitigation: Post-Radiation Compact Transistor Models

Incorporation of a robust device modeling process in a mixed-signal design flow is paramount for producing ICs that operate successfully in radiation and other high reliability environments. This section presents one such example: accommodating the effects of ionizing gamma radiation in the BSIM3v3 compact model. The 8V and 12V devices in the above process (Table III) have thicker gate oxides with a higher cross section for interaction in ionizing radiation. For successful design, the effects of ionizing radiation on the thicker gate oxide devices must be accurately modeled. Figure 2(a) shows transistor I_d-V_d and linear region I_d-V_g data for an 8V Commercial RadHard (CRH™) NMOS enhancement mode transistor, compared to simulations using the foundry's BSIM3v3 SPICE model. The symbols in the graphs are actual transistor data while the solid lines of the corresponding color are simulations. As can be seen, there is poor correlation between measured and simulated data for both I_d-V_d and I_d-V_g curves using the BSIM model received from the foundry. Figure 2(b) shows the same transistor data compared to Aeroflex's optimized 100krad(Si) compact transistor models. The improved correlation in the I-V curves provides accurate mixed-signal designs by mitigating the effects of total ionizing dose (TID) in critical device-based design parameters such as subthreshold current, transconductance and threshold voltage.

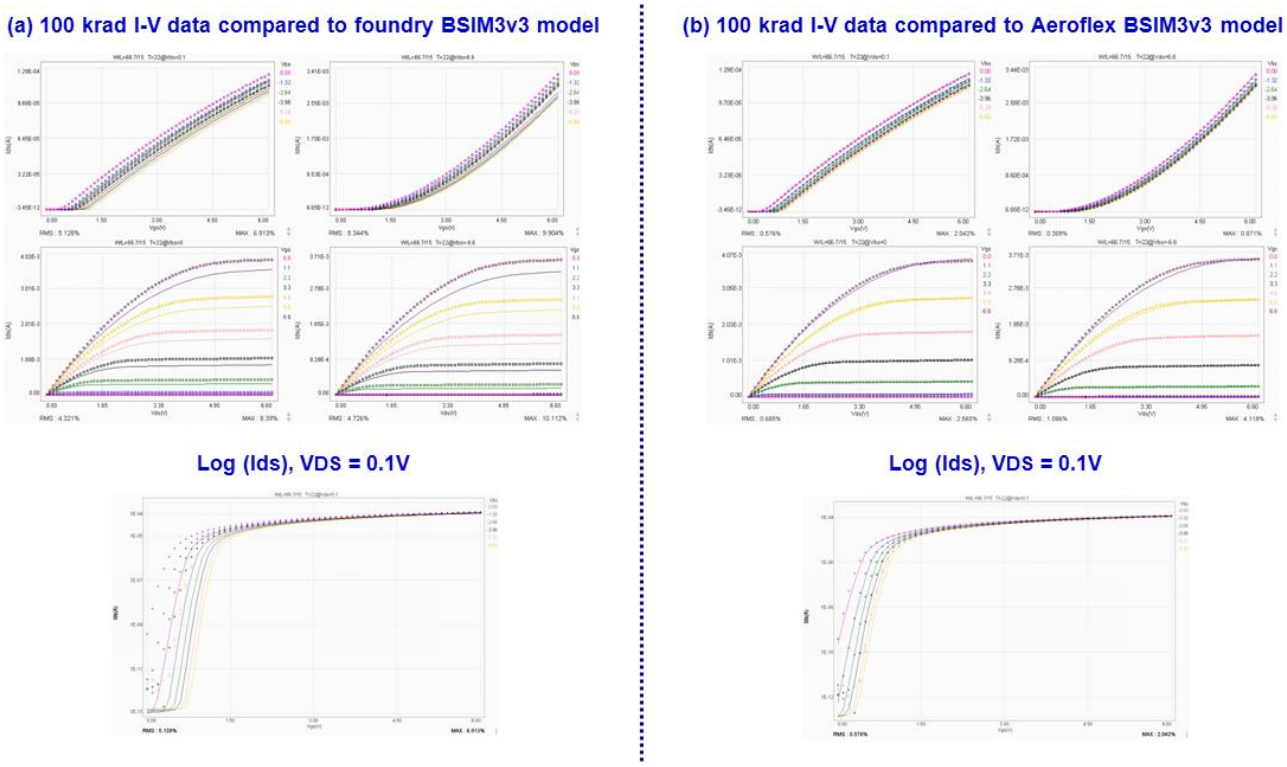

Figure 2: 8V Commercial RadHard (CRH™) NMOS Transistor (a) 100krad(Si) Data vs. foundry Pre-Rad BSIM 3v3 SPICE Model; (b) 100krad(Si) Data vs. Aeroflex 100krad(Si) BSIM 3v3 SPICE Model.

Table IV presents the results of radiation testing the UT08SC14ADV045 in gamma and neutron environments. Radiation environmental specifications were derived primarily from nuclear reactor applications. The Smart Sensor Integrated Circuit passed both low and high dose rate gamma radiation specifications, based upon U.S. MIL-STD 883, Test Method 1019.8. No neutron related effects related to bit upset or latchup were observed during testing to a neutron fluence of 6.8E11 n/cm^2 in accordance with U.S. MIL-STD-883, Test Method 1017.2.

Table IV: Key RadiationTest Results for the UT08SC14ADV045 Smart Sensor Integrated Circuit

Test	Results
Total Ionizing Dose (TID)	PASSED 100krad(Si) at 200rad/sec
Low-Dose Rate TID	PASSED 100krad(Si) at 10mrad(Si)/sec
NIU	NO UPSETS after 6.8E11 n/cm^2
NIL	NO LATCH-UP after 6.8E11 n/cm^2

CASE STUDY 2: UT16AD40P Analog-to-Digital Converter

Figure 3 shows a block diagram of the UT16AD40P analog-to-digital converter (ADC). The UT16AD40P is a 16-bit, 40-MSps CMOS pipeline ADC designed in a 0.18 µm mixed-signal CMOS process using Aeroflex's Commercial RadHard technology for harsh operational environments. Its excellent noise (76dBFS SNR) and distortion performance (95dBc SFDR) make this ADC ideal for those telecommunication and imaging applications posing the most severe electrical and environmental requirements. The full-scale range of the differential analog input is set to 2.5Vp-p by an internal voltage reference circuit. The input Sample-and-Hold Amplifier (SHA) samples the analog input at up to 40MSps. The optional duty-cycle stabilization internally produces 50% clock phases even when the externally provided clock features up to 20% - 80% duty cycle skew. An internal dither function for improved linearity of the conversion of small signal analog inputs can also be optionally selected. Typical linearity specifications of the ADC are ±2.5LSB INL and ±0.25LSB DNL. The digital outputs can be either in LVDS or CMOS format, in Single or Double Data Rate (SDR/DDR). In LVDS mode, an optional internal 100 Ω termination can also be selected. The UT16AD40P provides two output data formats: straight binary and 2's complement. The Output Enable control can be used to put all digital outputs in high impedance state, while leaving the internal analog circuitry fully active. The over-range flag OR is set high whenever the analog input exceeds the full-scale range. If the analog input is below its minimum, i.e. AINP-AINN < -1.25V, OR goes to logic 1 and data D[15:0] is set to its minimum value (0000x for the offset binary output format, and 8000x for 2's complement). An analog input larger than the maximum AINP-AINN > +1.25V will set the OR flag to 1 and D[15:0]=FFFFx (offset binary) or D[15:0]=7FFFx (2's complement). The SPI ports (Serial Peripheral Interface) provide a serial alternative to all the parallel control inputs, and allow the user to activate additional internal functions such as output Randomizer and output Test Patterns. Power Down turns off all internal analog circuits and places all digital outputs in a high-impedance state, thereby reducing the power consumption to 5mW. The Sleep mode allows for quicker recovery time (<250µs @ 0.1% full-scale precision) and consumes only 92mW. The RESET input allows the instantaneous refresh of the digital logic status without a lengthy interruption of the ADC operation. The UT16AD40P can run on dual 3.3/1.8V analog supplies, or on a single 3.3V supply with internal sub-regulation.

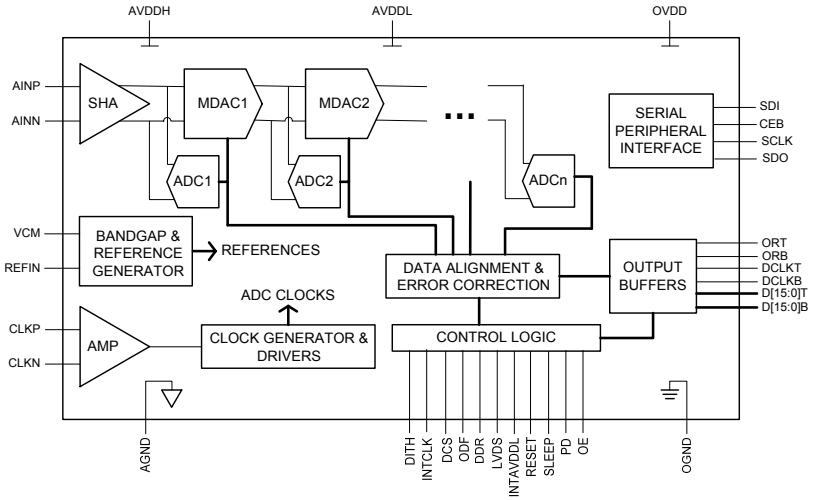

Figure 3: Block Diagram of UT08SC14ADV045

Table V: Operating Environment for UT16AD40P

Environment	Requirement
Total Ionizing Dose (TID)	300krad(Si)
Single Event Upset (SEU)	< 1E-10 errors/bit/day
Single Event Latch-Up (SEL)	122 MeV-cm^2/mg
Single Event Transients (SET)	Onset LET for "long duration" (two or more sample clocks) > 40 MeVcm^2/mg

Table V lists the key environmental requirements for the UT16AD40P. The environment requires operation in a total ionizing dose (TID) environment of 300krad(Si). The IC must be SEL immune at linear energy transfer (LET)

values up to 122 MeV cm^2/mg, and must have a low SEU error rate of < 1E-10 errors/bit-day. A more challenging requirement is to have no SET's with durations longer than 1 sample clock cycle for LETs below 40 MeV-cm^2/mg

Table VI shows the key features of the 0.18 µm mixed-signal CMOS process used. The process technology has competitive design rules and 6 metal layers, allowing for complex digital functionality, but also supports a variety of active and passive devices for analog design, including MiM capacitors and native (near zero threshold) devices.

Table VI: Key Technology Features for UT16AD40P

Technology Type	0.18µm Mixed-Signal CMOS
Minimum Feature Size	0.18 µm
Well Structure	Triple-Well (Substrate Isolated)
Transistors Used	1.8V Enhancement Mode Isolated NMOS & PMOS (self-aligned) 1.8V Enhancement Mode non-isolated NMOS (self-aligned) 3.3V Enhancement Mode Isolated NMOS & PMOS (self-aligned) 3.3V Enhancement Mode non-Isolated NMOS (self-aligned) Native non-isolated NMOS Bipolar NPN (vertical)
Metallization and Interconnects	6LM, Tungsten Plugs, CMP Planarization
Resistors	Diffusion Resistors, Poly Resistors (non-salicided), Hi-Poly Resistors
Capacitors	MiM, MOS-caps
Aeroflex Enhancements	P-type varactors, Low Dielectric Absorption MiM Capacitors, RH OTEP Metal Fuse

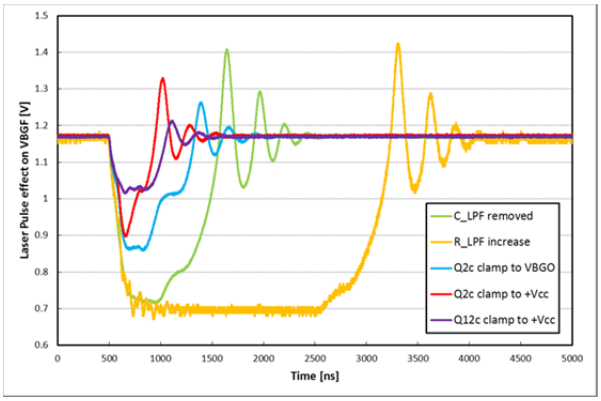

Figure 4: Yellow curve: SET induced LDP (as excited by laser equivalent to >100 MeV cm^2/mg); green, blue, purple, red: various circuit solutions that reduced LDP to acceptable duration for the tested LET.

Design Challenges & Mitigation: Elimination (and Classification) of Long Duration Pulses (LDP)

One of the goals for the UT16AD40P was fast recovery from SETs, specifically SET durations lasting only 1 sample clock cycle for the low LET values most frequently encountered in space for a sample rate of 10MSps. First and foremost, this requires an understanding of the sources of SET-induced Long Duration Pulses (LDPs). To that end, a test chip was designed and fabricated before the UT16AD40P design was completed. Using heavy ion irradiation, an LDP with ~600µs duration, 400mV-peak at the filtered output of the band-gap reference was observed. This would have impacted 24,000 cycles of a 40MSps ADC, with a range error up to 16% , had this circuit been used in the final device. In order to understand what design mitigation steps were possible, the same test chip structure was irradiated with laser, both at the United States Naval Research Laboratory (NRL) in Washington, DC and at Aeroflex Colorado Springs [1]. These laser studies isolated the LDP problem to a single device in the band-gap circuit. Owing to this understanding, several circuit solutions were subsequently designed and fabricated on another test chip, and irradiated using the laser at Aeroflex. The results of these runs are superimposed on the original test chip results and shown in Fig. 4. The LDP originally lasting 600µs was first reduced to ~2.5µsec and subsequently (red curve) minimized to < 500ns.

The problem of LDPs also illustrates the general problem of how to classify the SET probability for a given orbital environment, in a complex mixed-signal IC such as the UT16AD40P. Fig. 5(a) shows a cross-section curve when the criterion for SET rating is determined solely by the amplitude of the SET pulse. In this case, the cross section curve classifies events above 12mV (320 LSB's). Fig. 5(b) shows a cross section curve when the criterion is set for duration (irrespective of amplitude). In this case, the cross section refers to SETs lasting more than 2, 10, 50, and 100

sample clock cycles. The problem is reflected by the widely varying onset LETs and cross sections for the different SET conditions. It is apparent that a single cross section curve is not sufficient to give the system designer all the SET information needed to devise radiation-induced transient mitigation techniques at the system level, such as e.g. over-sampling.

In response to this problem, Aeroflex has recently proposed a comprehensive methodology for rating SETs [2] utilizing 3-D histograms - as shown in Fig. 6. The z-axis of the 3-D histograms is the normalized probability of SET events, determined by taking the number of SETs for any given base cell of the histogram and dividing by the total number of SETs observed. The x-axis is the duration of the SET measured in sample clocks, and the y-axis the maximum amplitude of the SET, in this case rated in LSBs of the 16-bit ADC. As can be seen in Fig. 6, there are no SETs with duration greater than 1 clock cycle at 30 MeV-cm^2/mg. Of course, the most desirable situation is to have all or most of the upset probability concentrated in the cell near the origin of the histogram. As the LET increases, we see that longer duration pulses start appearing, with small amplitude. The cross section curves in Fig. 5 can be generated by integrating each (non-normalized) 3-D histogram over the duration and amplitude of interest. Both the cross section curve in Fig. 5(b) and the histograms in Fig. 6 indicate that the goal of no LDPs has been achieved in this ADC.

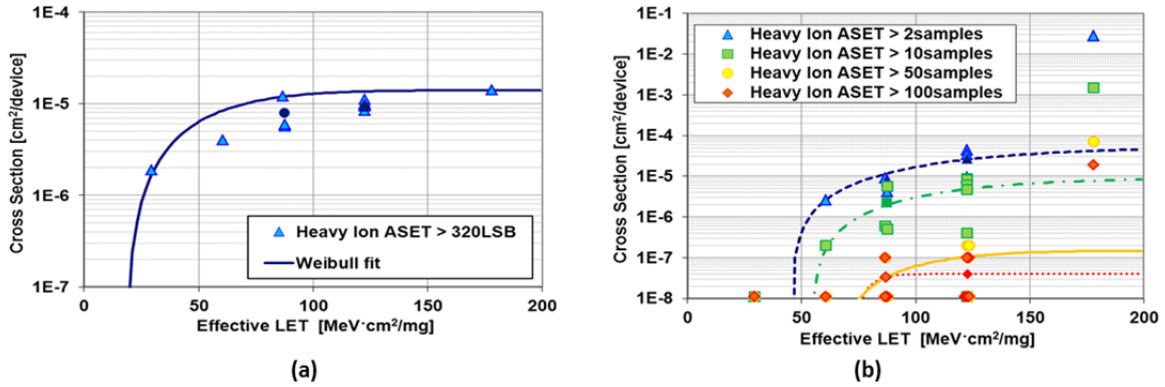

Figure 5: (a) Weibull fit of the data extracted from the 3-D histograms of the rad-hard ADC at increasing LET, for ASETs with peak amplitudes exceeding 12mV (>320LSB). (b) Weibull fit curves of ASETs of increasing durations, for the rad-hard ADC. The data points at the bottom indicate 0 events recorded for such runs.

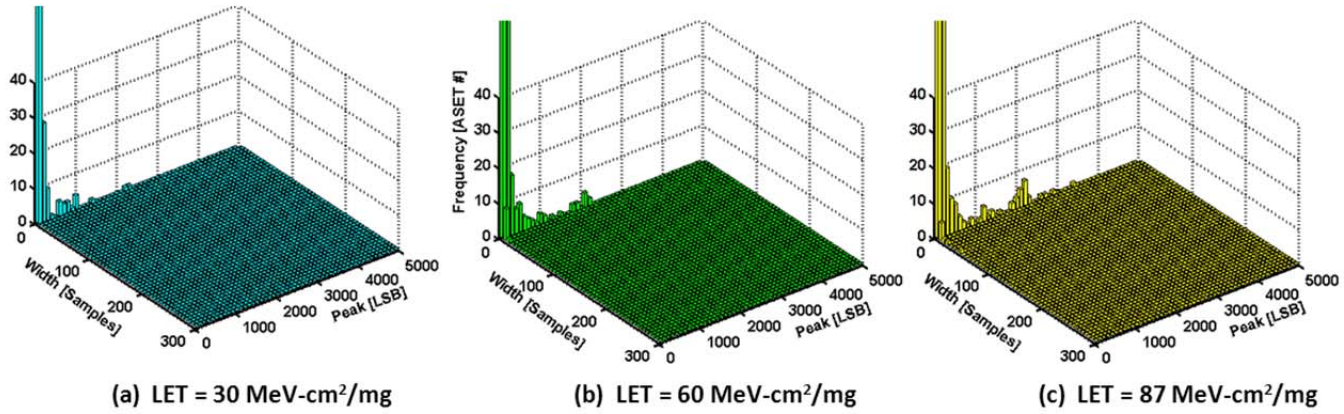

Figure 6: 3D Histograms of SETs in the UT16AD40P for (a) LET = 30 MeV-cm^2/mg, (b) LET = 60 MeV-cm^2/mg, and (c) LET = 87 MeV-cm^2/mg

CASE STUDY 3: UT04VS50P 4-Channel Voltage Supervisor

Fig. 7 shows a block diagram of the UT04VS50P 4-channel voltage supervisor. The UT04VS50P is a radiation-hardened Voltage Supervisor which simultaneously monitors up to four supply levels utilized in a system, providing status output for each signal, VOUTx, as well as, a system reset signal if any of the monitored signals moves out of range. To set the monitor trip points, the TH0 and TH1 pins allow the selection of three sets of preset threshold levels per channel, determined by an internal bandgap voltage reference, to reduce supply and temperature variance, and a fourth selection which allows the user to determine the level for each channel. There are two modes of operation,

determined by the OVSH pin. In the first mode, when the OVSH pin is connected to VSS, four independent supplies are monitored for an under-voltage condition. In the second mode when the OVSH pin is connected to VDD, then under-voltage and over-voltage of the inputs are monitored. In this mode, two supplies can be monitored using channels 1 and 3 or channels 2 and 4,respectively. The margin (or tolerance) to the given threshold voltage, for under-voltage monitoring, is determined by the setting of the TOL pin. The logic sense of the channel 3 and 4 outputs can be inverted by setting the INV pin, appropriately. Also, MRB, master reset, provides a means for a manual input to activate the RESET signals. In addition, the user can adjust two timing parameters by the addition of external capacitors to the device. These are the response times of the channel VOUTx signal when the associated input returns to a valid level, implemented by CDLYx, and the time to clear RESET (and RESETB) when a channel enable or input level becomes valid; implemented by CRESET.

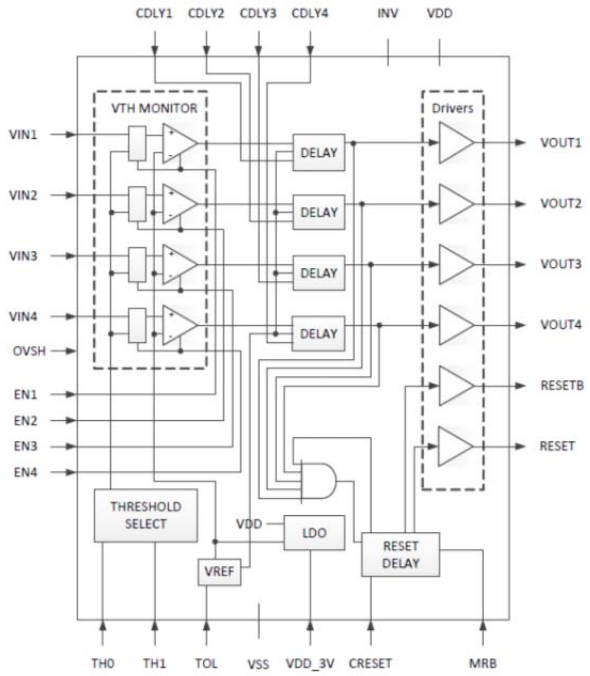

Figure 7: Block diagram of the UT04VS40P Voltage Supervisor

Table VII lists the key environmental requirements for this IC. The environment requires operation with a total ionizing dose (TID) of 300krad(Si), be latch-up immune up to a LET of 112 MeV-cm^2/mg, and very importantly, have no SETs observable on any of the output pin (VOUTx, RESET) or the input pin MRB below a LET of 80 MeV-cm^2/mg.

Table VIII shows the key features of the 0.35 µm mixed-signal CMOS process used. There are many features in common with the BCD technology in Table II, but the technology in Table VIII is from a different wafer foundry.

Table VII: Operating Environment for UT04VS50P

Environment	Requirement
Total Ionizing Dose (TID)	300krad(Si)
Single Event Latch-Up (SEL)	112 MeV-cm^2/mg
Single Event Transients (SET)	On-set LET for SET causing output glitches > 80 MeVcm^2/mg

Design Challenges & Mitigation: A Priori SET Error Rate Estimation and Design Mitigation

In order to avoid costly re-spins, an economical means of estimating SETs during mixed-signal design is required. Aeroflex developed two simulation codes, Qsim and SETsim to address this need [3]. Qsim creates single-event current sources for each reverse biased p-n junction in a SPICE netlist. These simulations are then used with a

designer-defined failure criterion to determine the critical charge that just causes such SET error. SETsim is a 3D ion simulator that determines the ion hit rate as a function of deposited charge for a given analog cell layout and orbital environment. The entire voltage supervisor family, including the UT04VS50P, was designed using Qsim and SETsim.

Table IX lists some key radiation results of the UT04VS50P. In addition to being SEL immune at the highest available LET of 112 MeV-cm2/mg, there were no SETs observed during a test session of 1E7 ions/cm^2 at a LET of 112 MeV-cm^2/mg. This is very important for an asynchronous device such as the UT04VS50P, which acts to protect microprocessors, digital signal processors (DSPs), field programmable gate arrays (FPGAs), and other complex digital or mixed-signal ICs, by asserting a reset signal of the power supply drops below a minimum (or optionally using the features of the UT04VS50P, exceeds a maximum) voltage on any of the monitored inputs.

Table VIII: Key Technology Features for UT04VS50P

Technology Type	0.35µm Mixed-Signal CMOS
Minimum Feature Size	0.35 µm
Well Structure	Triple-Well (Substrate Isolated)
Transistors Used	3.3V Enhancement Mode Isolated NMOS & PMOS (self-aligned) 5.0V Enhancement Mode Isolated NMOS & PMOS (self-aligned) Bipolar NPN (vertical)
Metallization and Interconnects	4LM, Tungsten Plugs, CMP Planarization
Resistors	Diffusion Resistors, Poly Resistors (non-salicided), Hi-Poly Resistors
Capacitors	MiM, MOS-caps
Aeroflex Enhancements	RH OTEP Metal Fuse

Table IX: Single Event Effects Results, UT04VS50P

Test	Results
SEL	> 112 MeV-cm^2/mg at 125°C, 5.5V
SET	No events @ 112 MeV-cm2/mg, 1E7 ions/cm^2

SUMMARY

Radiation Hardened Mixed-Signal IC designers face challenges that vary with the type of radiation environment and type of mixed-signal circuit being designed. Aeroflex has developed several design tools, laboratory characterization methods, and a comprehensive SET rating methodology that allows for first pass success in designing radiation hardened mixed-signal ICs, and provides the system designer complete SET information for system design decisions. Three case studies, the UT08SC14ADV04 smart sensor measurement system on a chip, the UT16AD40P pipe line ADC, and the UT04VS50P voltage supervisor were reviewed, and the application of one or more of the above tools during the development of each product was illustrated. The radiation results on the first pass silicon in each case met or exceeded the design goals, indicating that the tools are effective.

REFERENCES

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[3] D. Kerwin, "Mixed-Signal Design Methodology Using A Priori Single Event Transient Rate Estimates", *4th International Workshop on Analog and Mixed Signal Integrated Circuits for Space Applications*, Noordwijk, The Netherlands, 26 - 28 August 2012.