Ramon Chips is named in memory of Col. Ilan Ramon, Israeli astronaut who died on board the Columbia space shuttle, 1/2/2003

Advanced Features in RadSafe™ technology

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Outline

- RadSafe™ technology for 130nm
- All digital DLL
- Multi-IO buffer
- Mini-SERDES
- DDR2 interface
- SpaceFiber SERDES

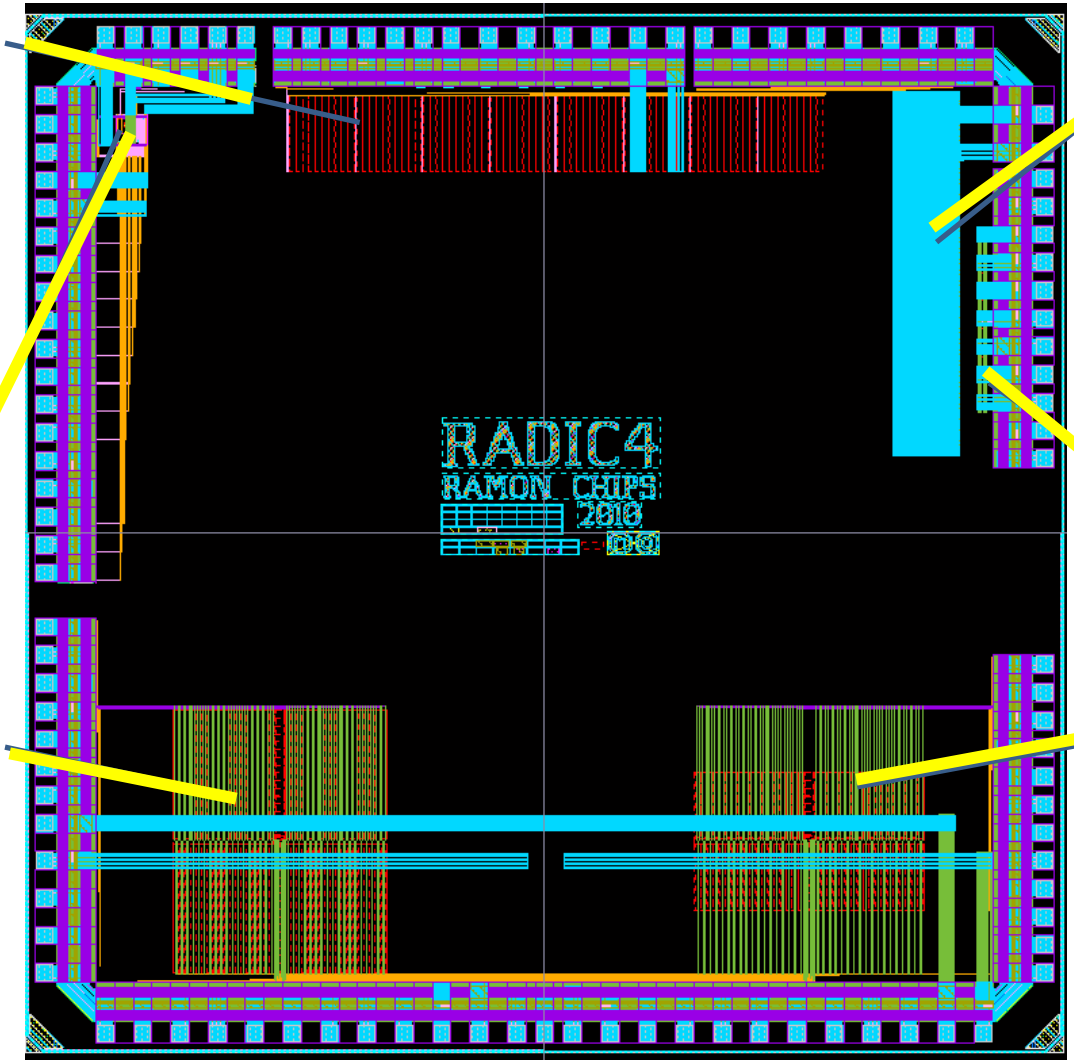
Selecting next generation technology

Parameter	0.13µ technology	Smaller geometries	Comments
Maturity & Reliability	+ More mature	- NBTI - TDDB	
Performance		+ Higher speed + Higher integration	• TDDB might limit supply voltage • SET filtering limits speed
Radiation hardening	+ Good TID & SEL	+ Good TID & SEL - More sensitive to SEU/SET	• High speed = high SEU/SET sensitivity
Power		+ 15% less per generation	• Mostly affected by supply voltage
Cost	+ 8” wafers + $250K / mask set	- 8” / 12” wafers - $1M mask set - Higher EDA cost	• RET increases mask cost • Xtalk is worse at small geometries
Availability	+ Available in Tower, iHP	- Available in large foundries only (ST, Lfoundry, …)	• Large foundries less willing to service space industry

RadSafe™ 0.13µ technology

- Density:
  - Logic > 120 Kgates / mm^2 (40K at 0.18µ)
  - SRAMs > 200 Kbit / mm^2 (80K at 0.18µ)
- Power < 40% of 0.18µ
- Speed > 250MHz [for large chips]
- SRAM cell size 4.4µ2
- Max core size 4048x72 = 290 Kbit (=32Kbyte +ECC)
  - Larger cores assembled with digital logic
  - EDAC added with digital logic

RADIC4: Test chip for RadSafe_013 technology



3 shift registers

10b RH ADC (1Msps,1mW)

4Kx72 RH SRAM

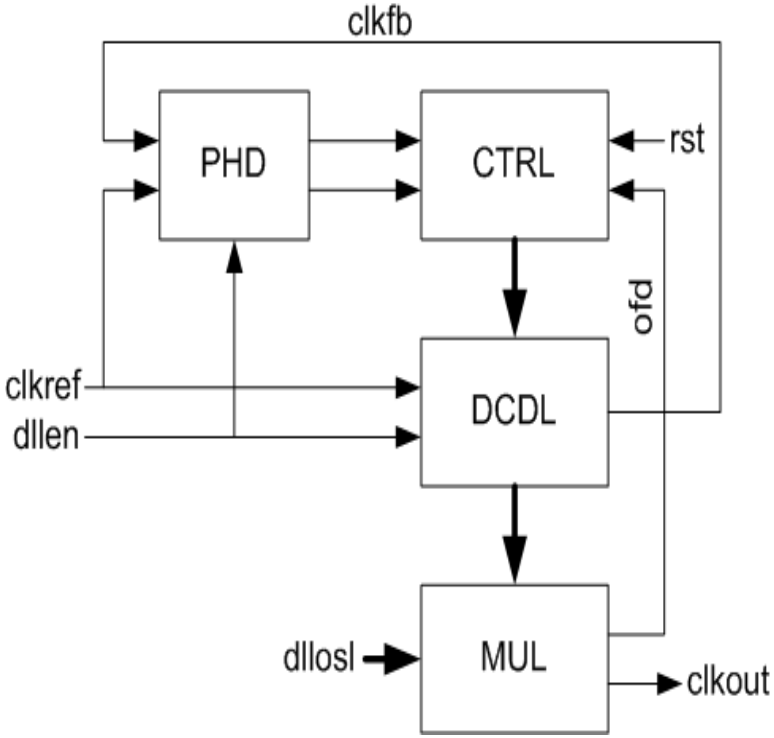
3 delay lines/ SET monitor

NMOS/PMOS Xtors

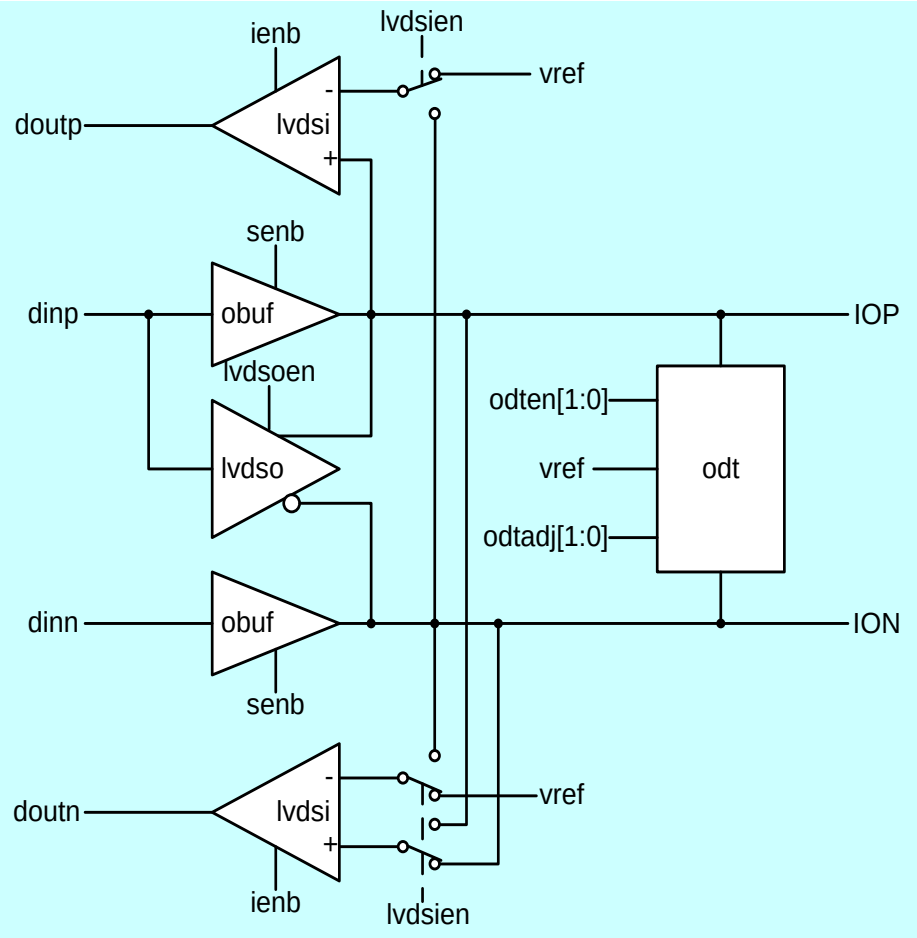
2Kx72 RH SRAM

Fault tolerant all-digital DLL

- Multiply frequency by 1/2/4
- Input frequency: 40-200MHz
- Output frequency: ≤ 400MHz
- Fully digital
- Over-frequency detector guarantees locking
- Fast locking / immediate re-locking
- Low power / small area
- Radiation hardened



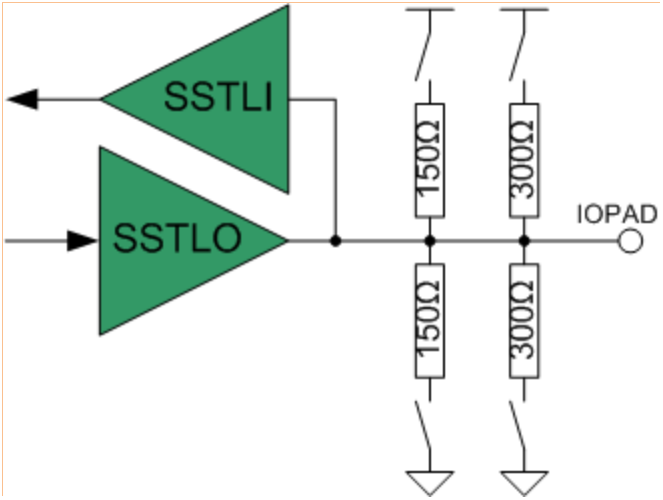
Fast configurable multi-IO buffer



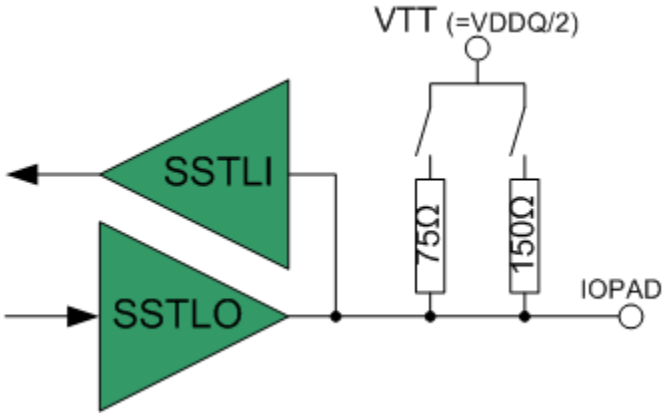
- LVDS input/output *(>800Mbps)*
- SSTL2/SSTL18 input/output *(>400Mbps)*
- LVTTL/LVCMOS25/LVCMOS18 input/output
- Tunable drive strength of LVDS
- Configurable ODT of 150/75/50 ohm/pin (single ended)
- Configurable ODT of 300/150/100 ohm/pair
- Calibrated ODT
- ODT referenced to VTT (= 1.2/0.9V)
- Independent power domain (2.5/1.8V)

Comparing termination concepts for SSTL18

- Without VTT [common]
  - Consumes DC current
  - Switch supply current
  - Termination of 50/75/150Ω

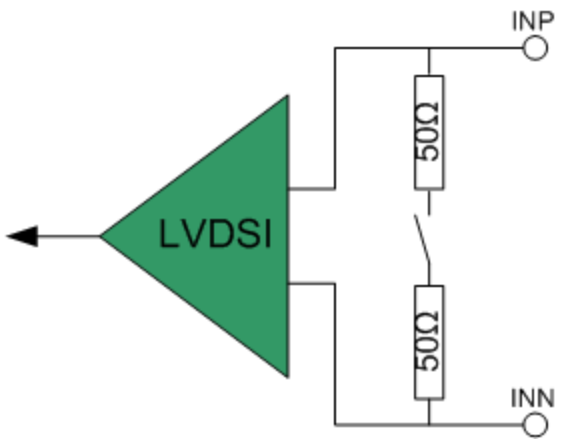


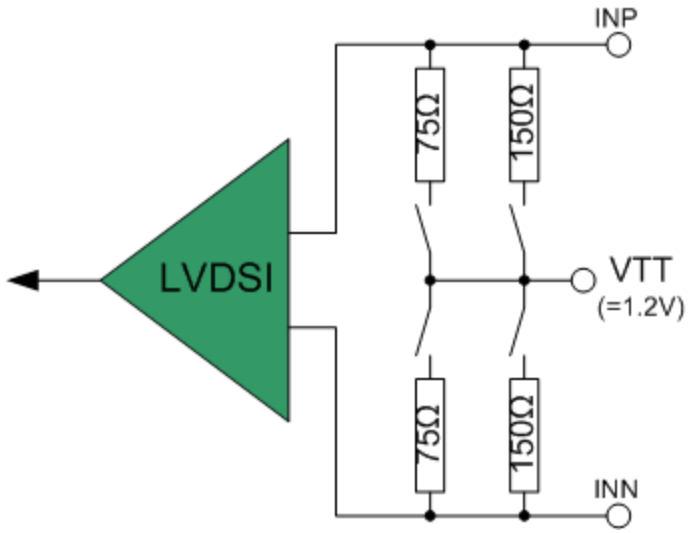
- With VTT [RadSafe]
  - No DC current
  - No switching of supply current
  - Requires VTT pin for balancing to VDDQ/2
  - Termination of 50/75/150Ω



Comparing termination concepts for LVDSI

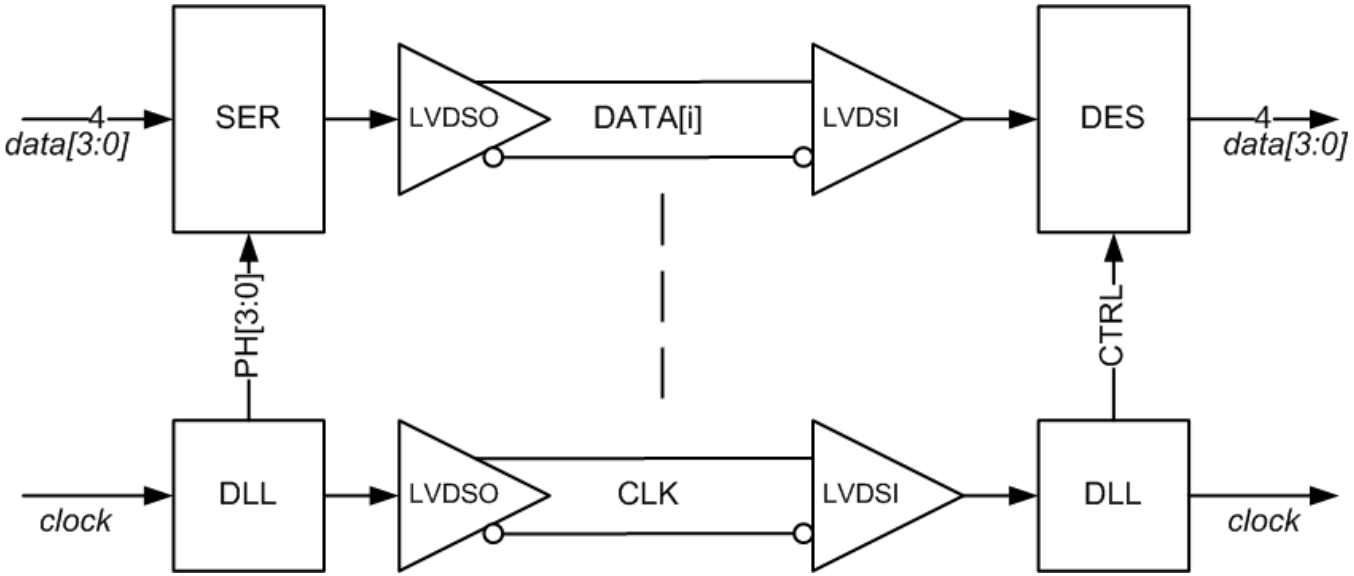
- Without VTT [common]
  - 100Ω termination only
- With VTT [RadSafe]
  - Adjustable termination resistance (300/150/100Ω)
  - Wide common mode range
  - Tolerant to discontinuities
  - Requires VTT





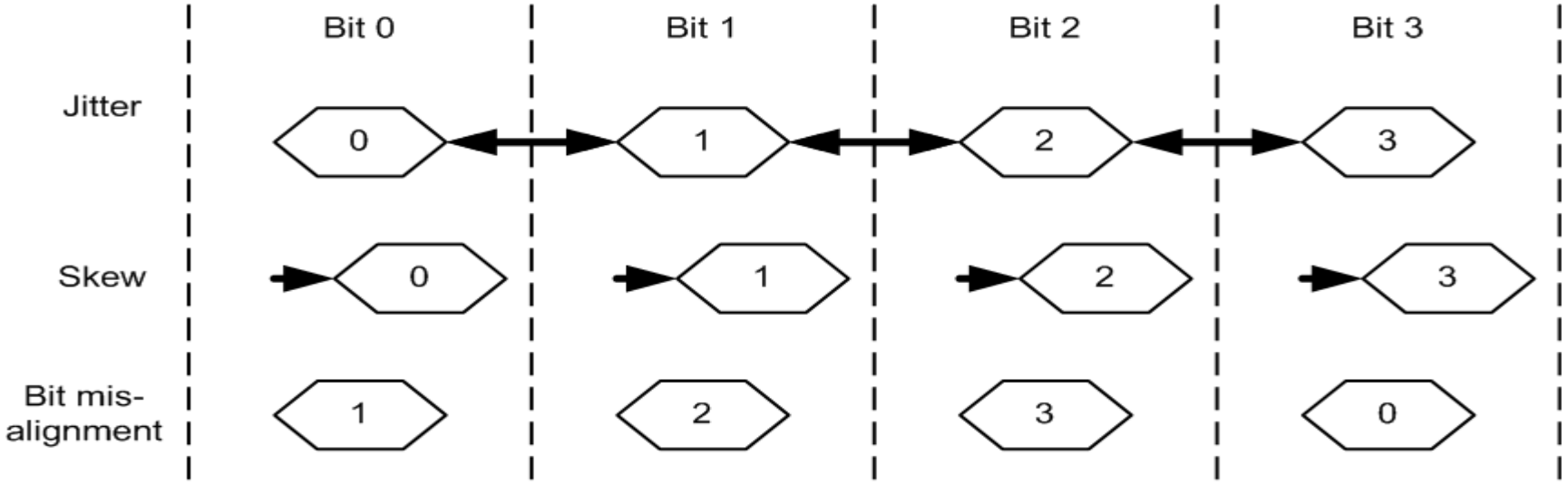
Mini-SERDES architecture

- 4 bits per LVDS signal pair
- Typical data rates – 4x200MHz <-> 1x800MHz
- Fully digital implementation
- Configurable ODT – low power, no extra components



De-serializer concept

- Performs Automatic Timing Adjustment per bit
- Performs Eye Opening by over sampling
- Performs Bit Alignment by locking to SYNC pattern
- Does not require on-board balancing of trace length

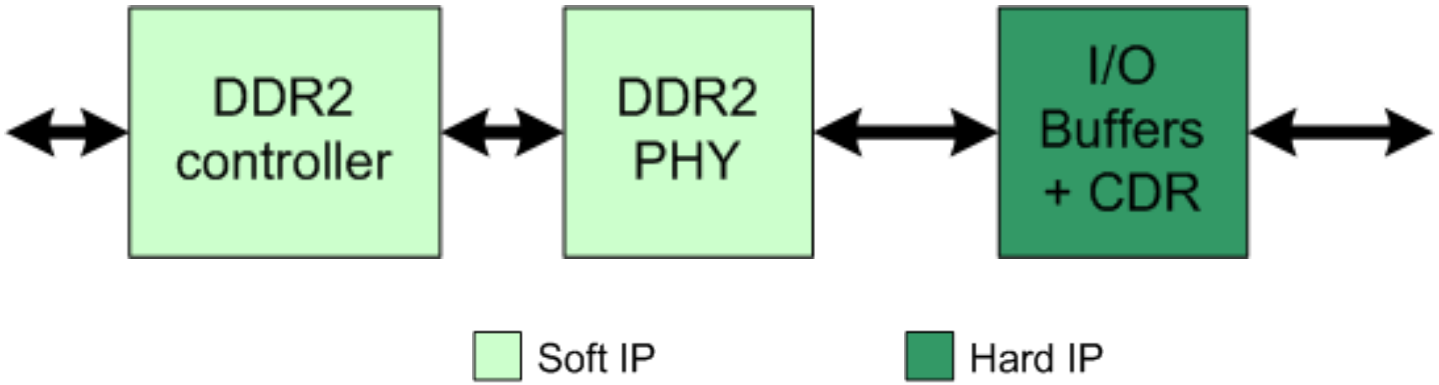


Advantages of mini-SERDES I/F

- High data rate
- Low latency – no encoding & decoding
- Robust differential signaling, low EMI
- Low power and low switching noise
- Almost unconstrained PCB routing
- No passives on board
- Fully implemented by rad-hard digital circuits
- Low area

DDR2 interface

- Enables interfacing with DDR2 memories
- Enables DDR2_400/533 (package dependent)
- Integrates “soft IP core” controller & PHY
- I/O block includes:
  - Multi-IO buffers configured as SSTL18
  - Proprietary CDR for dynamic timing alignment



EU R&D: SpaceFibre SERDES

- 2.5 Gbit/sec *SpaceFibre*
- EU FP7 project “VHiSSI” (2012-2014)
- With:
  - Astrium (DE)
  - Star-Dundee (UK)
  - iHP (DE)
  - EIT (IT)
  - ACE-IC (IL)

Summary

- RadSafe_130 technology with improved standard cells, SRAMs and ADDLL provides state-of-the-art performance, very high reliability, radiation hardening and affordable prices
- Configurable multi-IO buffers enable high data rate
  - When using LVDS or SSTL signaling and ODT
- DDR2 interface under development
  - Soft digital IP cores and multi-IO buffers
- SpaceFibre SERDES under development
  - Enabling 2.5 Gbps data communication
- These enhancements will enable the implementation of >10GIPS RC64 many-core chip