Advanced Features in RadSafe™ technology

Tuvia Liran [tuvia@ramon-chips.com]
Ran Ginosar [ran@ramon-chips.com]
Ramon-Chips Ltd., Israel
Outline

• RadSafe™ technology for 130nm
• All digital DLL
• Multi-IO buffer
• Mini-SERDES
• DDR2 interface
• SpaceFiber SERDES
## Selecting next generation technology

<table>
<thead>
<tr>
<th>Parameter</th>
<th>0.13µ technology</th>
<th>Smaller geometries</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maturity &amp; Reliability</td>
<td>+ More mature</td>
<td>- NBTI</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>- TDDB</td>
<td></td>
</tr>
<tr>
<td>Performance</td>
<td></td>
<td>+ Higher speed</td>
<td>• TDDB might limit supply voltage</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+ Higher integration</td>
<td>• SET filtering limits speed</td>
</tr>
<tr>
<td>Radiation hardening</td>
<td>+ Good TID &amp; SEL</td>
<td>+ Good TID &amp; SEL</td>
<td>• High speed = high SEU/SET sensitivity</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- More sensitive to SEU/SET</td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td></td>
<td>+ 15% less per generation</td>
<td>• Mostly affected by supply voltage</td>
</tr>
<tr>
<td>Cost</td>
<td>+ 8” wafers</td>
<td>- 8” / 12” wafers</td>
<td>• RET increases mask cost</td>
</tr>
<tr>
<td></td>
<td>+ $250K / mask set</td>
<td>- $1M mask set</td>
<td>• Xtalk is worse at small geometries</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Higher EDA cost</td>
<td></td>
</tr>
<tr>
<td>Availability</td>
<td>+ Available in Tower, iHP</td>
<td>- Available in large foundries only (ST, Lfoundry, ...)</td>
<td>• Large foundries less willing to service space industry</td>
</tr>
</tbody>
</table>
RadSafe™ 0.13µ technology

• Density:
  – Logic > 120 Kgates / mm² (40K at 0.18µ)
  – SRAMs > 200 Kbit / mm² (80K at 0.18µ)

• Power < 40% of 0.18µ

• Speed > 250MHz [ for large chips ]

• SRAM cell size 4.4µ²

• Max core size 4048x72 = 290 Kbit (=32Kbyte +ECC)
  – Larger cores assembled with digital logic
  – EDAC added with digital logic
RADIC4: Test chip for RadSafe_013 technology

- 3 shift registers
- 10b RH ADC (1MspS, 1mW)
- 4Kx72 RH SRAM
- 2Kx72 RH SRAM
- 3 delay lines/SET monitor
- NMOS/PMOS Xtors
Fault tolerant all-digital DLL

- Multiply frequency by 1/2/4
- Input frequency: 40-200MHz
- Output frequency: \( \leq 400\)MHz
- Fully digital
- Over-frequency detector guarantees locking
- Fast locking / immediate re-locking
- Low power / small area
- Radiation hardened
Fast configurable multi-IO buffer

- LVDS input/output (>800Mbps)
- SSTL2/SSTL18 input/output (>400Mbps)
- LVTTL/LVCMOS25/LVCMOS18 input/output
- Tunable drive strength of LVDS
- Configurable ODT of 150/75/50 ohm/pin (single ended)
- Configurable ODT of 300/150/100 ohm/pair
- Calibrated ODT
- ODT referenced to VTT (= 1.2/0.9V)
- Independent power domain (2.5/1.8V)
Comparing termination concepts for SSTL18

• **Without VTT** [common]
  – Consumes DC current
  – Switch supply current
  – Termination of 50/75/150Ω

• **With VTT** [RadSafe]
  – No DC current
  – No switching of supply current
  – Requires VTT pin for balancing to VDDQ/2
  – Termination of 50/75/150Ω
Comparing termination concepts for LVDSI

- **Without VTT [common]**
  - 100Ω termination only

- **With VTT [RadSafe]**
  - Adjustable termination resistance (300/150/100Ω)
  - Wide common mode range
  - Tolerant to discontinuities
  - Requires VTT
Mini-SERDES architecture

- 4 bits per LVDS signal pair
- Typical data rates – 4x200MHz <-> 1x800MHz
- Fully digital implementation
- Configurable ODT – low power, no extra components
De-serializer concept

- Performs Automatic Timing Adjustment per bit
- Performs Eye Opening by over sampling
- Performs Bit Alignment by locking to SYNC pattern
- Does not require on-board balancing of trace length
Advantages of mini-SERDES I/F

- High data rate
- Low latency – no encoding & decoding
- Robust differential signaling, low EMI
- Low power and low switching noise
- Almost unconstrained PCB routing
- No passives on board
- Fully implemented by rad-hard digital circuits
- Low area
DDR2 interface

- Enables interfacing with DDR2 memories
- Enables DDR2_400/533 (package dependent)
- Integrates “soft IP core” controller & PHY
- I/O block includes:
  - Multi-IO buffers configured as SSTL18
  - Proprietary CDR for dynamic timing alignment
EU R&D: SpaceFibre SERDES

• 2.5 Gbit/sec *SpaceFibre*

• EU FP7 project “VHiSSI” (2012-2014)

• With:
  – Astrium (DE)
  – Star-Dundee (UK)
  – iHP (DE)
  – EIT (IT)
  – ACE-IC (IL)
Summary

• RadSafe_130 technology with improved standard cells, SRAMs and ADDLL provides state-of-the-art performance, very high reliability, radiation hardening and affordable prices

• Configurable multi-IO buffers enable high data rate
  – When using LVDS or SSTL signaling and ODT

• DDR2 interface under development
  – Soft digital IP cores and multi-IO buffers

• SpaceFibre SERDES under development
  – Enabling 2.5 Gbps data communication

• These enhancements will enable the implementation of >10GIPS RC64 many-core chip