Advanced Features in RadSafe™ technology

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Abstract

The next generation RadSafe™ technology is dedicated to advance System on Chip (SoC) devices for space applications of digital signal processing and micro-processors. The technology should maximize processing performance by combining advanced micro-architecture, advanced silicon technology and high speed interfacing to peripheral devices. However, the requirements for very high reliability, cost and availability limit the use of the most advanced technologies.

For the next generation RadSafe™ technology we selected the 0.13µm technology. It provides significant improvement of performance and power, while this technology is mature, and available for affordable price.

Some of the improvements in the design infrastructure are presented. It includes improvements of the multi-I/O buffers and improved DLL cores. Several new cores will be introduced, include high speed SERDES and DDR2 I/F.

The new capabilities will enable the implementation of space grade RC64 – multi core processor, that will provide >10G instructions per second, mostly for signal processing.

A test vehicle for demonstrating the analog capabilities of the RadSafe™ technology is the compact 10b SAR ADC. This rad-hard core consumes only 1.5mW, the area is ~0.03mm^2, and use fully digital process flow, including for the analog circuits.

Introduction

Geometry scaling enables high performance digital processing. Currently (2012) most of the COTS space components are based on ≥0.18µm CMOS technologies, mostly due to reliability and availability constrains. ESA has selected 65nm as the selected technology for future generations. However, the cost barrier of such technology and reliability concerns are slowing the adoption of this technology for space. The 0.13µm is available, affordable, and can provide the required reliability and performance.

The RadSafe™ technology was used and qualified for GR712RC and JPIC SoCs, using 0.18 µm [1]. Next generation processors, such as multi core signal processors, require faster operation. The lessons learned from these products, and the potential of technology scaling, are implemented in the next generation libraries. The following will describe the key improvements.

One of the performance obstacles of space grade components is the low performance of the packages. The most reliable package is QFP, which have high inductance on its leads. The use of VDDIO=2.5V reduces the swing of the LVTTL and LVCMOS signals, while using faster devices than for 3.3V, and maintain the tolerance to 3.3V signaling. The new I/O library also enables the use of isolated power domains, which are needed for several applications, such as high speed interfacing.

The need for high frequency clocking dictates the need for rad-hard

PLL (phase locked loop) or DLL (delay locked loop) for clock multiplication and de-skewing. The use of all-digital delay locked loop (ADDLL), with expanded tuning range, and low jitter, enables useful internal clock frequency of >400MHz. Since the control data is stored in digital flip-flops, the operation of these DLLs can start and stop at any time, with no latency for re-locking.

High performance processors requires advanced and high capacity external memories. For interfacing with DDR2 memories, and complete DDR2 interface is under development. The use of multi-IO buffers will enable dual use of the buffers, for other applications as well.

Transferring high data rate with limited number of signals and package pins requires the use of SerDes. The RadSafe™ SerDes is currently under development, which exceeds 2.5Gbps, is compatible with several standard interfacing protocols, including SpaceFiber. It is immune to all radiation effects. To enable the use of high inductance packages, it includes configurable equalizers.

Advanced I/O cells

The I/O library is powered by 2.5V supply. It provides ~30% faster response due to smaller voltage swing and faster devices. The standard buffer cells are tolerant to 3.3V signals, and can interface any 3.3V device with TTL signal levels. In addition, these cells are compatible with cold spare.

LVDS buffers, with cold spare and fail safe capabilities had been developed. These buffers enables >400MHz speed (800Mbps @DDR) at extreme temperatures. The output current is referenced externally, enabling tuning the drive strength for optimal speed and power performance.

The DDR2 PHY requires SSTL18 bi-directional and differential uni-directional buffers, powered by isolated 1.8V supply. These buffers includes switchable on die termination (ODT) with adjustable impedance of 50/75/150Ω. The reference voltage for the resistive termination, VTT, is driven by external pin, typically connected to 1.2V. This ODT technique consumes much less DC power than the conventional technique, where the termination is implemented by resistors to VDD and GND (Figure 1). Same ODT can be used for SSTL18 and LVDS, enabling wider range of impedances, that enables power reduction in some applications.

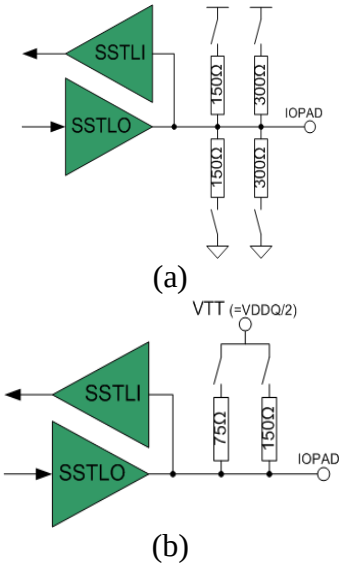

Figure 1: Conventional (a) and RadSafe™ (b) termination methods

To enable configuring the use of the same pins for either LVDS, powered by 2.5V, or SSTL18, powered by 1.8V supply, in either directions, we developed a fast multi-IO cell, presented in Figure 2.

Several applications, such as fast multi-IO cells, require isolated power domains. A complementary library cells and methodology enables that capability, while supporting high ESD immunity and low resistance of supply traces.

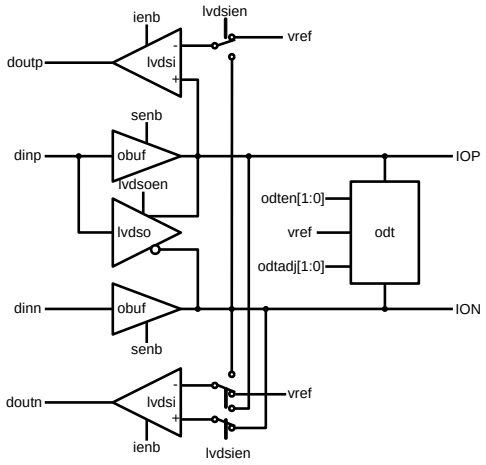

Figure 2: Schematic of multi-IO cell in RadSafe™ library

All digital DLLs

The need for clock multiplication and de-skewing is achieved by DLL core. The tuning range of input frequency is 25÷125MHz, while the output can be configured to 1X/2X/4X/bypass of reference input. The resolution is typically <20pS. Special features provide immunity to SET, and locking is constantly traced. The ADDLL is presented in Figure 3. The core is placed in the I/O ring, and power with internally regulated power supply.

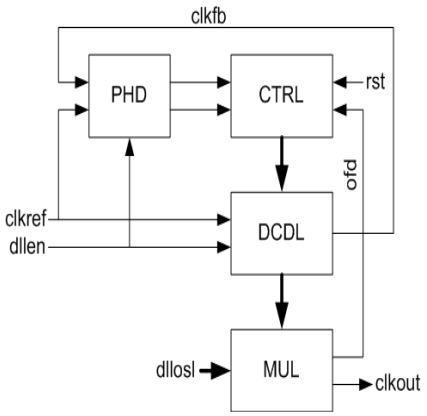

Figure 3: All-digital DLL core

DDR2 PHY

The DDR2 is becoming the standard memory interface for the next generation processors for space. The interface includes multi-IO buffers, and synthesizable CDR and DDR2 controller, which are integrated in the core logic.

SerDes core

The SpaceFiber is an emerging standard for chip-chip and board-board interfacing up to 3m, for data rates up to 2.5Gbps. It is based on general purpose analog SerDes, with advance configurable equalizer to support wide range of packages and transmission medias.

The design technology is currently under mutual development by Star Dundee (UK), Ramon Chips and ACE-IC (Israel), participating in VHiSSI project - an FP7 program.

Summary

We had upgraded our design infrastructure of cells and cores for advanced SoCs. It is an improved version of RadSafe™ libraries, ported to conventional 0.13µm process technology. It support high speed interfaces, like DDR2 and high speed SerDes. This technology provides all the building blocks needed for implementing high performance multi-core processor for DSP applications.

All these advanced circuits are designed to mitigate all radiation effects, and providing very high reliability.

References

[1] T. Liran et al, "A Radiation-Hardened Design Flow for Advanced SoC", DASIA 2010, June 2010