IHP BiCMOS technologies for RF and mixed signal applications

August 26 - 28, 2012

R.F. Scholz, F. Teply, M. Cirillo

IHP
Im Technologiepark 25
15236 Frankfurt (Oder)
Germany
Outline

Introduction

0.25µm BiCMOS - SGB25RH
  - Technology description
  - Evaluation Status
  - Running radhard library project

0.13µm BiCMOS - SG13S
The IHP`s Building in Frankfurt (Oder)
IHP in a Nutshell

• Institute of the Leibniz Association
  Owned by the State of Brandenburg; limited liability company since 1991

• Founded in 1983
  Long term experience in silicon technology & materials research

• Silicon based high-frequency technologies, circuits and systems
  for the wireless and broadband communication

• 300 people from 20 countries
  Among them 139 scientists

• Certified DIN EN ISO 9001:2008
## Pilot Line

<table>
<thead>
<tr>
<th>Cleanroom Size</th>
<th>~1000 m² Class 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>RF SiGe:C BiCMOS</td>
</tr>
<tr>
<td>Wafer Size</td>
<td>200 mm</td>
</tr>
<tr>
<td>Capacity</td>
<td>100 Wafer Starts / Week</td>
</tr>
<tr>
<td>Tool Set Capability</td>
<td>0.25µm / 0.13 µm</td>
</tr>
<tr>
<td>Mode of Operation</td>
<td>24h, 7 Days / Week</td>
</tr>
<tr>
<td>SiGe:C BiCMOS Cycle Time</td>
<td>≥1.7 Days / Mask level</td>
</tr>
</tbody>
</table>
Application Specific Integrated Circuit (ASIC) development flow

- **ASIC Design**
- **Prototyping (MPW) Test, Redesign**
- **Fabrication**
- **On wafer test**
- **Assembly & final test**

**IP- IHP System/Circuit Design**
/D Design partner Arquimea Ingenieria, Madrid
**MPW run**
Several customer share one wafer

**Customer 1**
**Customer 2**
**Customer 3**

**Engineering run**

**Performed in IHP Labs**

**Organized with external partners**
Cicor/RHe Micross UK
## Technology Roadmap
### (complete technologies)

<table>
<thead>
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</tr>
</thead>
<tbody>
<tr>
<td>SGB25V</td>
<td>$f_T/f_{MAX}$[GHz]/$BV_{CE0}$[V]</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td>0.25 µm</td>
</tr>
<tr>
<td>SGB25V</td>
<td>75/95/2.4, 45/90/4, 25/70/7</td>
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</tr>
<tr>
<td>SGB25RH (SGB25V)</td>
<td>75/95/2.4, 45/90/4, 25/70/7</td>
<td>2012 Q1</td>
<td>2012 Q2</td>
<td>2012 Q3</td>
<td>2012 Q4</td>
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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>SG25H3</td>
<td>120/140/2.4, 110/180/2.3, 45/140/5, 30/80/7</td>
<td></td>
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<tr>
<td>SG25H1</td>
<td>190/190/1.9, 180/220/1.9</td>
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<tr>
<td>SG13S</td>
<td>250/300/1.7, 45/120/3.7</td>
<td></td>
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</tr>
<tr>
<td>SG13RH (SG13S)</td>
<td>240/300/1.7, 50/120/3.7</td>
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<tr>
<td>SG13G2</td>
<td>300GHz/ 500GHz /1.6 (no digital libs)</td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td>0.13 µm</td>
</tr>
</tbody>
</table>

August 2012
## MPW Schedule 2012

<table>
<thead>
<tr>
<th>TAPE IN</th>
<th>Shipment</th>
<th>SGB25</th>
<th>SG25</th>
<th>SG13</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>V</td>
<td>H1</td>
<td>H3</td>
</tr>
<tr>
<td>Dec 12, 11</td>
<td>Apr 20, 12</td>
<td></td>
<td></td>
<td>x</td>
</tr>
<tr>
<td>Jan 09, 12</td>
<td>Apr 02, 12</td>
<td>x</td>
<td>x^1</td>
<td>x</td>
</tr>
<tr>
<td>Apr 16, 12</td>
<td>Aug 27, 12</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Apr 30, 12</td>
<td>Jul 23, 12</td>
<td>x</td>
<td>x^1</td>
<td>x</td>
</tr>
<tr>
<td>Jul 30, 12</td>
<td>Nov 19, 12</td>
<td></td>
<td></td>
<td>x</td>
</tr>
<tr>
<td>Sep 03, 12</td>
<td>Nov 27,12</td>
<td>x</td>
<td>x^1</td>
<td>x</td>
</tr>
<tr>
<td>Nov 05, 12</td>
<td>Feb 11, 13</td>
<td>x</td>
<td>x^1</td>
<td></td>
</tr>
<tr>
<td>Dec 10, 12</td>
<td>Apr 19, 13</td>
<td></td>
<td></td>
<td>x</td>
</tr>
</tbody>
</table>

1  Shipment 7 days later

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### TAPE IN

<table>
<thead>
<tr>
<th>TAPE IN</th>
<th>Shipment (standard)</th>
<th>GD</th>
<th>H3P</th>
<th>RF-MEMS switch^1</th>
<th>LBE^1</th>
<th>Cu Plating (with IZM)^2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jan 09, 12</td>
<td>May 14, 12</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>Apr 30, 12</td>
<td>Aug 27, 12</td>
<td>x</td>
<td></td>
<td>x</td>
<td>x</td>
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</tr>
<tr>
<td>Sep 03, 12</td>
<td>Jan 07, 13</td>
<td>x</td>
<td>x</td>
<td>x</td>
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<td>x</td>
</tr>
<tr>
<td>Nov 05, 12</td>
<td>March 11,13</td>
<td>x</td>
<td></td>
<td>x</td>
<td>x</td>
<td></td>
</tr>
</tbody>
</table>

^1 Localized Backside Etching shipment 12 days later than standard shipment
^2 Cu Plating Shipment 8 weeks after standard shipment
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0.13µm BiCMOS - SG13S
# SGB25RH Process Options

<table>
<thead>
<tr>
<th>Features</th>
<th>SGB25V / SGB25RH Full BiCMOS</th>
</tr>
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<tbody>
<tr>
<td><strong>Bipolar</strong> (fT/fmax/BVCE0)</td>
<td></td>
</tr>
<tr>
<td>High-speed HBT:</td>
<td>80 GHz/ 100 GHz/ 2.4 V</td>
</tr>
<tr>
<td>Medium-voltage HBT:</td>
<td>45 Ghz/ 120 GHz /4 V</td>
</tr>
<tr>
<td>High-voltage HBT:</td>
<td>28  GHz/ 120 GHz/ 7 V</td>
</tr>
<tr>
<td><strong>CMOS</strong></td>
<td></td>
</tr>
<tr>
<td>Vdd=2.5V, Tox=5nm</td>
<td></td>
</tr>
<tr>
<td><strong>CMOS logic</strong></td>
<td>Digital libraries</td>
</tr>
<tr>
<td><strong>Passives</strong></td>
<td>Poly-Si resistors, MIM capacitors, MOS varactors, a.o.</td>
</tr>
<tr>
<td><strong>Interconnects</strong></td>
<td>5 layer Al incl. 2µm &amp; 3µm thick layers</td>
</tr>
</tbody>
</table>
SGB25V/SGB25RH (1-mask) HBT Construction

There are 3 HBTs differing in $BV_{CEO}$ and peak $f_T$.

The different curves explain the typical scattering across an 8” wafer.
SGB25RH Elements and Applications

Basic structure elements:

- PMOS
- NMOS
- Isolated NMOS
- MOS Varactor
- RPND resistor
- RSIL resistor
- RPPD resistor
- RHIGH resistor
- MIM Capacitor
- npnVS bipolar HBT
- npnVH bipolar HBT
- npnVP bipolar HBT
- Inductor made by backend metal layer
- Antenna diode
- ESD clamp
- Digital standard cells
- Digital IO cells

Components in CMOS, bipolar and BiCMOS:

- Maximal application frequency up to 20 GHz
- as chip or packaged
- Mixed Signal Technology
- fast counters
- fast shift register
- FlipFlops
- Dividers
- Frequency-/Phase comparator
- Charge pumps
- VCOs
- Linear amplifiers
- Current sources
- PLLs (integer and fractional)
- Digital Analog Converters
- etc.
IHP Cadence DFII Design Flow

Layout design
layout input
Virtuoso
DRC
Assura
LVS
Assura
Filler Generation
Assura
GDSII
xstream
Tape-out

Schematic entry
Parasitic Extraction
Assura/QRC COLUMBUS
Schematic entry
Virtuoso
Digital entry
Encounter

Simulation
EM simulation
MOMENTUM SONNET
Mixed signal & RF simulation
APS (AMS Designer) Spectre/GoldenGate
Waveform Viewer
AWD, DDS
Test vehicle evaluation by DLR/ESA

TCV – standard technology test segments packaged in DIL64 (HBTs, NMOS, PMOS, resistors, MIM, MOS varactor, diodes)

DEC – Circuit blocks in Stratege 64 pin RF package (CMOS RO, CMOS shift register, bipolar ROs, ECL shift register with internal VCO)

RIC – 20 GHz VCO with divider, 6GHz output and SPI interface to control frequency, KYOCERA package
Status of SGB25RH evaluation

• TCV: 4000 hours passed, Expected failures occurred, test report available, 250°C storage test OK but gold wire packages fail, 275°C storage test up to 500h OK, 125°C storage test in package OK
• RIC: Long term stress test passed 4000 hours without errors
• DEC: 2 step stress done without errors as of May 2012, 2 more to do, Long Term stress to be done afterwards
• All tests (DEC) finished end of 2012
• Parts for DPA sent to ESA
• DLR/ESA Audit performed successfully 19th/20th of October 2011
• Final Goal IHP technology in preferred part list
Radiation test Data SGB25V/SGB25RH

• Teply et. al.: Radiation Hardness Evaluation of a 0.25 μm SiGe BiCMOS Technology with LDMOS Module, RADECS 2011 Data Workshop, available online at IEEE Xplore

• Kayser-Threde: Radiation Test Report - TID on early Structures (30-20-RP-KT-001_2)
• Kayser-Threde: Radiation Test Report - SEE on early Structures (30-20-RP-KT-002_2)
• Kayser-Threde: Radiation Test Report - TID Verification LO7 (3020-RP-KT-005)
• Kayser-Threde: Radiation Test Report - SEE Verification LO7 (3020-RP-KT-006)
Additional activity:
Test of Radhard library in SGB25RH

• New DRC Rules on Transistor Level
  Disabling of Latchup Rules is Forbidden
  Gate Poly extension of MOS gate is limited
  PWell and Nwell contact rings must have limited dimensions
  All Devices must be located within contacted NWell/PWell Ring
  Gate Poly have not to cross any well border
  Gate Poly must be within NWell or Pwell
  Active Shapes on different nets must be shielded with well contact

• Applied in Dolphin cell library and integrated the standard Cadence design flow
Evaluation of Radhard Library

Goal:
• Design Test structures to characterize each types of Single Event Upsets

Categories of Test Structures:
• Register cells: FlipFlops, latches, RAM
• Combinational Logics: Using NAND/NORS
• Special Structures: IO, Bandgap circuits
• Test pattern – Generator/ion
• FPGA / Labview

Radiation Tests:
• Heavy ion tests with effective LETs ranging from 1.8 MeV*cm²/mg to >80 MeV*cm²/mg
# Test Structures

<table>
<thead>
<tr>
<th>TEST STRUCTURES</th>
<th>MEASUREMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Registers</td>
<td></td>
</tr>
<tr>
<td>a Static shift registers - Stages 2048</td>
<td></td>
</tr>
<tr>
<td>b Dynamic Shift Registers - 1024</td>
<td></td>
</tr>
<tr>
<td>2 Ring Oscillators</td>
<td>Operational frequency and power consumption Inverter propagation delay, $T_{pd}$ with Varying LETs, Power delay wrt $V_{DD}$ with Varying LETs</td>
</tr>
<tr>
<td>1000+1 stages</td>
<td></td>
</tr>
<tr>
<td>3 SRAM</td>
<td>Transient Faults Static and Dynamic Modes of operation Single Bit and Multi Bits Upset Distribution SEUs (varying $V_{DD}$ and Temperatures over LET)</td>
</tr>
<tr>
<td>4 IO - LVDS</td>
<td></td>
</tr>
<tr>
<td>5 ECL Shift Registers</td>
<td></td>
</tr>
<tr>
<td>6 Bandgap Reference</td>
<td></td>
</tr>
</tbody>
</table>

All digital structures are variants: `sgb25_cell`, `sgb25rhd_cell`, TMR
Chip Layout/Package for SEU Tests

Radiation campaign including board design will be performed in September by ARQUIMEA Ingenieria, Madrid
Space projects in SGB25V/SGB25RH

ARQUIMEA (Spain – Prime Contractor) : “EUROPEAN LVDS DRIVER Incl. COLD SPARE CAPABILITY; DEVELOPMENT AND ESCC EVALUATION AND QUALIFICATION ” - ESA Tender AO/1-6922/11/NL/LvH.”

Project Consortium :
Design and Programme Management : ARQUIMEA (Spain)
Technology Provider : IHP (Germany)
Assembly House : Micross (UK)
Test House : Alter Technology Group (Spain)

Full Duration : 30 Months (for Phase I to Phase III)

Objective : Rad-Hard LVDS ICs with the following functions :
• **Dual LVDS Transceiver pair IC** compatible to NS DS90LV049Q Automotive part.
• **4x4 LVDS cross point IC** compatible to TI NS65LVDS125 commercial part.
Space projects in SGB25V/SGB25RH

Space Engineering (Italy): “HIGHLY INTEGRATED BFN USING ON CHIP MULTINODE CONCEPT” - ESA Tender AO/1-5920/08/NL/ST.”

Current SiGe MMIC technology, allows the design of multinode MMICs integrating more than one beam-forming node on the same chip. The technology allows also the integration of mixed analogue/digital functions on the same chip, thus significantly reducing the complexity part count, yield and overall cost of BFNs for both multibeam reconfigurable payload/antennas and for phased array mobile terminals.

Democritus University of Thrace (GREECE): Essential TeleMetry (ETM) support ASIC

Thales Alenia Space (France) partly CNES funded, IHP as subcontractor

Kayser Threde/IHP (Germany): Fractional-N Synthesizer, 12 bit DAC 1.5Gsamples

IHP (Germany): DLR funded, Middleware Switch
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0.13µm BiCMOS - SG13S
## SG13 Process Options

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<td><strong>CMOS</strong></td>
<td>Vdd=1.2 V, Tox=2 nm + Vdd=3.3 V, Tox=7 nm</td>
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</table>
Companies and institutions supporting this initiative

- Kayser Threde
- Jena-Optronik
- Advico GmbH
- IMST GmbH
- Astrium
- Dolphin Integration
- Tesat
# DLR project: Evaluation of a radhard library and ESCC test structures in 0.13µm BiCMOS

## Goals:
- SG13 Technology radiation evaluation for Space applications
- Target RF mixed signal application up to 120 GHz
- Low power digital designs

## Workpackages:
- Mixed Signal BiCMOS DesignKit with radhard digital IP
- Development and radiation test of TCV teststructure
- Development and radiation test of DEC teststructure
General overview project proposal
0.13µm mixed signal technology

- Radhard library is available
- Start October 2012 till December 2014
- Additional ESA funding possible in 2013 for complete evaluation in case of good test results from DLR project
Conclusion

- IHP targets to offer its SiGe BiCMOS technologies as foundry service for Space applications

- Evaluation of 0.25µm BiCMOS technology nearly finalized

- Running Space Projects in 0.25µm BiCMOS

- Radhard and ESCC evaluation for 0.13µm BiCMOS will be started October 2012