MIXED-SIGNAL DESIGN METHODOLOGY USING A PRIORI SINGLE EVENT TRANSIENT RATE ESTIMATES

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Outline

▼ Introduction

▼ Design Flow

▼ Qsim:
  ▼ Determination of Critical Charge

▼ SETsim:
  ▼ Rate vs Deposited Charge

▼ SET Error Rate Estimates
  ▼ Intersection of Critical Charge with Rate vs. Deposited Charge

▼ SET Scorecard:
  ▼ Compiled SET/SEU Error Rates for the Entire Mixed-Signal ASIC

▼ Some Results
  ▼ Laser + Beamline vs SETsim + Qsim

▼ Summary
Introduction

▼ Radiation Performance:
  - Total Ionizing Dose (TID):
    ▼ Must be characterized on test structures
  - Single Event Latch-Up (SEL)
    ▼ Must be characterized on test structures
  - Single Event Upset (SEU)
    ▼ Can be characterized using test chip containing digital cell library elements
  - Single Event Transients (SET)
    ▼ Are different for different analog circuits
    ▼ Can lead to SEU

▼ How to deal with SET error rates?
  ▼ Characterize on unique test chip?
    - One test chip for every ASIC?
  ▼ A Priori SET Rate Estimates
    - Cost effective if the method is reliable
Design Flow
Part 1
Schematic Design
Design Flow

Part 2
Physical Design
Design Flow

Part 3
Final Full-Chip Simulations + Database Prep.

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Design Flow: Part 1 Schematic Design

- Analog Schematic Design/Simulations
  - Qsim Simulations (SETsim w/ Approx. Layout)
    - $Q_{\text{crit}}$ goals met?
      - NO
      - YES
        - NO
        - YES
          - Connect Entire ASIC/Mixed-Mode Sim.

- Digital RTL Design
  - Synthesis Script/Digital Core Synthesis
    - Prelim. SEU Rates Acceptable?
      - NO
      - YES
Design Flow: Part 2 Physical Design

1. Interim Design Review (IDR)
   - Analog Cell Layout
     - SETsim Simulations
       - SET Error Rates met?
         - YES: Connect Entire ASIC/Mixed-Mode Sim.
         - NO: Back Annotation/Static Timing Analysis
   - Final Synthesis/Digital Place & Route
     - SEU Error Rates met?
       - YES: Connect Entire ASIC/Mixed-Mode Sim.
       - NO: Back Annotation/Static Timing Analysis
Design Flow: Part 3

Full ASIC SET/SEU Scorecard

Analog Cell Layout

Final SET/SEU Error Rates OK?

Final Database Review

Pass all DRC, LVS, ERC, SOA?

Tapeout Database to Wafer Foundry

Database Prep.

YES

Critical Design Review (CDR)

YES

END Design Phase/START Prototype

NO

A

NO
Qsim

- Uses double-exponential model for funnel currents
- Total injected charge is the area under the double-exponential curve
- Current source:

\[
I(t) = \begin{cases} 
  y_1 & \text{for } 0 \leq t \leq t_{d1} \\
  y_1 + (y_2 - y_1) \cdot \left(1 - \exp\left(\frac{t - t_{d1}}{\tau_1}\right)\right) & \text{for } t_{d1} \leq t \leq t_{d2} \\
  y_1 + (y_2 - y_1) \cdot \left(1 - \exp\left(\frac{t - t_{d1}}{\tau_1}\right)\right) + (y_1 - y_2) \cdot \left(1 - \exp\left(\frac{t - t_{d2}}{\tau_2}\right)\right) & \text{for } t_{d2} \leq t \leq t_{\text{max}} 
\end{cases}
\]
Qsim

- **SPICE™** based simulation engine
- Qsim parses SPICE netlist to find each unique electrical node
  - If node is not reverse-biased, it is skipped
- Qsim then creates new SPICE netlist containing double-exponential current sources
  - User defines parameters of the current source:
    - $\tau_1$, $\tau_2$, $y_2$
    - $y_1$ based upon bias-point used for simulation
- Qsim batches SPICE simulations
- User inspects output to determine whether SET caused an error
Qsim: Determining Critical Charge, $Q_{crit}$

1. Define Circuit-Under-Test as subcircuit netlist
2. Set parameters in qsim.header file
3. Run Qsim
4. Determine the most sensitive node(s) for defined error condition(s)
5. Increase magnitude of current pulse
6. Run Qsim
7. Apply current pulse to the most sensitive nodes
8. Did error occur?
   - Yes: Calculate charge by integrating the current pulse over time that was applied to the selected node
   - No: End Qsim Simulation

Output of integration = Critical Charge ($Q_{crit}$)
SETsim

▼ Inputs:
- 3-Dimensional Sensitive Regions representing one or more electrical nodes
  ▼ Multiple diffusions of same electrical node
  ▼ Multiple diffusions of two or more different electrical nodes
  ▼ 6-sided prisms with 8 vertices (trapezoidal prisms)
- Particle Radiation Environment
  ▼ No scattering: Flux Density vs. LET
  ▼ Scattering: Flux Density vs E for each ion type in spectrum

▼ Output:
- Rate vs. Deposited Charge for the node in the analog cell being modeled, for the particular environment
SETsim

3-Dimensional Sensitive Regions: Prismatoids

- What is a Prismatoid?
  - Polyhedron with all vertices lying in one of two parallel planes
  - At least two parallel surfaces (surface of silicon and sensitive depth of silicon)
  - Other sides need not be perpendicular to the two parallel surfaces
  - Two parallel sides need not be the same size nor same number of vertices

- SETsim uses any number of 6-sided prismatoids with 8 vertices, 4 in each of the two parallel planes, i.e. trapezoidal prismatoids
  - Prismatoids may abut one another on any face to create arbitrarily complex geometries
Unequal number of vertices in each of the parallel planes

Equal number of vertices in each of the parallel planes.
(4 vertices in each plane = trapezoidal prismatoid)
Abutting Prismatoids: Plan View

Top surface plan view
Abutting Prismatoids: Plan View

Add another trapezoidal prismatoid
Abutting Prismatoids: Plan View

and another....
Abutting Prismatoids: Plan View
Abutting Prismatoids: Plan View
Abutting Prismatoids: Plan View
Abutting Prismatoids: Plan View

Arbitrarily Complex Shapes Can be Modeled
Abutting Prismatoids: Cross-Section View

Effects of varying doping concentration with depth can be modeled.
### Prismatoid Object Properties

**Electrical Node:**
- Index specifying which electrical node is being modeled
- May have multiple prismatoids defining the same electrical node
- May have multiple prismatoids defining different electrical nodes (as in multiple bit upset)

**Material Index:**
- Index specifying material such as Si, SiO₂, Al, W, Cu
- For non-Si materials:
  - Ion Scattered; Ion Energy and LET modified
  - But no charge is collected
- For Si material index:
  - Ion Scattered; Ion Energy and LET modified
  - Charge is collected per electrical node
Multiple Sensitive Regions

Total Path Length: \( \Delta x = \text{Path}_1 + \text{Path}_2 \)

\[ Q_{gen} = \frac{LET_{ion} \cdot \rho_{Si} \cdot \Delta x}{E_c} \]
SETsim Simulation Space

- RPP region enclosing ALL prismatoids constructed
  - This is the “simulation space”
  - Any region between prismatoids is considered Si, but not part of any electrical node
SETsim: Virtual Ion Generation is NOT Monte Carlo

▼ For each face of the RPP

– For each ion type in the spectrum
– For each energy of such ion.....
– For $x = x_{\text{min}}$ to $x_{\text{max}}$ step $\Delta x$
– For $y = y_{\text{min}}$ to $y_{\text{max}}$ step $\Delta y$
– For $\theta = 0^\circ$ to $90^\circ$ step $\Delta \theta$
– For $\phi = 0^\circ$ to $360^\circ$ step $\Delta \phi$
– Create an Ion Object and “shoot” it into the simulation space
– Push Ion a fixed distance.
– Scatter Ion. Calculate new Ion Energy/LET
  ▼ If ion inside prismatoid of Si with nonzero electrical node index: Collect Charge
– Repeat until Ion Energy < 0 .... or until ion has exited simulation space

▼ Next RPP face
Ion Scattering Problem

Ion (after scattering)

Ion (before scattering)

$\phi$ (Zenith): 0° to 180°
$\theta$ (Azimuth): 0° to 360°
Ion Scattering

- Off-line simulations of ion scattering using TRIM
- For a fixed thickness of Si (or SiO₂, Al, etc.), and for a given ion energy, there is a distribution of ion positions at the back of the thin slice of material
- Reduce to Azimuth and Zenith angle distributions
- Azimuth is (not surprisingly) uniformly distributed between 0° and 360°
- Zenith distribution changes with energy and is highly peaked
- About 1k simulations per ion x 80 ions = 80k simulations per material.
Ion Scattering

- Fit the off-line simulation of zenith scattering angle to an appropriate statistical distribution
  - Beta Distribution has upper and lower bound.
  - Scattered zenith angle has fixed upper and lower bound (0°, or no scattering, to 180°, completely back-scattered).

- Beta Distribution: Two parameters, $\alpha$ and $\beta$

$$P(x) = \frac{1}{B(\alpha, \beta)} x^{\alpha-1} (1 - x)^{\beta-1}$$

- Parameters $\alpha$ and $\beta$ related to peak of distribution as follows:

$$x_{\text{max}} = \frac{\alpha - 1}{\alpha + \beta - 2}$$
Fit to Beta Distribution: Fe in Si

Zenith Angle Probability Distribution for 500keV Fe ions traversing 0.1 microns Si

Blue: Simulation Data
Black: Beta Distribution Fit
Linear (or Polynomial) Fit of the $\beta$ parameter of Beta Distribution.
Beta Distribution Parameters vs Ion Energy

Linear (or Polynomial) Fit of the $\beta$ parameter of Beta Distribution.

\[ x_{\text{max}} = \frac{\alpha - 1}{\alpha + \beta - 2} \]
Ion Scattering: Summary

▼ Equations Pre-determined for:
- $\beta$ vs $E$ for each ion type
- $\phi_{max}$ vs $E$ for each ion type
- $\alpha$ of scattering Beta Distribution can then be uniquely determined

▼ Ion Scattering:
- Choose a random number between 0 and 1
  - Azimuth ($\theta$): multiply random number by 360°
- Choose another random number between 0 and 1
  - Zenith ($\phi$): use random number as probability in Inverse Beta Distribution to generate scattered zenith angle.
- This is the only part of simulation that is “Monte Carlo”.
  - If scattering not enabled, then simulation is completely deterministic.
SETsim Output: Rate vs Deposited Charge

rhinv2, Ion Hit Rate vs. Deposited Charge

*SET error rate*

$q_{crit}$
### SET Scorecard Example (Worse Solar Day)

<table>
<thead>
<tr>
<th>Cell Name</th>
<th>Cell Description</th>
<th>Critical Charge (Coulombs)</th>
<th>Worse Solar Day SET/SEU Rate per Cell (#/day)</th>
<th>Instances</th>
<th>Duty Cycle</th>
<th>SET Rate (#/day)</th>
<th>Instances</th>
<th>Duty Cycle</th>
<th>SET Rate (#/day)</th>
<th>Instances</th>
<th>Duty Cycle</th>
<th>SEU Rate (incl. SET) (#/day)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RHAO2222</td>
<td>4-wide 2-2-2-2 inputs AND-OR</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>2.0%</td>
<td>6.40E-08</td>
<td></td>
<td></td>
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<tr>
<td>RHAO21</td>
<td>2-wide 2-1 inputs AND-NOR</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>2.0%</td>
<td>6.40E-08</td>
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<td></td>
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<tr>
<td>RHAO22</td>
<td>2-wide 2-2 inputs AND-NOR</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>2.0%</td>
<td>6.40E-08</td>
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<td></td>
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<tr>
<td>RHBUF1</td>
<td>1x Buffer</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
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<td>6.40E-08</td>
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<tr>
<td>RHBUF2</td>
<td>2x Buffer</td>
<td>1.49E-12</td>
<td>6.95E-09</td>
<td>2.0%</td>
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<td>100.0%</td>
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<td>6.40E-08</td>
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<tr>
<td>RHBUF4</td>
<td>4x Buffer</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
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<td>8.01E-07</td>
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<td>6.40E-08</td>
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<tr>
<td>RHBUF4S</td>
<td>4x Buffer (4x-4x)</td>
<td>2.90E-12</td>
<td>2.30E-12</td>
<td>50</td>
<td>2.0%</td>
<td>2.30E-12</td>
<td>50</td>
<td>100.0%</td>
<td>1.15E-10</td>
<td>2.0%</td>
<td>4.60E-12</td>
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<tr>
<td>RHBUF8</td>
<td>8x Buffer</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>2.0%</td>
<td>6.40E-08</td>
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<td>RHBUF8S</td>
<td>8x Buffer (8x-8x)</td>
<td>5.80E-12</td>
<td>9.34E-14</td>
<td>50</td>
<td>100.0%</td>
<td>4.67E-12</td>
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<td>1.15E-10</td>
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<td>4.60E-12</td>
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<tr>
<td>RHENO</td>
<td>2-wide 2-2-2-inputs OR-NAND-NAND</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>2.0%</td>
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<td>RHHAD1</td>
<td>Half Adder</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
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<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>2.0%</td>
<td>6.40E-08</td>
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<td></td>
</tr>
<tr>
<td>RHINV1</td>
<td>1x Inverter</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>2.0%</td>
<td>6.40E-08</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RHINV2</td>
<td>2x Inverter</td>
<td>1.49E-12</td>
<td>6.95E-09</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>2.0%</td>
<td>6.40E-08</td>
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<tr>
<td>RHOAI211</td>
<td>3-wide, 2-1-1 input OR-NAND</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>2.0%</td>
<td>6.40E-08</td>
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<tr>
<td>RHINOR2</td>
<td>2-input exclusive-NAND</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>2.0%</td>
<td>6.40E-08</td>
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<tr>
<td>RHHOR2</td>
<td>2-input exclusive-OR</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>2.0%</td>
<td>6.40E-08</td>
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</tr>
<tr>
<td>RHSDS2APCM - SEU</td>
<td>Scan D flip-flop, asynch preset/clear</td>
<td>1.50E-12</td>
<td>1.00E-12</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
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<td>1024</td>
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<tr>
<td>RHSDS2APCM - async SET</td>
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<td>1.49E-12</td>
<td>1.00E-12</td>
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<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>1.00E+00</td>
<td>1.00E+00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RHSDS2APCM - output SET</td>
<td></td>
<td>1.49E-12</td>
<td>1.00E-12</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>1.00E+00</td>
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<td>RHSDS1M - SEU</td>
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<td>100.0%</td>
<td>0.00E+00</td>
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<td>1.00E+00</td>
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</tr>
<tr>
<td>RHSDS2M - output SET</td>
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<td>1.49E-12</td>
<td>1.00E-12</td>
<td>100.0%</td>
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<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>1.00E+00</td>
<td>1.00E+00</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Subtotals:**

- **Critical Charge (Coulombs):**
  - Subtotal: 1.39E-09

- **Worse Solar Day SET/SEU Rate per Cell (#/day):**
  - Subtotal: 8.01E-07

- **SEU Rate (incl. SET) (#/day):**
  - Subtotal: 2.31E-06
## SET Scorecard Example (Worse Solar Day)

### Critical Charge

<table>
<thead>
<tr>
<th>Cell Name</th>
<th>Cell Description</th>
<th>Critical Charge (Coulombs)</th>
<th>SET/SEU Rate per Cell (#/day)</th>
<th>Instances</th>
<th>Duty Cycle</th>
<th>SET Rate (#/day)</th>
<th>Instances</th>
<th>Duty Cycle</th>
<th>SET Rate (#/day)</th>
<th>Subtotals</th>
</tr>
</thead>
<tbody>
<tr>
<td>RHAO2222</td>
<td>4-wide 2-2-2-2 inputs AND-OR</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>6.40E-08</td>
<td>1.39E-09</td>
</tr>
<tr>
<td>RHAO21</td>
<td>2-wide 2-1 inputs AND-NOR</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>6.40E-08</td>
<td>1.39E-09</td>
</tr>
<tr>
<td>RHAO22</td>
<td>2-wide 2-2 inputs AND-NOR</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>6.40E-08</td>
<td>1.39E-09</td>
</tr>
<tr>
<td>RHBUF1</td>
<td>1x Buffer</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>6.40E-08</td>
<td>1.39E-09</td>
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<tr>
<td>RHBUF2</td>
<td>2x Buffer</td>
<td>1.49E-12</td>
<td>6.95E-09</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>6.40E-08</td>
<td>1.39E-09</td>
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<tr>
<td>RHBUF4</td>
<td>4x Buffer</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>6.40E-08</td>
<td>1.39E-09</td>
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<tr>
<td>RHBUF4S</td>
<td>4x Buffer (4x-4x)</td>
<td>5.80E-12</td>
<td>9.34E-14</td>
<td>50 2.0%</td>
<td>2.30E-12</td>
<td>100.0%</td>
<td>1.15E-10</td>
<td>100%</td>
<td>4.60E-12</td>
<td>2.31E-06</td>
</tr>
<tr>
<td>RHBUF8</td>
<td>8x Buffer</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>6.40E-08</td>
<td>1.39E-09</td>
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<tr>
<td>RHBUF8S</td>
<td>8x Buffer (8x-8x)</td>
<td>5.80E-12</td>
<td>9.34E-14</td>
<td>50 100.0%</td>
<td>4.67E-12</td>
<td>100.0%</td>
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<td>4.60E-12</td>
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<td>RENO</td>
<td>2-wide 2-2-2-inputs OR-NAND-NAND</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>6.40E-08</td>
<td>1.39E-09</td>
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<tr>
<td>RHHAD1</td>
<td>Half Adder</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>6.40E-08</td>
<td>1.39E-09</td>
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<tr>
<td>RHINV1</td>
<td>1x Inverter</td>
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<td>3.20E-08</td>
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<td>0.00E+00</td>
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<td>100.0%</td>
<td>0.00E+00</td>
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<td>6.40E-08</td>
<td>1.39E-09</td>
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</table>

### Worse Solar Day

<table>
<thead>
<tr>
<th>Cell Name</th>
<th>Cell Description</th>
<th>Critical Charge (Coulombs)</th>
<th>SET/SEU Rate per Cell (#/day)</th>
<th>Instances</th>
<th>Duty Cycle</th>
<th>SET Rate (#/day)</th>
<th>Instances</th>
<th>Duty Cycle</th>
<th>SET Rate (#/day)</th>
<th>Subtotals</th>
</tr>
</thead>
<tbody>
<tr>
<td>RHSDS2AP</td>
<td>Scan D flip-flop, no preset/clear</td>
<td>1.50E-12</td>
<td>1.00E-12</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>6.40E-08</td>
<td>1.39E-09</td>
</tr>
<tr>
<td>RHSDS2AP</td>
<td>&quot;&quot;</td>
<td>1.49E-12</td>
<td>1.00E-12</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100.0%</td>
<td>0.00E+00</td>
<td>100%</td>
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<td>1.39E-09</td>
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### Reset-Network

<table>
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<th>SET/SEU Rate per Cell (#/day)</th>
<th>Instances</th>
<th>Duty Cycle</th>
<th>SET Rate (#/day)</th>
<th>Instances</th>
<th>Duty Cycle</th>
<th>SET Rate (#/day)</th>
<th>Subtotals</th>
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<tbody>
<tr>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>6.40E-08</td>
<td>1.39E-09</td>
</tr>
<tr>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>6.40E-08</td>
<td>1.39E-09</td>
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### Clock-Network

<table>
<thead>
<tr>
<th>Critical Charge (Coulombs)</th>
<th>SET/SEU Rate per Cell (#/day)</th>
<th>Instances</th>
<th>Duty Cycle</th>
<th>SET Rate (#/day)</th>
<th>Instances</th>
<th>Duty Cycle</th>
<th>SET Rate (#/day)</th>
<th>Subtotals</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>6.40E-08</td>
<td>1.39E-09</td>
</tr>
<tr>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>0.00E+00</td>
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<td>1.39E-09</td>
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### Synchronous-Logic

<table>
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<th>Instances</th>
<th>Duty Cycle</th>
<th>SET Rate (#/day)</th>
<th>Instances</th>
<th>Duty Cycle</th>
<th>SET Rate (#/day)</th>
<th>Subtotals</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>6.40E-08</td>
<td>1.39E-09</td>
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</tbody>
</table>
## SET Scorecard Example (Worse Solar Day)

| Cell Name   | Cell Description                  | Critical Charge (Coulombs) | SET/SEU Rate per Cell (#/day) | Instances | Duty Cycle | SET Rate (#/day) | Instances | Duty Cycle | SET Rate (#/day) | Instances | Duty Cycle | SET Rate (#/day) | Instances | Duty Cycle | SET Rate (#/day) | Instances | Duty Cycle | SET Rate (#/day) | Instances | Duty Cycle | SET Rate (#/day) |
|-------------|-----------------------------------|----------------------------|--------------------------------|-----------|------------|------------------|-----------|------------|------------------|-----------|------------|------------------|-----------|------------|------------------|-----------|------------|------------------|-----------|------------|------------------|-----------|------------|------------------|-----------|------------|------------------|-----------|------------|
| RHAO222     | 4-wide 2-2-2-2 inputs AND-OR      | 7.70E-13                   | 3.20E-08                       | 2.0%      | 0.00E+00   | 100.0%           | 0.00E+00   | 100%       | 2.0%             | 6.40E-08  |
| RHAO21      | 2-wide 2-1 inputs AND-NOR         | 7.70E-13                   | 3.20E-08                       | 2.0%      | 0.00E+00   | 100.0%           | 0.00E+00   | 100%       | 2.0%             | 6.40E-08  |
| RHAO22      | 2-wide 2-2 inputs AND-NOR         | 7.70E-13                   | 3.20E-08                       | 2.0%      | 0.00E+00   | 100.0%           | 0.00E+00   | 100%       | 2.0%             | 3.20E-08  |
| RHBUF1      | 1x Buffer                         | 7.70E-13                   | 3.20E-08                       | 2.0%      | 0.00E+00   | 100.0%           | 0.00E+00   | 100%       | 2.0%             | 6.40E-08  |
| RHBUF2      | 2x Buffer                         | 1.49E-12                   | 6.95E-09                       | 2.0%      | 0.00E+00   | 100.0%           | 0.00E+00   | 100%       | 2.0%             | 6.40E-08  |
| RHBUF4      | 4x Buffer                         | 7.70E-13                   | 3.20E-08                       | 2.0%      | 0.00E+00   | 25               | 0.00E+00   | 100%       | 2.0%             | 6.01E-07  |
| RHBUF4S     | 4x Buffer (4x-4x)                 | 2.90E-12                   | 2.30E-12                       | 50        | 2.0%       | 2.30E-12         | 50         | 100%       | 1.15E-10          | 4.60E-12  |
| RHBUF8      | 8x Buffer                         | 7.70E-13                   | 3.20E-08                       | 2.0%      | 0.00E+00   | 100.0%           | 0.00E+00   | 100%       | 2.0%             | 6.40E-08  |
| RHBUF8S     | 8x Buffer (8x-8x)                 | 5.80E-12                   | 9.34E-14                       | 50        | 100%       | 4.67E-12         | 100%       | 1.87E-13 |
| RENO        | 2-wide 2-2-2 inputs OR-NAND-NAND  | 7.70E-13                   | 3.20E-08                       | 2.0%      | 0.00E+00   | 100.0%           | 0.00E+00   | 100%       | 2.0%             | 6.40E-08  |
| RHHAO1      | Half Adder                        | 7.70E-13                   | 3.20E-08                       | 2.0%      | 0.00E+00   | 100.0%           | 0.00E+00   | 100%       | 2.0%             | 6.40E-08  |
| RHINV1      | 1x Inverter                       | 7.70E-13                   | 3.20E-08                       | 2.0%      | 0.00E+00   | 100.0%           | 0.00E+00   | 100%       | 2.0%             | 6.40E-08  |
| RHINV2      | 2x Inverter                       | 1.49E-12                   | 6.95E-09                       | 2.0%      | 0.00E+00   | 100.0%           | 0.00E+00   | 100%       | 2.0%             | 1.39E-08  |

**Worse Solar Day**

- Critical Charge: 1.39E-09
- SET/SEU Rate: 8.01E-07
- Subtotal SET Rate: 2.31E-06

*Inadvertent RESET asserted.*
## SET Scorecard Example (Worse Solar Day)

<table>
<thead>
<tr>
<th>Cell Name</th>
<th>Cell Description</th>
<th>Critical Charge (Coulombs)</th>
<th>Worse Solar Day</th>
<th>Reset-Network</th>
<th>Clock-Network</th>
<th>Synchronous-Logic</th>
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<tbody>
<tr>
<td></td>
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<td></td>
<td>SET/SEU Rate per Cell (#/day)</td>
<td>Instances</td>
<td>Duty Cycle</td>
<td>SET Rate (#/day)</td>
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<tr>
<td>RHAO21</td>
<td>2-wide 2-1 inputs AND-NOR</td>
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<td>3.20E-08</td>
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<tr>
<td>RHAO22</td>
<td>2-wide 2-2 inputs AND-NOR</td>
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<tr>
<td>RHBUF1</td>
<td>1x Buffer</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
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</tr>
<tr>
<td>RHBUF2</td>
<td>2x Buffer</td>
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<tr>
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<td>4x Buffer</td>
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<tr>
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<td>4x Buffer (4x-4x)</td>
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<td>2.0%</td>
<td>2.30E-12</td>
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<td>8x Buffer</td>
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<td>3.20E-08</td>
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<tr>
<td>RHBUF8S</td>
<td>8x Buffer (8x-8x)</td>
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<td>9.34E-14</td>
<td>50</td>
<td>100.0%</td>
<td>4.67E-12</td>
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<tr>
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<td>2-wide 2-2-2-inputs OR-NAND-NAND</td>
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<td>3.20E-08</td>
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<tr>
<td>RHADD1</td>
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<tr>
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<td>1x Inverter</td>
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<td>3.20E-08</td>
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<tr>
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<td>3.20E-08</td>
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<tr>
<td>RHSDS2APCM - SEU</td>
<td>Scan D flip-flop, async preset/clear</td>
<td>1.50E-12</td>
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<tr>
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<tr>
<td>RHSDS2M - output SET</td>
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<td>8.01E-07</td>
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</tr>
</tbody>
</table>

**SEFI**
## SET Scorecard Example (Worse Solar Day)

<table>
<thead>
<tr>
<th>Cell Name</th>
<th>Cell Description</th>
<th>Critical Charge (Coulombs)</th>
<th>SET/SEU Rate per Cell (#/day)</th>
<th>Duty Cycle</th>
<th>Instances</th>
<th>SET Rate (#/day)</th>
<th>Duty Cycle</th>
<th>Instances</th>
<th>SET Rate (#/day)</th>
<th>Duty Cycle</th>
<th>Instances</th>
<th>SEU Rate (incl. SET) (#/day)</th>
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<tbody>
<tr>
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<td>4-wide 2-2-2-2 inputs AND-OR</td>
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<td>3.20E-08</td>
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<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
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<td>6.40E-08</td>
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<tr>
<td>RHAOI21</td>
<td>2-wide 2-1 inputs AND-NOR</td>
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<tr>
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<td>RHBUF2</td>
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</tr>
<tr>
<td>RHBUF4</td>
<td>4x Buffer</td>
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<tr>
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<tr>
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<td>3.20E-08</td>
<td>2.0%</td>
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<td>0%</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>2.0%</td>
<td>6.40E-08</td>
</tr>
<tr>
<td>RHINV2</td>
<td>2x Inverter</td>
<td>1.49E-12</td>
<td>6.95E-09</td>
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<td>0%</td>
<td>0.00E+00</td>
<td>0%</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>2.0%</td>
<td>1.39E-08</td>
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<tr>
<td>RHAO2211</td>
<td>3-wide, 2-1-1 input OR-NAND</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>2.0%</td>
<td>6.40E-08</td>
</tr>
<tr>
<td>RHXNOR2</td>
<td>2-input exclusive-NOR</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>2.0%</td>
<td>6.40E-08</td>
</tr>
<tr>
<td>RHXOR2</td>
<td>2-input exclusive-OR</td>
<td>7.70E-13</td>
<td>3.20E-08</td>
<td>2.0%</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>100%</td>
<td>0.00E+00</td>
<td>100%</td>
<td>2.0%</td>
<td>6.40E-08</td>
</tr>
<tr>
<td>RHSDS2APCM - SEU</td>
<td>Scan flip-flop, asynch preset/clear</td>
<td>1.50E-12</td>
<td>1.00E-12</td>
<td>100%</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
<td>100%</td>
<td>1024</td>
<td>1.02E-09</td>
<td>100%</td>
<td>2.0%</td>
<td>1.02E-09</td>
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<tr>
<td>RHSDS2APCM - async SET</td>
<td>&quot;&quot;</td>
<td>1.49E-12</td>
<td>1.00E-12</td>
<td>100%</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
<td>100%</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
<td>1.0%</td>
<td>6.40E-08</td>
</tr>
<tr>
<td>RHSDS2APCM - output SET</td>
<td>&quot;&quot;</td>
<td>1.49E-12</td>
<td>1.00E-12</td>
<td>100%</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
<td>100%</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
<td>1.0%</td>
<td>6.40E-08</td>
</tr>
<tr>
<td>RHSDS2M - SEU</td>
<td>Scan flip-flop, no preset/clear</td>
<td>1.50E-12</td>
<td>1.00E-12</td>
<td>100%</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
<td>100%</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
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<td>1.0%</td>
<td>6.40E-08</td>
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<tr>
<td>RHSDS2M - output SET</td>
<td>&quot;&quot;</td>
<td>1.49E-12</td>
<td>1.00E-12</td>
<td>100%</td>
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<td>0.00E+00</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
<td>1.0%</td>
<td>6.40E-08</td>
</tr>
</tbody>
</table>

Subtotals: 1.39E-09 8.01E-07 2.31E-06

---

**SEU**
Some Results: Qsim vs Laser Irradiation

(a) Laser Irradiation of LVDS Driver  
(Laser Equivalent LET = 330 MeV cm²/mg)

(b) Qsim Simulation of same LVDS Driver  
showing same error. Magnitude of error ~same as oscilloscope trace.
SETsim Results:

Digital SEU, YB03 ADC ASIC

Inverter chain feeding an SEU-hardened SDFF

(Weibull fit is an "aid to the eye". Not enough data for meaningful shape and width parameter extraction.)
SETsim Results:

Inverter chain feeding an SEU-hardened SDFF

SETsim predicted on-set LET = 60 MeV cm²/mg

Digital SEU, YB03 ADC ASIC

No upset observed at LET=91.4

(Weibull fit is an "aid to the eye". Not enough data for meaningful shape and width parameter extraction.)
16-bit 40MSps Pipeline ADC
16-bit 40MSps Pipeline ADC

Converted Output deviation from normal noise level should last only 2 clock cycles
ASETs in 16-bit 40MSPS Pipeline ADC

Goal: No SETs lasting > 2 sample clocks for LET < 40 MeV cm²/mg
Result: ASET > 2 sample clocks on-set LET ~48 MeV cm²/mg
SETsim Results: 4-Channel Voltage Supervisor
SETsim Results: 4-Channel Voltage Supervisor

Inputs set to 50mV above comparator trip point
SETsim Results: 4-Channel Voltage Supervisor

Outputs monitored for SET (either glitches or change in state)
4-Channel Voltage Supervisor Results

▼ Bias Conditions:
  - 4 Inputs biased at 50mV above comparator trip point
  - VDD=3.0V, 2.7V

▼ Beam:
  - Xe, 60° angle of incidence (effective LET 112 MeV cm²/mg)
  - 1E7 ions/cm²

▼ SETsim Prediction:
  - SET on-set LET ~80 MeV cm²/mg

▼ Results:
  - No SETs observed at 112 MeV cm²/mg at either VDD = 3.0V or VDD = 2.7V
SETsim vs CREME96

Table I: Comparison of Predicted Error Rates: SETsim vs. CREME96
(Sensitive Volume = 1 x 5 x Depth μm)

<table>
<thead>
<tr>
<th>Depth(μm)</th>
<th>Environment</th>
<th>Error Rate from SETsim (errors/day)</th>
<th>Error Rate from CREME96 using HUP (errors/day)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Worse Solar Day</td>
<td>16.5E-8</td>
<td>7.4E-8</td>
</tr>
<tr>
<td>1.4</td>
<td>Worse Solar day</td>
<td>2.54E-7</td>
<td>1.5E-7</td>
</tr>
<tr>
<td>1.0</td>
<td>Solar Min/GCR Max</td>
<td>15.5E-11</td>
<td>6.84E-11</td>
</tr>
<tr>
<td>1.4</td>
<td>Solar Min/GCR Max</td>
<td>2.38E-10</td>
<td>1.48E-10</td>
</tr>
</tbody>
</table>

SETsim error rates ~60% to ~120% higher than CREME96:

SETsim integrates over $2\pi$ sterradians over each of the six faces of simulation region.

This emphasizes longest path lengths.
Summary

▼ A Priori SET Estimates made during Mixed-Signal ASIC design using Qsim and SETsim tools
  – Qsim used to determine Critical Charge
  – SETsim used to determine rate vs Deposited Charge

▼ Intersection of $Q_{crit}$ (Qsim) with Rate vs Charge curve (SETsim) gives SET error rate for the cell

▼ SET Scorecard used to compile SET results for entire Mixed-Signal ASIC
  – Error rates categorized: SEU, SET, SEFI, etc.

▼ Results indicate beam-line and laser measured error rates are lower than those predicted by SETsim.
  – Meeting error rate goals in ASIC design: high confidence that Mixed-Signal ASIC beam-line results will be within specification
Dank U!
Thank you!
Danke!
Merci!
Grazie!
Gracias!
Tack!
Ευχαριστούμε!
תודה!