MIXED-SIGNAL DESIGN METHODOLOGY USING A PRIORI SINGLE EVENT TRANSIENT RATE ESTIMATES

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INTRODUCTION

Mixed-signal integrated circuits used in space applications are exposed to solar particles and galactic cosmic rays (GCR). For earth orbit environments, the energy and composition of the particle radiation depends primarily upon the orbital inclination and the orbit altitude. However, due to the solar cycle and its interaction with the GCR, there is also a time dependence to the intensity and energy composition of the particle radiation [1]. Both forms of particle radiation can cause deleterious effects in microelectronics, including single event latch-up (SEL), single event upsets (SEUs), single event transients (SETs), or single event effects (SEE), some of which are irreversible and destructive to the electronics.

SET and SEU rates are typically determined from particle accelerator experiments on test structures containing analog and digital cells that will be incorporated into a new Application Specific Integrated Circuit (ASIC) design. The cost and schedule impact of doing this for each cell in a full-custom, mixed-signal ASIC makes this approach impractical. Furthermore, the solid angle available for particle accelerator experiments is limited by both the available beam energies and the thickness of the layers of metal and dielectric material over-lying the sensitive device regions [2]. Whereas the particle energies in space environments make it possible to have heavy ion strikes that deposit charge in multiple sensitive regions, beam line experiments are often limited to probing only a single sensitive region at a time. While radiation testing of the prototype mixed-signal ASIC is certainly required, a cost-effective means of making a priori estimates of SET/SEU rates is required to avoid costly re-designs of full-custom mixed-signal ASICs. To calculate such error rates, including the effects of angled ion strikes, fully three-dimensional (3-D) simulations are needed.

DESIGN FLOW

Fig. 1 shows a typical design-flow for a full-custom, mixed-signal ASIC. In the first phase, the detailed specification of the ASIC is finalized, culminating in a preliminary design review (PDR). The detailed specification contains all of the electrical and functional information necessary for a behavioral model of the entire ASIC to be created. In the next phase, analog functions in the ASIC are designed schematically using primitive devices available in the mixed-signal library, such as transistors, resistors, capacitors, and varactor. (Typically, entire schematics are re-used or adapted from an existing library of analog cells.) In parallel with this effort, the digital portion of the ASIC is designed using a behavioral language such as VHDL or Verilog. Once the digital design has been completed and verified, it can be synthesized to the digital library elements. This gate-level netlist can then be connected to the analog schematic, rendering a complete schematic-level description of the ASIC. At this point, the complete ASIC may be simulated using a mixed-mode simulation tool such as Mentor Graphics ADMS [3]. Upon successful completion of full chip simulations over process, temperature, voltage, and total ionizing dose, an interim design review (IDR) is held. At this point, there is enough simulation data to confirm that the design goals of the ASIC have been achieved. In the final design stage, the detailed analog schematic is implemented as a detailed physical design (i.e. layout). The digital netlist is placed and routed, and detailed static timing simulations are performed, now using the extracted parasitic

capacitances and resistances due to the layout of the cells and the metal wire interconnections. Likewise, the analog schematic must be re-simulated with the parasitic capacitances and resistances of the detailed layout of such analog cells, including metal wiring. Lastly, the full-chip simulation is repeated using the schematics which include the parasitics. A final critical design review (CDR) is held to review the full-chip simulation results to verify compliance with the ASIC design goals. Upon successful completion of the CDR, the GDSII tooling database for the mixed-signal ASIC is prepared, and run through rigorous design rule checking (DRCs) as well as checks to ensure that the physical layout of the design conforms with the schematic, or layout vs. schematic (LVS) checks, electrical rule checks (ERC) and safe operating area (SOA) checks to make sure that foundry electrical rules and reliability rules developed by Aeroflex, respectively, have been obeyed. Upon successful database integrity checking, the design database, usually in a format called GDSII or GDS2, is transmitted to the wafer foundry so that design masks may be made. After such mask tooling has been delivered to the wafer foundry, a prototype lot of mixed-signal ASIC wafers may be fabricated.

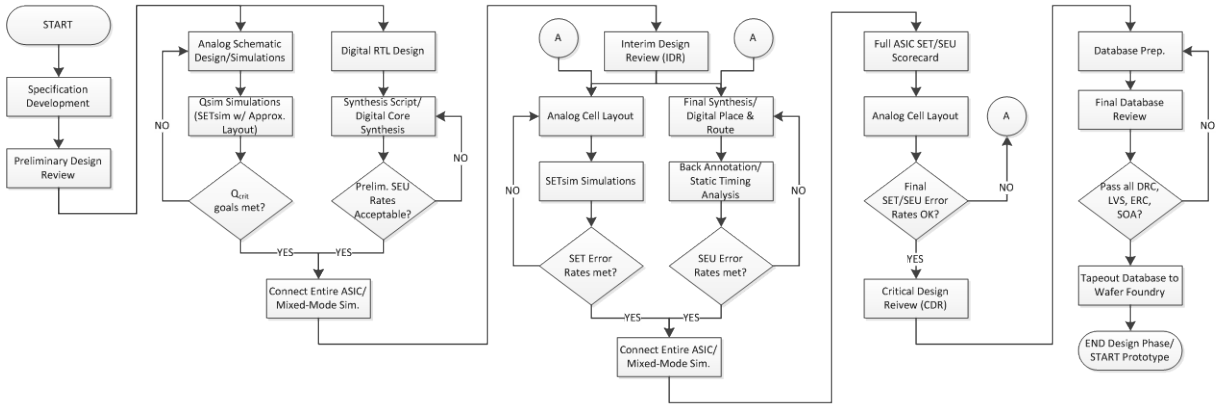

Figure 1: Mixed-Signal Design Flow

Qsim: Determination of Critical Charge, Q_{crit}

It is very important to understand the susceptibility of the design to SEE during the schematic design stage, because often times the best mitigation of SEE in mixed-signal circuits is to modify/improve the architecture of the design. To that end, we have developed an optimization module called Qsim, using SPICE as the simulation engine. This tool uses the double-exponential model for funnel charge currents, where the total charge is the area under the double-exponential curve. This approach, for first order approximation of deposited charge using SPICE simulations, has been proved as an adequate representation of SETs [4-6]. The typical profile for a double exponential current source shown in Fig. 2 agrees well with the measured charge collection response of a 1 Ohm-cm silicon diode biased at 25V irradiated by different ions [7].

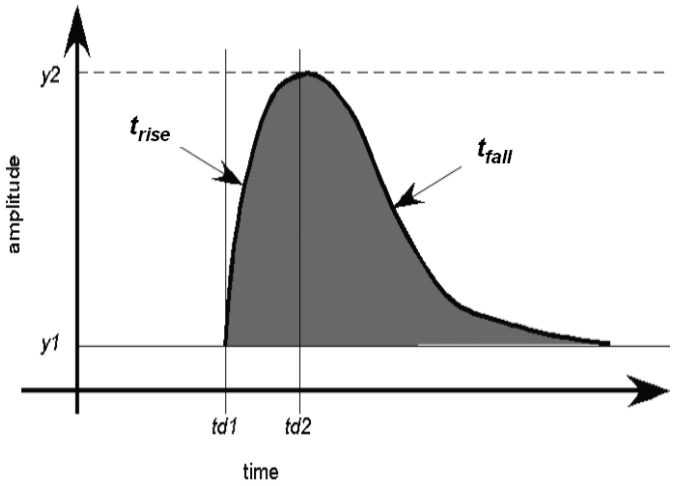

Figure 2. Typical profile for the double-exponential current source used for the single-event source.

The current source used for the SPICE simulations is defined in equation (1) as follows:

$$I(t)=\begin{cases} y_1 \quad \text{for} \quad 0 \le t \le t_{d1} \\ y_1+(y_2-y_1)\cdot\left(1-\exp\left(\dfrac{t-t_{d1}}{\tau_1}\right)\right) \quad \text{for} \quad t_{d1} \le t \le t_{d2} \\ y_1+(y_2-y_1)\cdot\left(1-\exp\left(\dfrac{t-t_{d1}}{\tau_1}\right)\right)+(y_1-y_2)\cdot\left(1-\exp\left(\dfrac{t-t_{d2}}{\tau_2}\right)\right) \quad \text{for } t_{d2} \le t \le t_{\max} \end{cases} \tag{1}$$

where the current at time, t, is $I(t)$, τ_1 represents the rise time of the double exponential, which models the "prompt" charge collected over a very short period of time, τ_2 represents the fall time of the double exponential, which models the charge collected due to funneling (i.e. diffusion), y_2 - y_1 represents the amplitude of the current pulse, t_{max} is the maximum simulation time, and the pulse duration is $t_{d2} - t_{d1}$ occurring at simulation time $t = t_{d1}$ [7]. The parameters τ_1 and τ_2 are provided by the user, whereas y_2 - y_1 is calculated based upon the timing information of the profile.

Qsim operates by parsing the SPICE compatible netlist of the electrical design, finding each of the CMOS transistors in the netlist. The device is logged and parsed for nodal and parametric information such as transistor width, length, and number of drain/source fingers. Using the nodal information, Qsim determines whether the source and/or drain of each transistor is connected to the bulk node. If this is true, Qsim will not inject current into that particular circuit node. This is based upon the assumption that a node susceptible to SET must be reversed biased.

A typical simulation flow for Qsim is shown in Fig. 3. Qsim accepts the netlist that includes the circuit for simulation. Qsim also includes user-defined information that provides the magnitude, rise, and fall times for the double-exponential single-event current. By inspecting the original electrical design netlist, Qsim determines which reverse biased p-n junctions of the CMOS transistors should be included in the SPICE netlist for simulation. Qsim then creates a SPICE compatible netlist with the single-event current source(s) included for SPICE based simulation.

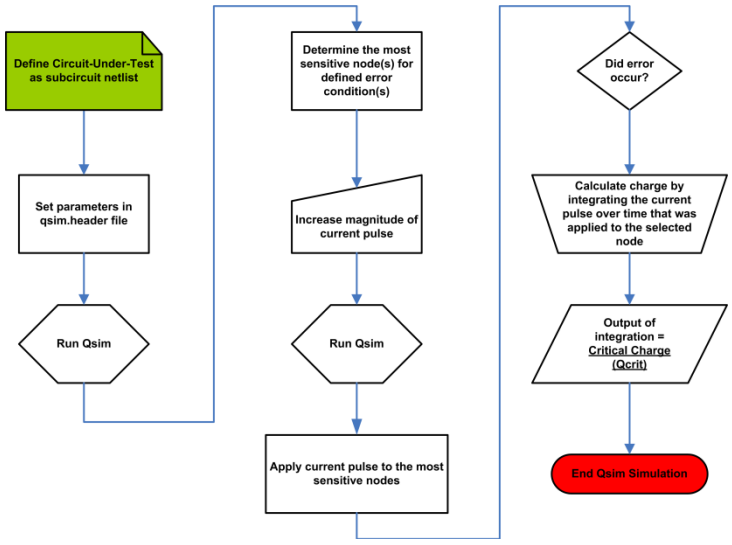

Figure 3: Typical Qsim flow for determining critical charge of a cell.

Qsim creates single-event current sources that are the same for each reverse biased p-n junction included in the simulation, therefore each p-n junction simulated receives an equivalent charge, which is calculated by integrating the double-exponential current profile over time. This allows for easy identification of the sensitive junctions. Once the sensitive node(s) have been identified, further SPICE simulations are performed using very low charges causing no transient errors or upsets. Simulations continue with increasing amounts of injected charge until transient errors and/or

upsets are seen on one of more of the nodes. The critical charge is then chosen as the lowest injected charge applied to a p-n junction that causes the first error/upset. This procedure is continued until either all nodes have exhibited errors/upsets, or until a value of injected charge is reached that has been pre-determined (based upon experience) to be so large that any errors associated with this value of charge or greater are deemed to be of such a low rate that their omission does not appreciably affect the overall error rate estimates for the ASIC.

SETsim: Determination of Error Rate

Having determined Q_{crit} for a sensitive node, the designer must be able to determine the error rate for that critical charge. This depends upon the particular environment, and the particular layout of the node. Charge will be generated in silicon by a heavy according to equation (2) as follows:

$$Q_{gen} = \frac{LET_{ion} \cdot \rho_{Si} \cdot \Delta x}{E_c} \tag{2}$$

where Q_{gen} is the charge generated in silicon due to a heavy ion with linear energy transfer, LET_{ion}, ρ_{Si} is the density of silicon, Δx is the path length traveled by the ion through the sensitive region, and E_c is the energy required to produce one electron-hole pair in silicon. For many years, the sensitive regions in integrated circuits have been modeled as rectangular parallelepipeds (RPP). Since the heavy ions from the GCR strike an integrated circuit from all directions, there will be many possible path lengths through the RPP. Some of these will be short, such that $Q_{gen} < Q_{crit}$. In these cases, the ion will not cause an error. However, other paths through the RPP will be long enough and/or the LET of the ion large enough such that $Q_{gen} > Q_{crit}$. In these cases an error will occur. This method of determining the chord-length distribution that will cause $Q_{gen} < Q_{crit}$, is called the RPP method [8-10].

We have developed a simulation program called SETsim that provides an alternative method for determining the error rate. The sensitive regions are modeled as six-sided solid prismatoids. The two parallel surfaces of each prismatoid are parallel to the surface of the silicon die being modeled. The remaining four surfaces need not be parallel to each other. By using prismatoids, sensitive regions that vary with depth may be modeled. Multiple, abutting prismatoids can be used to model a single sensitive region. Curved or bent regions can be constructed through the use of multiple, abutting, trapezoidal prismatoids as shown in Fig. 4. Deep sensitive regions whose width vary with depth may be modeled by abutting the parallel surfaces of two or more prismatoids.

In addition to eight vertices, each such prismatoid has two associated indices: one designating the electrical node, and one designating the material associated with the region. Multiple sensitive regions having a silicon material index that represent the same electrical node are modeled by giving the same electrical node index to multiple prismatoids. When SETsim in run in a mode where ion scattering is taken into account, then for materials other than silicon, the electrical node is ignored, and such regions are considered to be shielding material. Multiple sensitive regions representing multiple electrical nodes are modeled by giving different electrical node indices to the prismatoids associated with each electrical node. Overlying structures (e.g. inter-level dielectric regions, tungsten contacts, etc.) may optionally be included, where each such shielding prismatoid has an associated material index other than silicon. Currently, a limited number of microelectronic materials of interest are supported: silicon, silicon dioxide, aluminum, and, tungsten. When run in a mode where ion scattering is not considered, prismatoids with material indices other than silicon are not considered in the simulation.

The SETsim program, written in the C^{++} programming language, reads a geometry input file containing the coordinates of the eight vertices of each six-sided prismatoid along with electrical node and material indices. A data object is instantiated for each prismatoid, where the vertices of the prismatoid are stored as properties of the data object. SETsim then calculates the extent of the minimum RPP that contains all such data objects. This RPP becomes the simulation region. Any region within the simulation region but outside of all prismatoids that were enumerated in the geometry input file is considered to have a silicon material index, but be inactive, i.e. does not belong to any electrical node and therefore does not accumulate charge.

The second input file to the SETsim program is a file containing information on the radiation environment. The environment file contains a list of energies and ion flux densities associated with each energy for each ion in the radiation environment. Alternatively, SETsim can use an environment file containing flux density as a function of LET. In this case, the optional ion scattering routine may not be used, since the values of LET are not associated with a particular ion.

A diagram of the six-sided RPP representing the extent of the simulation region, and its rectangular coordinate system are shown in fig. 4. Each face of the top surface of the simulation region is broken up into smaller regions of area $\Delta x * \Delta y$, where $\Delta x = \Delta y$. For each such surface region, a spherical coordinate system centered on this surface region located at position (x,y) is used to generate the incoming direction of virtual ion strikes, where the azimuth angle

variable is θ and the zenith angle is ϕ as shown in fig. 4. For each entry in the environment file, multiple virtual ion objects are created with azimuth angle between 0 and 360 degrees in increments of $\Delta\theta$, and zenith angles between 0 and 90 degrees in increments of $\Delta\phi$. The values of Δx and Δy are typically 0.02 to 0.2 microns, depending upon the extent of the simulation region, while $\Delta\theta$ and $\Delta\phi$ may be a few degrees to 10 degrees, but always a value such that a zenith angle of 90 degrees and an azimuth angle of 360 degrees will always be included in the simulation. For each virtual ion, SETsim pushes the ion a fixed distance, calculates the deposited charge according to equation (2), optionally scatters the ion such that after each step, there are new zenith and azimuth angles associated with the ion, decrements the energy of the ion, and then determines the new LET of the ion based upon piece-wise curve fits of the LET vs energy data for that particular ion type. The entire process is repeated for each of the other 5 surfaces of the simulation region.

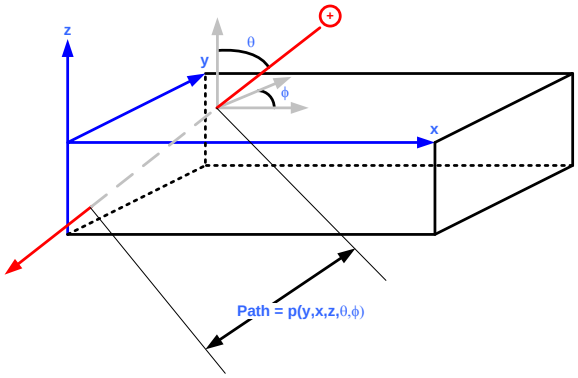

Figure 4: Diagram of the simulation region used in SETsim. The RPP contains all the prismatoids representing sensitive regions or shielding regions. Shown are the rectangular coordinates (*x, y, z*), azimuth angle (θ), zenith angle (ϕ), and ion track.

There is some "double counting" that occurs at the edges of the simulation region, e.g. a zenith angle of 90 degrees on the edge of the "top" face of the simulation region corresponds to a zenith angle of 0 degrees on the "side" face of the simulation region that shares that edge. This double counting further emphasizes the longest paths (depending upon the two faces and adjoining edge involved), which provides a little more margin in the error rate output of SETsim, which is taken to be an upper limit to the error rate for a given cell and environment. Table I lists the error rates determined from SETsim compared to CREME96 (HUP) for a 5 micron x 1.0 micron sensitive region with varying depths of 1 and 1.4 microns for two different orbital environments, where the critical charge, Q_{crit}, has been arbitrarily set to 1pC. As can be seen, SETsim consistently over-predicts the error rate compared to CREME96. This is acceptable since the goal of SETsim is to provide a conservative upper bound to the error rate, ensuring that longest path lengths are always included in the calculation.

Table I: Comparison of Predicted Error Rates: SETsim vs. CREME96

Depth(μm)	Environment	Error Rate from SETsim (errors/day)	Error Rate from CREME96 using HUP (errors/day)
1.0	Worse Solar Day	16.5E-8	7.4E-8
1.4	Worse Solar day	2.54E-7	1.5E-7
1.0	Solar Min/GCR Max	15.5E-11	6.84E-11
1.4	Solar Min/GCR Max	2.38E-10	1.48E-10

Optional Method for Scattering Ions

Off-line simulations of energetic ion interactions with the various materials of interest were performed using SRIM2006[11]. For example, SRIM2006 was used to simulate 10,000 energetic iron ions impinging upon a thin slab (e.g. 0.1 micron) of silicon. For each iron ion that is transmitted through the slab, the SRIM simulator records the ion's position at the back surface of the slab, and its direction. The ion's exit position may be expressed in polar coordinates, where ρ is the minimum distance from the line that represents the ion's path through the region had it not been scattered, and the azimuth angle θ the angle with respect to an arbitrary axis perpendicular to the undisturbed line of flight of the ion. As expected, the azimuth angle is uniformly distributed. The radial distribution of the ion may be transformed into a distribution of zenith angles (switching coordinate system from polar to spherical), such that the net scattering of the

ion through the thin slab is considered to be a single scattering event causing the ion to deviate from its original path by zenith angle $\Delta\tilde{\phi}$. Fig. 5 shows such a distribution of $\Delta\phi$ for iron ions with initial energy of 500 keV after traversing 0.1 microns of silicon. The domain of the scattering angle probability distribution function is 0 to 180 degrees. Therefore, the probability distribution should follow some form of a beta distribution [12]. The beta distribution may be expressed as follows:

$$P(x) = \frac{1}{B(\alpha,\beta)} x^{\alpha-1}(1-x)^{\beta-1} \tag{3}$$

where $B(\alpha,\beta)$ is the beta function (which normalizes the probability distribution), α and β are fitting parameters, and x is considered to be the reduced domain of the variable of interest, i.e. x varies between 0 and 1 where 1 represents the maximum extent of the random variable. As can be seen from the form of the beta distribution, the parameter α controls the shape for small values of the random variable, while β controls the shape for large values. By taking the first derivative of the probability distribution function, one may easily determine that the peak probability must occur at a value of x_{max}, as follows:

$$x_{\max} = \frac{\alpha - 1}{\alpha + \beta - 2} \tag{4}$$

From the output of the scattering simulation, one may easily determine x_{max}. Since α and β are no longer independent once x_{max} is known, one need only determine α or β to uniquely determine the probability distribution for scattering. The shape parameter α can be fixed for a given ion and material (at least for energies where scattering is significant), and β can then be expressed as a function of the ion energy. Thus the scattering problem is reduced to calculating β for a given ion-material pair as a function of the ion's energy as shown in fig. 6. The zenith angle may then be computed based upon the cumulative probability function of equation (4) above, and a desired probability (e.g. most likely zenith angle, or angle whose cumulative probability is 90%, etc.). The azimuth angle is chosen randomly with uniform probability distribution between 0 and 360 degrees. This procedure is repeated to determine the ion's direction after the scattering. (The direction is only weakly correlated with the scattering zenith angle.)

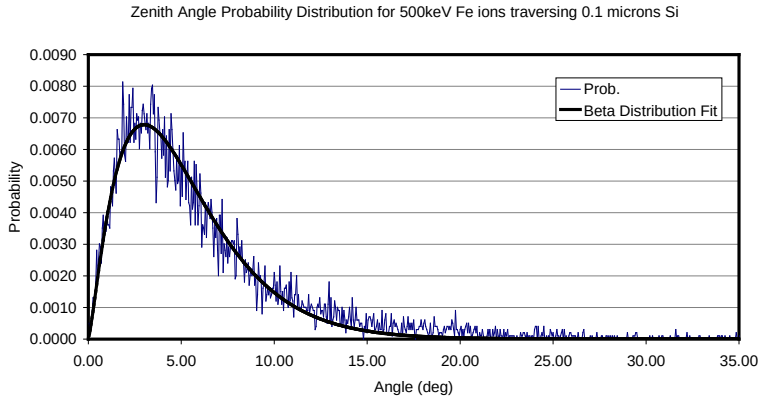

Figure 5: Zenith angle (ϕ) scattering distribution for 500 keV Fe traversing 0.1 micron Si. The solid line is the Beta Distribution fit to the simulated data.

The stopping power of the ion is changed based upon the path length through each prismatoid, the material composition of the prismatoid, and the energy of the ion. The energy dependence of stopping power was downloaded for each ion type in each material type from SRIM, and look-up tables generated. SETsim interpolates the value of the stopping power based upon the initial energy through a path increment in any particular prism in the simulation region. If scattering is not enabled, the path length is the path increment being simulated (usually 0.1 micron). If scattering calculations are enabled, the path length is assumed to be the hypotenuse of the right triangle defined by the path increment and the radial scattering distance (determined by the scattering zenith angle). For small simulation regions, scattering does not appreciably change the path length; however, for larger structures such as photonic sensors, scattering can significantly affect the path length distribution.

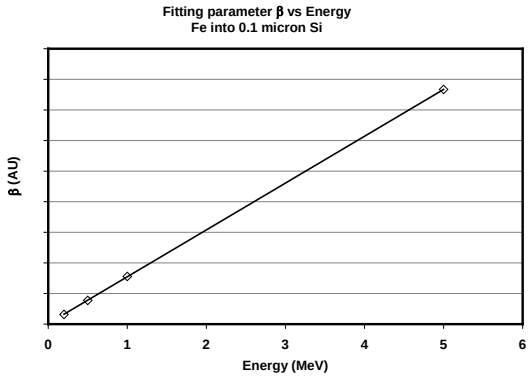

Figure 6: Determining scattering angle fitting parameter as a function of ion energy.

RESULTS

Fig. 7 shows the primary SETsim output: cumulative rate (#/day) vs. deposited charge, in this example for an inverter in a 0.35 micron technology on the worst solar day environment. The critical charge, as determined from Qsim, is shown as a vertical line on the plot. The intersection of this line with the rate vs. charge curve is the SET error rate for this particular cell for the particular environment. In this case, the inverter shown would have an error rate of 2E-9 #/day for the Worse Solar Day environment. This cell would typically only be a candidate for synchronous design use, where the exposure for SET is reduced to a percentage of the shortest clock period, depending upon the slew rate of the clock.

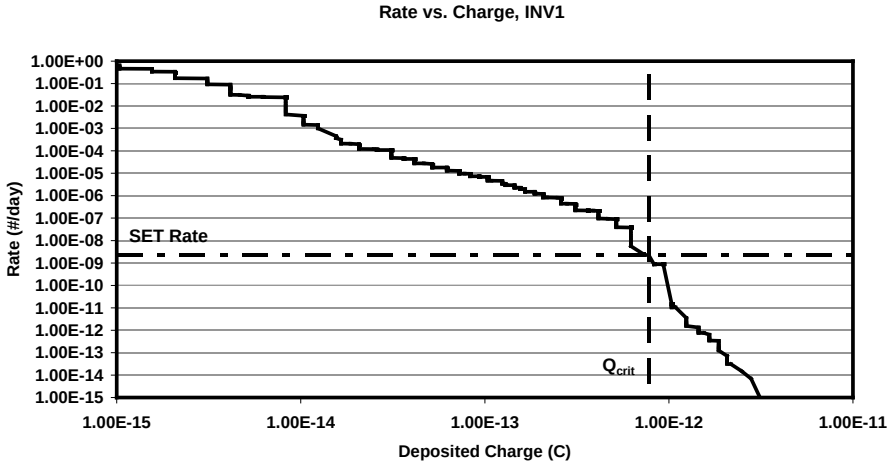

Figure 7: The main SETsim output is Rate vs. Deposited Charge. This shows the Rate vs. Deposited Charge for an inverter in the 0.35 micron technology on the worse solar day.

In designing IC's where SET/SEU performance is a parameter that is optimized just like any other design requirement, curves like Fig. 7 are produced for each cell (analog or digital) in the entire design. SET, ASET, or SEU rates are then associated with each such cell. Just as with Fig. 7, layout designers can run simulations to optimize layout by minimizing the error rate.

SET Scorecard

With a curve similar to Fig. 7 generated for each cell in a design, one can then calculate the SET/SEU error rate for an entire design. Using a "scorecard" approach, each instance of each cell in the design is recorded and assigned a duty cycle (depending upon whether the cell is operated synchronously or asynchronously) to calculate overall error rates. The overall SET/SEU "budget" may be apportioned to different subsets (e.g. clock tree, reset net, power on reset) such that error rates may be reported by criticality, e.g. errors causing chip reset or other Single Event Functional Interrupts (SEFI), errors causing corrupt data (SEU), or transient errors (SET). Designers can use this information to

optimize ASICs for power. Table II shows an extract from a fictitious SET scorecard, showing typical categories of error.

Table II: Example SET scorecard

Design:	YB22									
Environment	Worse Solar Day							**Error Rate Classification**		
Cell Name	**Number of Instances**	**Usage**	**Critical Charge (pC)**	**SETsim Cell Error Rate (#/day)**	**Duty Cycle**	**Total Error Rate (#/day)**		**SEU Error Rate (#/day)**	**SET Error Rate (#/day)**	**SEFI/Critical Error Rate (#/day)**
RHINV2	40	Reset Network	2.0	1.00E-10	100%	4.0E-09				4.00E-09
RHINV4	100	Clock Tree	4.0	5.00E-11	100%	5.0E-09				5.00E-09
RHINV2	1024	Digital Core	2.0	1.00E-10	2%	2.0E-09		2.05E-09		
RHCOMP1	4	Analog	2.0	1.00E-10	100%	4.0E-10			4.00E-10	
TOTALS						**1.1E-08**		**2.0E-09**	**4.0E-10**	**9.0E-09**

SUMMARY

Two simulation tools for a priori determination of maximum SET error rates were reviewed: Qsim and SETsim. Qsim is used during the schematic design of a mixed-signal ASIC program to determine the critical charges for sensitive nodes in analog and digital cells. Architectural changes to the cell may be suggested by Qsim results to improve the value of the critical charge before a lot of time and effort has been expended in physical design of the cell.

SETsim is an alternative to the RPP method that is used to determine the rate at which charge of a given value is deposited in the sensitive regions of the cells. The intersection of the Rate vs Charge output from SETsim and the critical charge from Qsim gives the SET/SEU error rate for the cell. For cells with multiple sensitive electrical nodes, the error rate determined for each electrical node are summed to give the overall error rate for the cell. Using an SET scorecard, with duty cycles assigned to each cell based upon how such cell is operated in the design, classes of error rates can be estimated before the mixed-signal ASIC design is taped out to the foundry.

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