ANALYSIS OF SINGLE EVENT TRANSIENT EFFECTS IN ANALOGUE TOPOLOGIES

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I. INTRODUCTION

Nowadays, the study of the radiation effects affecting mixed-mode circuits in space environment applications is a major concern for designers. From this point of view, the influence of high-energy particle impacts for system performance is becoming crucial as technologies shrink. Higher operation frequencies and smaller transistor dimensions lead to a more critical influence of Single Event Effects (SEE) on the designed circuits. In modern technologies, a well-known threat such as Single Event Transient (SET) errors generated from heavy-ion strikes is becoming even more influential. On the one hand, as higher operation frequencies can be reached, the SET latching sensitivity of the digital parts of the systems is increased. A transient pulse generated at the input of a combinational path can be propagated through the transistor structures and even increase its width; as a consequence, it can produce Single Event Upset (SEU) or Multiple Bit Upset (MBU)[1]. This effect has also been an object of study in digital technologies, and has been called Pulse Induced Propagation Broadening (PIPB) [2][3].

On the other hand, analogue parts of the circuits are even more critically affected by voltage transient perturbations due to impact-generated electron-hole pairs collected by the nodes of devices in deep sub-micron technologies. In addition to this, analogue SETs strongly depend on the electrical system-level configuration of the devices and can seriously affect the overall performance of the circuits. Therefore, the study of SET influence on analogue circuits has become an extremely interesting trend [4], as the analysis of SET sensitivity can provide useful information in order to ensure radiation-hardened designs. However, dealing with the analysis of analogue circuits with more complex topologies than basic logic cells is a challenging tread as the number of transistors increase. Tools like TCAD can extract exhaustive and accurate information of the effects on the proper design layout [5]. Elements like charge sharing or current distributions are clearly depicted, but spending a huge amount of computing effort.

In this paper, a new tool, named as SESAN (SEE Electrical Sensitivity Analyzer), which can offer a rapid diagnostic over analogue designs with a large number of transistors is presented. This tool will automatically modify the circuit netlist adding configurable current sources based on Single Event Transient charge injection models described on literature [6][7]. Additionally, it also implements designer's defined heuristics to automatically extract the most relevant results from simulations. From an initial set of configuration parameters defined by the user, it is possible to rapidly find critical nodes on the selected architectures, allowing the possibility of performing a SET sensitivity analysis in more complex analogue designs.

As a particular case of study, several commonly implemented analogue schemes (operational amplifiers -OpAmp) have been designed and analyzed in a 130 nm CMOS technology of ST Microelectronics using the presented tool. Besides, these topologies are extensively used as building blocks for analogue systems.

II. AUTOMATION PROCESS

In this work, the implementation of the analysis tool has been done through OCEAN [8] automation scripts applied to Spectre netlists under Cadence environment. The whole analysis and simulation process followed by the proposed tool is described in Fig 1.

The injection of SETs is based on realistic induced charge models applied over transistor-level versions of the circuits under test. The proposed simulation method permits analyzing the performance of the analogue circuits under emulated irradiation conditions. Combined with user defined criteria for error discrimination, it is possible to determine the most vulnerable nodes that would require a radiation-hardened design.

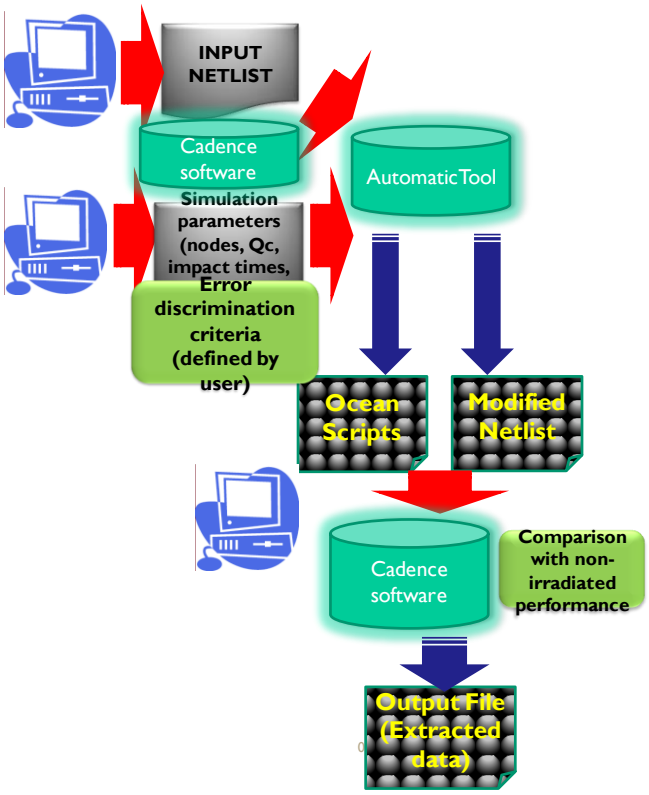

Fig. 1 Script generation and analysis method

The applied simulation method is based on reproducing Single Event Transient effects by means of charge generation models that emulate the current injection produced by particle impacts. The ionization model applied in electrical simulation is a current source with double exponential dynamics, as illustrated in the next equation:

$$I_{rad} = \frac{Q_c}{\tau_d - \tau_r}\left(e^{-\frac{\tau}{\tau_d}} - e^{-\frac{\tau}{\tau_r}}\right) \quad (1)$$

where τ_r is the rise time related to the plasma track dynamics, τ_d is the down time related to charge drift and diffusion in the transistor, and Qc is the net charge associated to the transient current through the transistor node. This is a well-known model widely described in literature [6] that can be implemented using an AHDL model. The current source is injected on the transistor node affected by the particle track. The rise time will be around 1ps, and it is determined by the plasma track physics. The down time is essentially related to the linear energy transfer (LET) value [9] and marginally to the chosen technology, with typical values around 200 ps. The main simulation parameter is Qc, with a minimum value known as critical charge or the minimal amount of net charge needed to produce a SEE. The Qc maximum value can be estimated from the LET through the following formula:

$$Qc = (\rho \cdot LET \cdot d)/3.6 \quad (2)$$

where ρ is the silicon density, LET is the linear energy transfer, d is the device active depth (typically the well depth), q is the elementary charge, and 3.6 (eV) is the threshold energy for electron-hole pair production. Parametric simulations can be set from the maximum Qc down to the critical charge, based on experimental critical LET data in the selected technology.

A first version of the proposed tool has been implemented, which provides two main features: an automatic placement of current sources and the script-based analysis of injected SETs in every node. The results are processed following user defined criteria for error discrimination. Initially, there are two main possibilities for SET analysis over analogue schemes depending on the purpose of the user. On the one hand, global sensitivity evaluations can be performed to test the most vulnerable nodes by injecting lots of SETs in different nodes of the circuit for several impact times. On the other hand, a more selective strategy can be performed by choosing only concrete nodes and times considered to be critical by the designers of the circuits under test. In any case, the implemented methodology can be extended to the analysis of several emulated impacts in different nodes, even providing information of multiple outputs selected by the user.

The evaluation of the influence of SETs over an analogue circuit at transistor level is performed in two steps:

A. Step 1: instrumented netlist generation.

For the simulation and analysis procedure, the presented tool will require the Spectre netlist of the circuit test-bench. This test-bench is generated by the circuit designer in order to test the analogue performance of the scheme. This step does not represent extra work for the designer.

A new netlist will be automatically generated adding an I_{rad} current source to the nodes of the analogue circuit that could be affected by an ionization transient. The SET injection is implemented using configurable AHDL models, as described before. Simulation parameters such as the critical charge (Qc) injected, the rise (τ_r) and down (τ_d) times and the instant in which the particle impact is generated must be defined as inputs by the user (these parameters are technology dependent).

In this way, the main tasks of the designer at this stage are:

- To generate a test-bench for analogue simulation of the circuits under test. This test-bench will be generated using the CADENCE environment with Spectre simulator, as it is useful for analogue designers, with no need for any special consideration about SET effects.
- To define the technology parameters to be used for SET injection by means of the configurable I_{rad} sources, or to load these parameters from a technology file provided by the manufacturer.

As a result of this process, the tool will generate a new Spectre netlist that will be used later by an OCEAN script to evaluate the influence of SETs over the circuit. It should be noted that although an I_{rad} can been added to every node of the designed circuits, the user will be able to select the ones considered for the analysis allowing a computer efficient simulation. This also helps to the possibility of simulating complex circuits by partial analysis of sub-blocks instead of performing a complete analysis of all the designed schemes, which usually can involve too many transistors in analogue designs.

B. Step 2: script generation

In this second step, an OCEAN based script for the analysis of the selected circuits will be generated using the new netlist previously described. Using Cadence OCEAN scripts, ionizing particle impacts can be simulated in Spectre by injecting SETs to the circuits under test. The generated script allows performing a set of parametric transient simulations dependent on the intensity of the particle impacts in one (or several) nodes at different times chosen by the user. The extracted information will be determined by user-defined criteria based on a heuristic analysis of the expected errors.

The main tasks to be performed in this phase by the designer are:

- The user should define the objective impact node or nodes from the possibilities provided by the tool. It is possible to consider all possible nodes or to focus the campaign in a specific part of the circuit.
- The user should define the time of impacts. It is possible to generate SETs in a random or a deterministic way, even in the same node and different time of impact, so that the circuit is evaluated in all possible working points.
- The user should define the nodes considered as outputs and the maximum deviation from a non-irradiated pattern admitted at these nodes. In this way, a set of heuristic criteria based on figures of merit associated to inequations for error discrimination is implemented. For example, thresholds of output's SET pulse duration or voltage deviations.

For every simulation, the output signal affected by any current induced SET on a circuit node is compared to the non-irradiated output response. Two main parameters have been considered for SET sensitivity analysis: the time in which the transient peak generated by an emulated impact fades and the signal recovers it normal shape (recovery time) and the maximum voltage deviation of the signal compared to its ideal (non-irradiated) response. The required precision to recover from a transient error is set to a value of amplitude defined by the user. By means of the implemented script, the effects of injected SETs simulations in the selected nodes of the circuit are analyzed for every simulation and data are extracted and saved to a file to be processed. Fig. 2 shows an example of output file generated by the tool.

From the extracted results, a sensitivity map of the analogue schemes under study can be obtained, determining the most vulnerable nodes to SETs. It can be noted that all the analysis is performed in a transparent way to the designer, providing crucial information for the next steps of the radiation-hardened implementation of the analogue circuits under test.

Output	Impact node	Qc	Timp	Trec	Vmax
/I0/net32	I0_M11	5,00E-13	1,00E-08	5.1	0.109233
/Vout	I0_M11	5,00E-13	1,00E-08	6.4	0.225535
/I0/net32	I0_M11	5,00E-13	2,00E-08	5.1	0.109186
/Vout	I0_M11	5,00E-13	2,00E-08	6.4	0.225493
/I0/net32	I0_M10	5,00E-13	1.3e-08	2.3	0.426629
/Vout	I0_M10	5,00E-13	1.3e-08	3.6	0.183520
/I0/net32	I0_M10	5,00E-13	1.9e-08	2.3	0.370461
/Vout	I0_M10	5,00E-13	1.9e-08	3.0	0.147083
/I0/net32	I0_M13	5,00E-13	8,00E-09	2.8	0.205726
/Vout	I0_M13	5,00E-13	8,00E-09	3.9	0.186725
/I0/net32	I0_M13	5,00E-13	2.2e-08	3.3	0.143872
/Vout	I0_M13	5,00E-13	2.2e-08	4.6	0.231184
⋮					

Fig. 2 Example of an output file generated by SESAN

III. APPLICATION TO ANALOGUE TOPOLOGIES

To test the performance of the developed tool, several amplifier schemes have been designed in a 130 nm CMOS technology and analyzed under simulated irradiation conditions following the proposed methodology. Four classical topologies have been tested: a two stage OpAmp with Miller compensation (Fig. 3a), a telescopic OpAmp (Fig. 3b), a fully cascoded two stage OpAmp (Fig. 3c) and a current mirror OpAmp (Fig. 3d). These designs have been chosen to test their robustness against SET as representative topologies which include common structures widely implemented in analogue schemes, such as current mirrors, differential pairs or cascaded stages where vulnerabilities can be found.

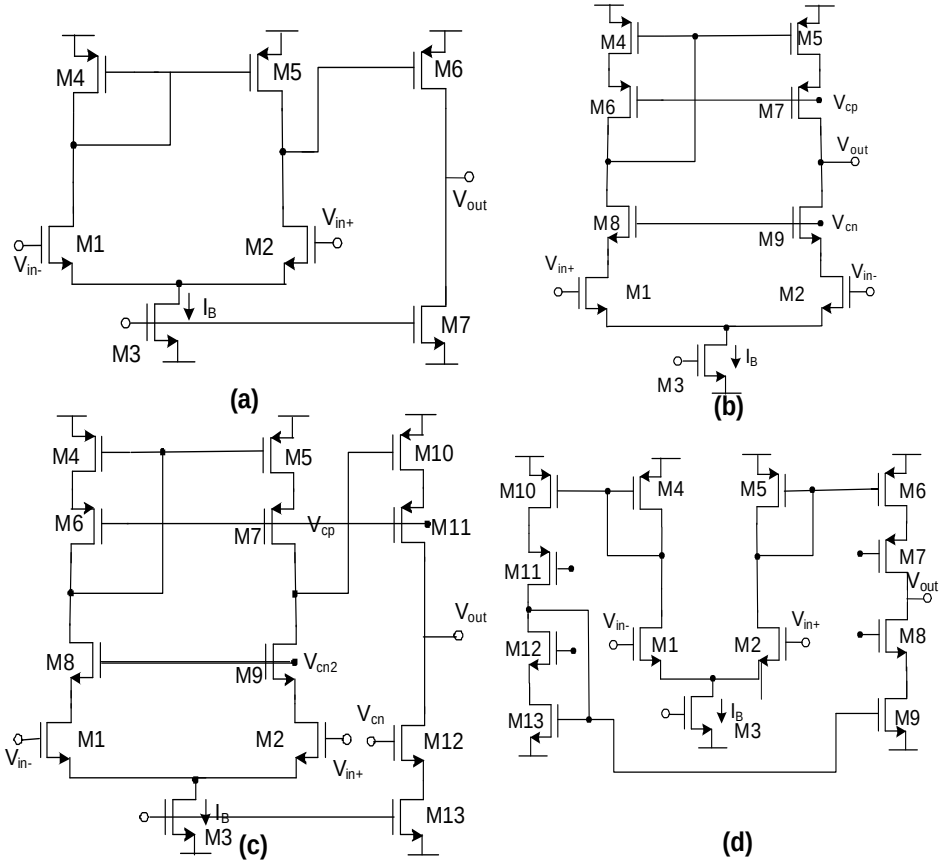

Fig. 3(a) Two stage OpAmp with Miller compensation (b) Telescopic OpAmp (c) Fully cascaded two stage OpAmp (d) Current mirror OpAmp (OTA)

As stated before, our tool employs OCEAN scripts to perform the analysis in an automatic way. The following conditions were considered for this case:

- Different simulations have been carried out varying the impact times along the signal period for a given critical charge and node. In this way, the response of the amplifier will be evaluated for all the possible bias conditions of the transistors.
- No simultaneous impacts on multiple nodes have been considered, as the probability of a multiple impact is nearly negligible. Yet, automatic simulation scripts allow the evaluation of one or more emulated impacts in every possible node of the circuits.

At this point, the main task of the designer will be to generate a test-bench for analogue simulation of the circuits under test. In this case, all the schemes have been simulated using the test-bench shown on Fig. 4a, with a sinusoidal input of 400 mVpp amplitude at a frequency of 200 MHz. An example of simulation for a modeled impact is shown in Fig. 4b, to illustrate the transient response at the output compared to the ideal (non-irradiated) output of the analogue circuit.

Although simulations are initially considered for isolated particle impacts, the analysis can be extended to several nodes, impact times and even different outputs to be processed. As an example, a simulation for an impact on several instants along the signal period on a fixed node (M12 on the current mirror scheme of Fig. 3d) is shown in Fig. 5. The SET injection campaign performed consists on injecting charge pulses on every node of the selected schemes in different times along the signal period to evaluate their performance at the output for different biasing conditions.

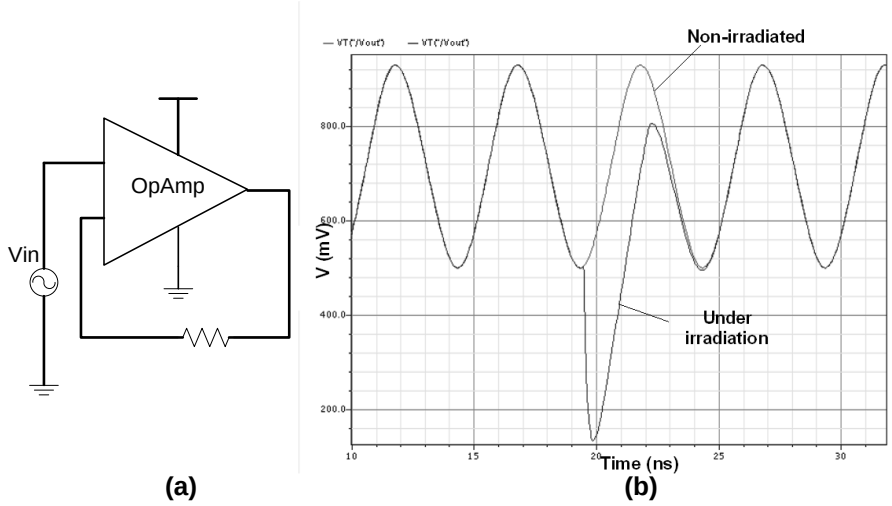

Fig. 4 (a) Simulated OpAmp test bench(b) Transient response to a SET

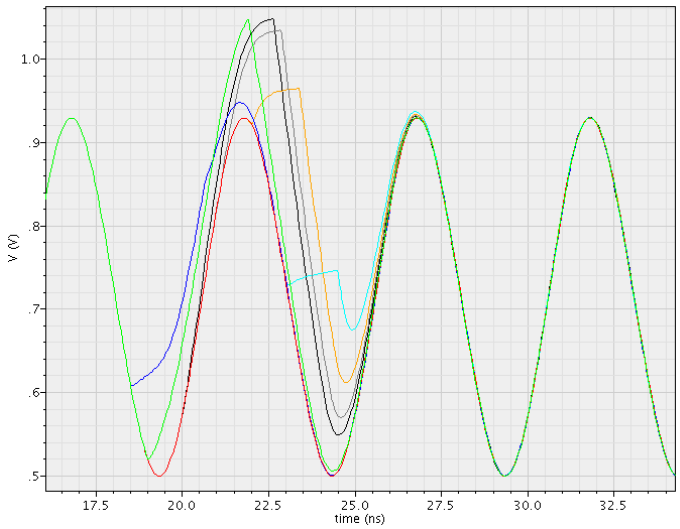

Fig. 5 Transient response to SETs injected at a node in different times along the signal period

TABLE I. MOST SIGNIFICANT RESULTS FOR INJECTED SETS

Effect	Transistor	Recovery time (ns)	Voltage deviation (mV)	Circuit Topology
Largest deviation	M2	3.7	290	Miller OpAmp
Longest recovery	M3	5.1	122	
Largest deviation	M9	3.9	394	Telescopic OpAmp
Longest recovery	M9	4.4	357	
Largest deviation	M8	4.7	450	Current mirror (OTA)
Longest recovery	M12	6.4	225	
Largest deviation	M9	4.5	390	Fully cascoded OpAmp
Longest recovery	M9	6.3	219	

A comprehensive description of the influence of SET in the analogue designed schemes is provided by the tool, analyzing the times and voltage extracted from charge injection simulations in every node of the circuit. The required precision for recovery times has been set to 4 mV in this work. A summary of the most critical nodes in every scheme obtained from simulations is included on table I.

The information extracted from the results shows recovery times of near than one period of the output signals (or even more in some schemes) and maximum voltage variations with similar values to the signal's amplitude. The critical nodes found are consistent with the expected locations derived from theoretical design considerations, showing a crucial influence of injected SETs on biasing nodes and current copies.

IV. CONCLUSIONS

A systematic tool for automatic analysis of analogue circuits affected by high energy particle impacts has been developed and tested. Thanks to the automated placement and script generation, massive injection campaigns can be performed over schematic-level circuits to diagnose their SET sensitivity following user-defined criteria. Additionally, the tool performance is independent from the chosen technology, as the information is provided by the user as a separate technology file. To test the performance of the tool, different topologies of operational amplifiers have been simulated under irradiation conditions using current injected SETs, obtaining consistent results with theoretical predictions for these schemes. These results show the potential of our tool as a valid assessment to find the most critical nodes in the analogue circuits under test.

The implemented methodology allows the determination of possible vulnerabilities under irradiation conditions for multiple analogue topologies and large number of transistors in a transparent way to the user. Furthermore, the proposed tool allows to perform the analysis of simultaneous impacts in different nodes or even to process their influence on several outputs chosen by the user. The work carried out can be considered as a first step of an automation process for the design of radiation-tolerant systems.

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