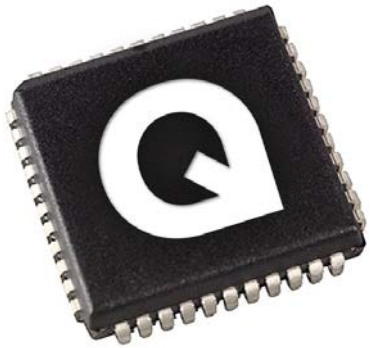
RECONFIGURABLE SYSTEM ON CHIP FOR MULTIPLE APPLICATIONS



E. Pun, D. González, R. Cabás, F. Gutiérrez (ARQUIMEA INGENIERíA SLU).

R. Jansen (ESA)

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OBJETIVES OF THE PRESENTATION

- Present the benefits of a Reconfigurable System On Chip for Multiple Applications
- Present the HF Cosmic Vision ASIC Architecture and how it can fit several applications
- Present the expected performance of the chip
- Present the first Test Chip and its differences with the final chip
- Present the IPs availability

RATIONALE BEHIND THE ASIC (BACKGROUND)

- The ASIC development is an activity in the frame of The Cosmic Vision Science Program from ESA (JUICE –Jupiter ICy moons Explorer).

- JUICE is to be Europe's next large science mission

- Is part of the effort to develop high reliability, high performance integrated circuits for space use in Europe

- For more information visit the Cosmic Vision site at: sci.esa.int

RATIONALE BEHIND THE ASIC (OBJECTIVES)

- To develop a single ASIC that can be used for different applications
- The users will learn how to use one single device and could use it for various purposes
- With the objective of getting a good performance regardless of the application
- Able to meet the radiation requirements of the mission
- To be used for frontend readout, basic analogue signal conditioning and data conversion

RATIONALE BEHIND THE ASIC (OBJECTIVES)

- The ASIC is then envisaged to be

1. Radiation tolerant
2. Reconfigurable
3. Tunable
4. Multi-functional
5. Suitable for multiple instrumentation applications

RATIONALE BEHIND THE ASIC (APPLICATIONS)

➢The ASIC is conceived to suit the following applications:

1. Radiation detector
2. Radiation spectrometer
3. CCD signal processor
4. ADC
5. DAC
6. Filter
7. Low Noise Amplifier

RATIONALE BEHIND THE ASIC (TECHNOLOGY)

- The ASIC is designed for and manufactured in the 180nm CMOS UMC process using the radiation-hardened DARE library.

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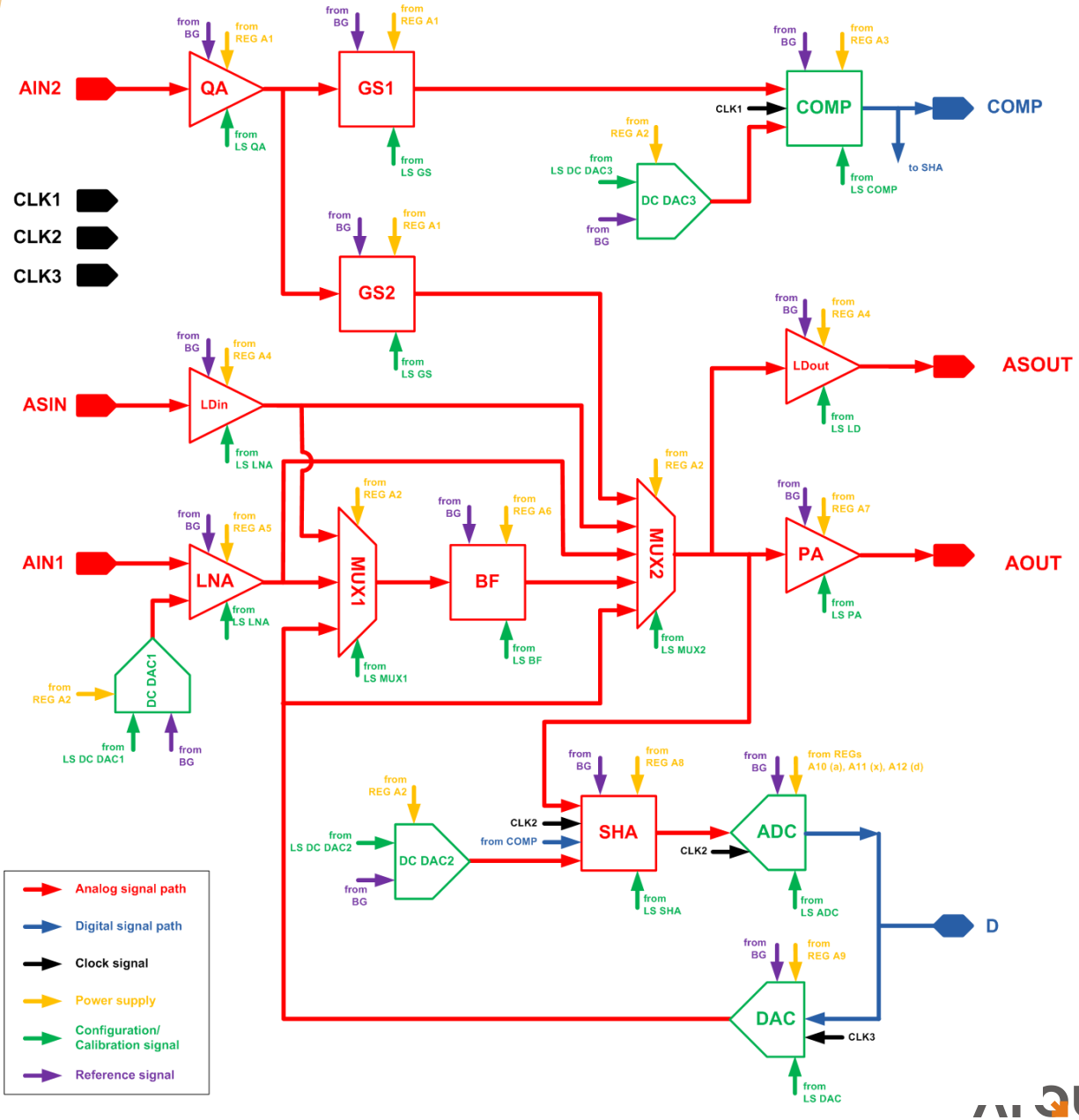
ASIC ARCHITECTURE



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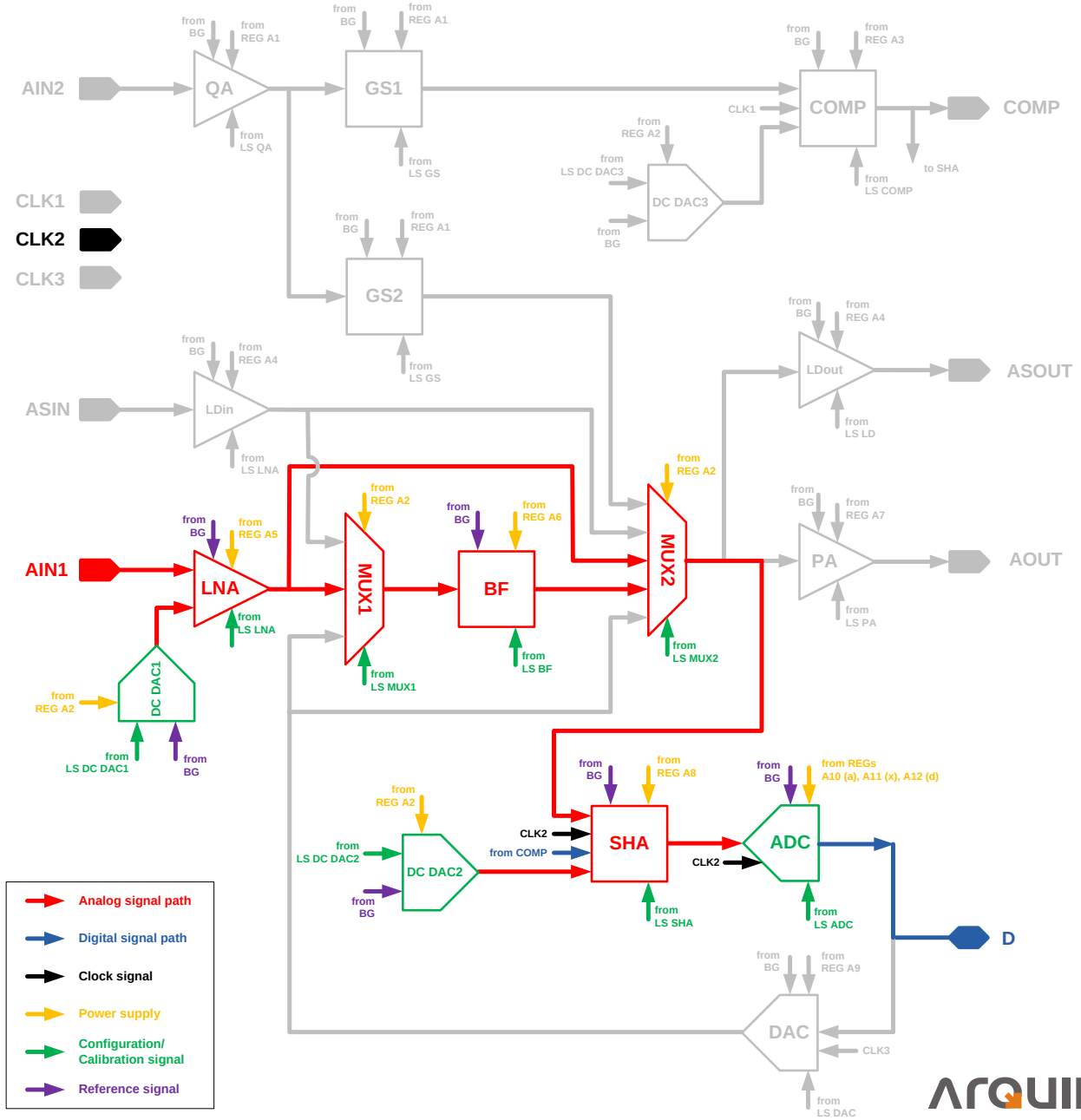
APPLICATIONS (CCD signal processor)



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APPLICATIONS (CCD signal processor)

Nº	Parameter	Value	Unit	Comments
1	Input range	[0; 1.5]	V	Specified for single ended
2	Input clamping	Configurable from 0 to 1.5	V	Specified for single ended
3	Input clamping step	100	mV	Specified for single ended
4	V/V gain (before filtering)	Configurable from -6 to 30	dB	
5	V/V gain step (before filtering)	1	dB	
6	V/V gain flatness	0.4	dB	
7	Noise insertion (before filtering)	6	nV/√Hz	Frequency range [0.1;10] MHz
8	Offset correction (after filtering)	Configurable from 10 to 1000	mV	Specified in single ended
9	Offset correction step (after filtering)	10	mV	Specified for single ended
10	V/V gain (before conversion)	Configurable from 0 to 30	dB	Post-offset correction
11	V/V gain step (before conversion)	6	dB	Post-offset correction
12	Sample rate	Configurable from 10 to 100	MHz	
13	Effective Nº of bits	12@10 10@100	Bits@MHz	Values for different sampling rates
14	ASIC current consumption	300	mA	A maximum voltage gain and maximum speed condition

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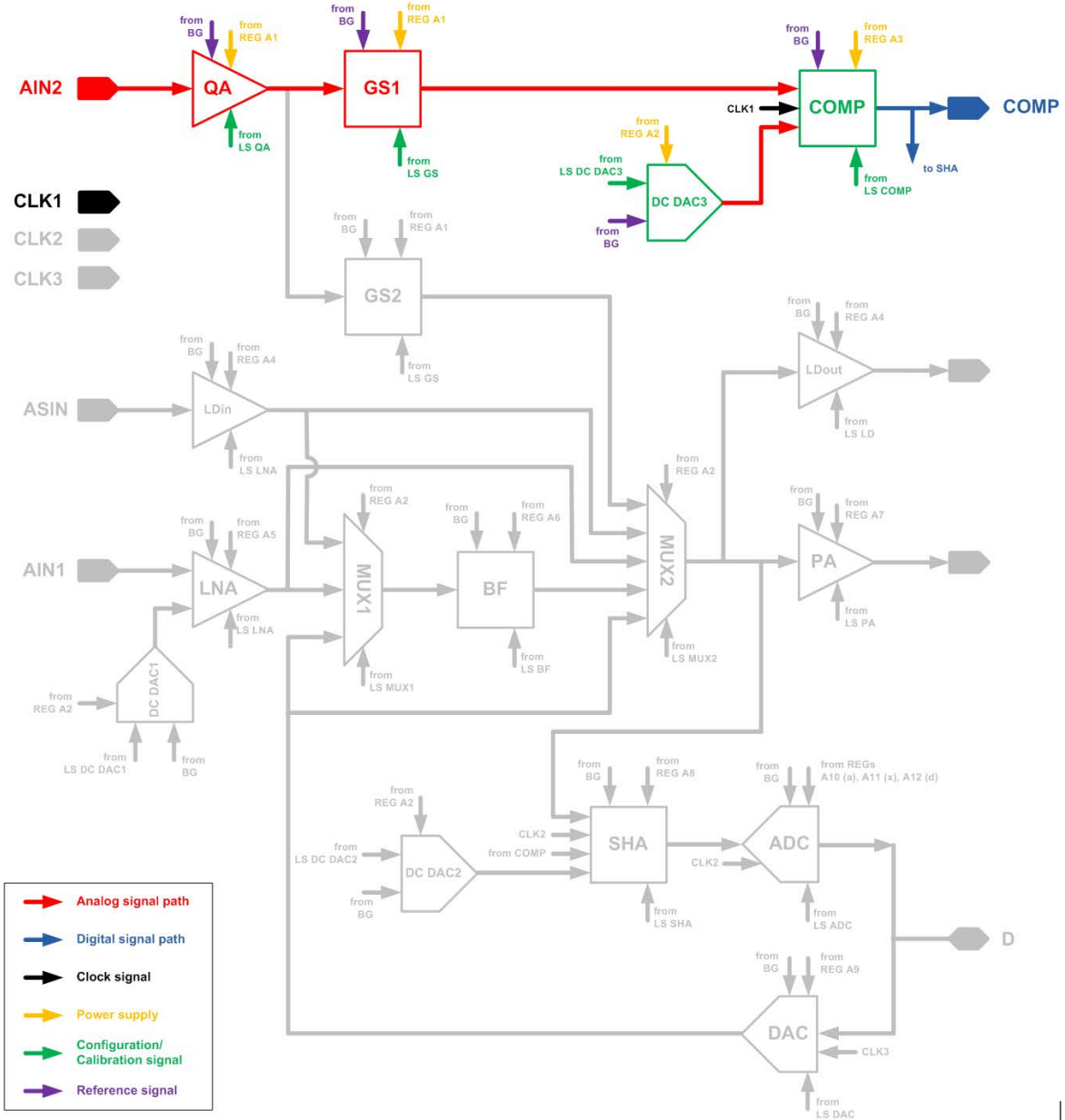
APPLICATIONS (Radiation Detector)



APPLICATIONS (Radiation Detector)

Nº	Parameter	Value	Unit	Comments
1	ENC	120	e_{rms}	Input capacitance 10pF and peaking time 10µs
2	ENC slope	12	e_{rms}/pF	Peaking time 10µs
3	Range	200@0.2 20000@20	fC@pF	Feedback capacitor
4	Peaking time for Gaussian shaper	[0.1; 10]	µs	
5	Peaking time accuracy for Gaussian shaper	5	%	
6	Threshold level	[10; 1000]	mV	
7	Threshold step	10	mV	
8	Current consumption contribution of LNA and filter	50	mA	10µs peaking time

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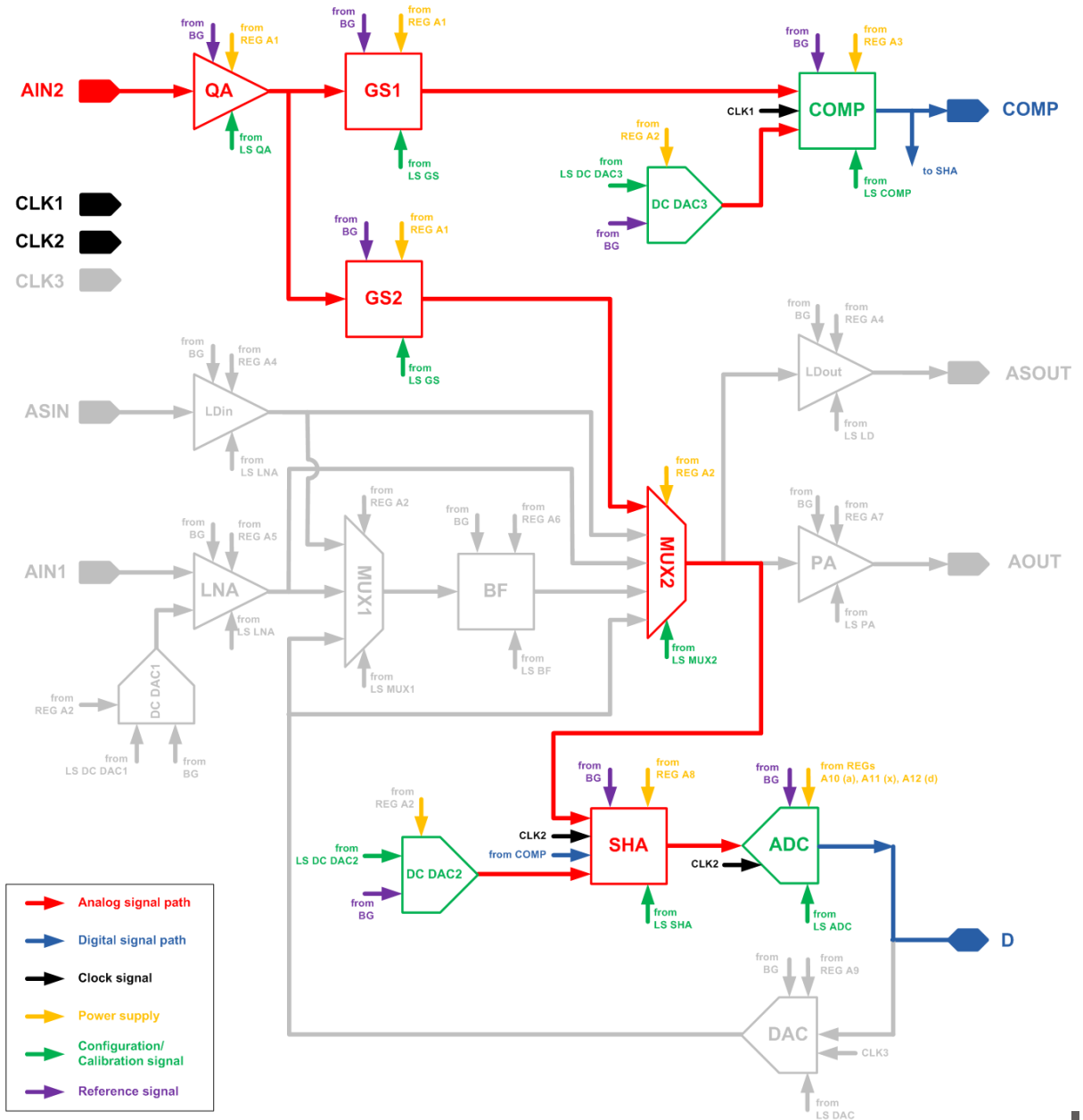
APPLICATIONS (Radiation Spectrometer)



APPLICATIONS (Radiation Spectrometer)

Nº	Parameter	Value	Unit	Comments
1	ENC	120	e_{rms}	Input capacitance of 10 pF and peaking time of 10µs
2	ENC slope	12	e_{rms}/pF	Peaking time of 10µs
3	Range	200 @ 0.2 2000 @ 20	fC@pF	Feedback capacitor
4	Peaking time for Gaussian shaper	[0.1; 10]	µs	
5	Peaking time accuracy for Gaussian shaper	5	%	
6	Effective number of bits	12 @ 10 10 @ 100	bits@MHz	See ADC configuration for further specification
7	Threshold level	[10; 1000]	mV	
8	Threshold step	10	mV	Specified for single ended
9	Current consumption contribution of LNA and filter	50	mA	10µs peaking time (TBC)

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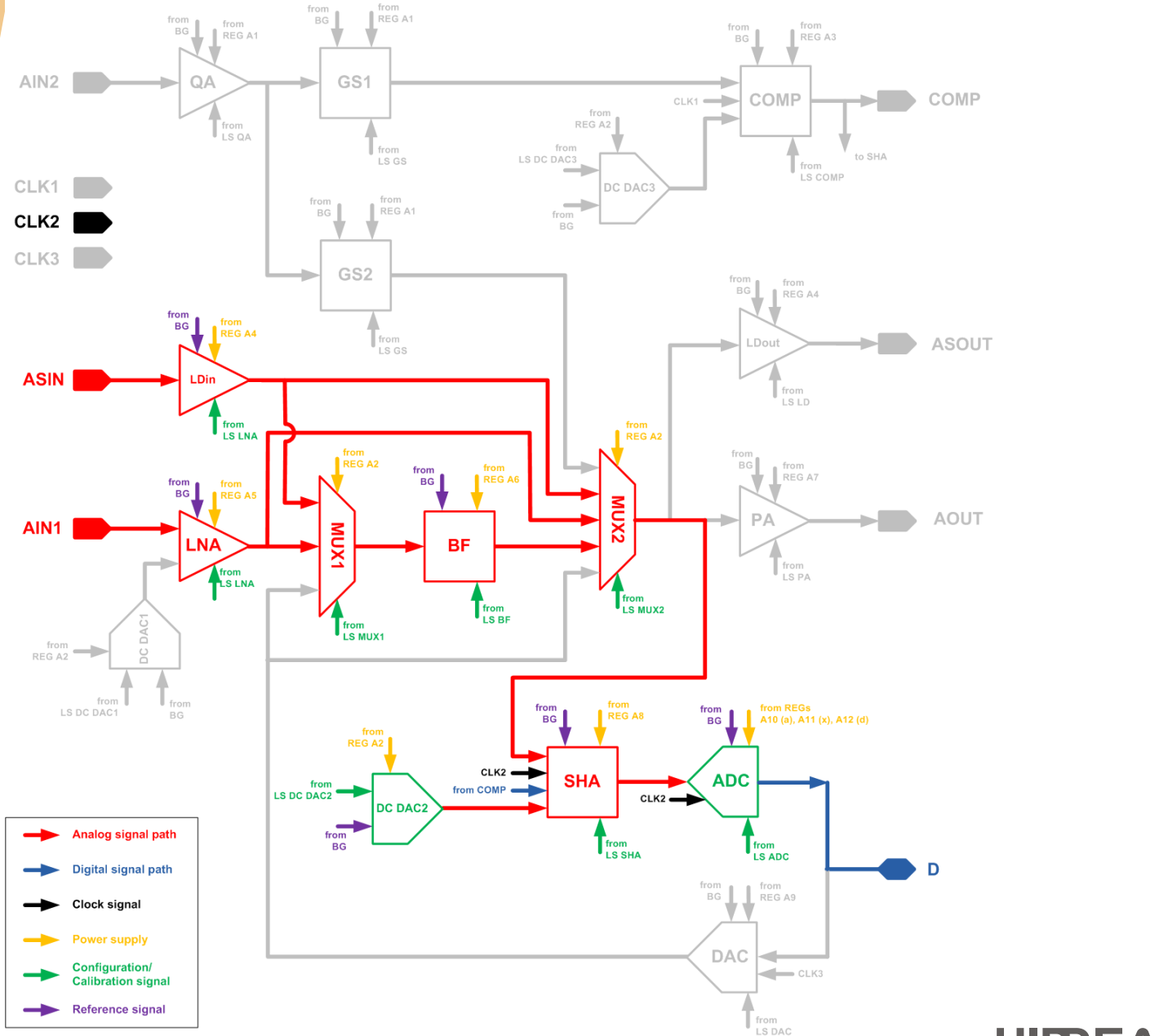
APPLICATIONS (ADC)



APPLICATIONS (ADC)

Nº	Parameter	Value	Unit	Comments
1	Number of bits	15 @ 10 15 @ 100	Bits @ MHz	
2	Sample rate	[10; 100]	MHz	
3	Effective number of bits	12 @ 10 10 @ 100	Bits @ MHz	
4	Input range	2	Vdpk	Differential input and nominal gain
5	Maximum gain flatness	0.4	dB	Over the signal frequency range of 50kHz – 5MHz
6	Maximum gain stability	0.1	dB	Overt the temperature range
7	Minimum THD	74@10 64@100	dB@MHz	
8	Minimum SFDR	74@ 10 64 @ 100	dB@ MHz	
9	Current consumption contribution of ADC block	250 @ 100	mA@MHz	Typical

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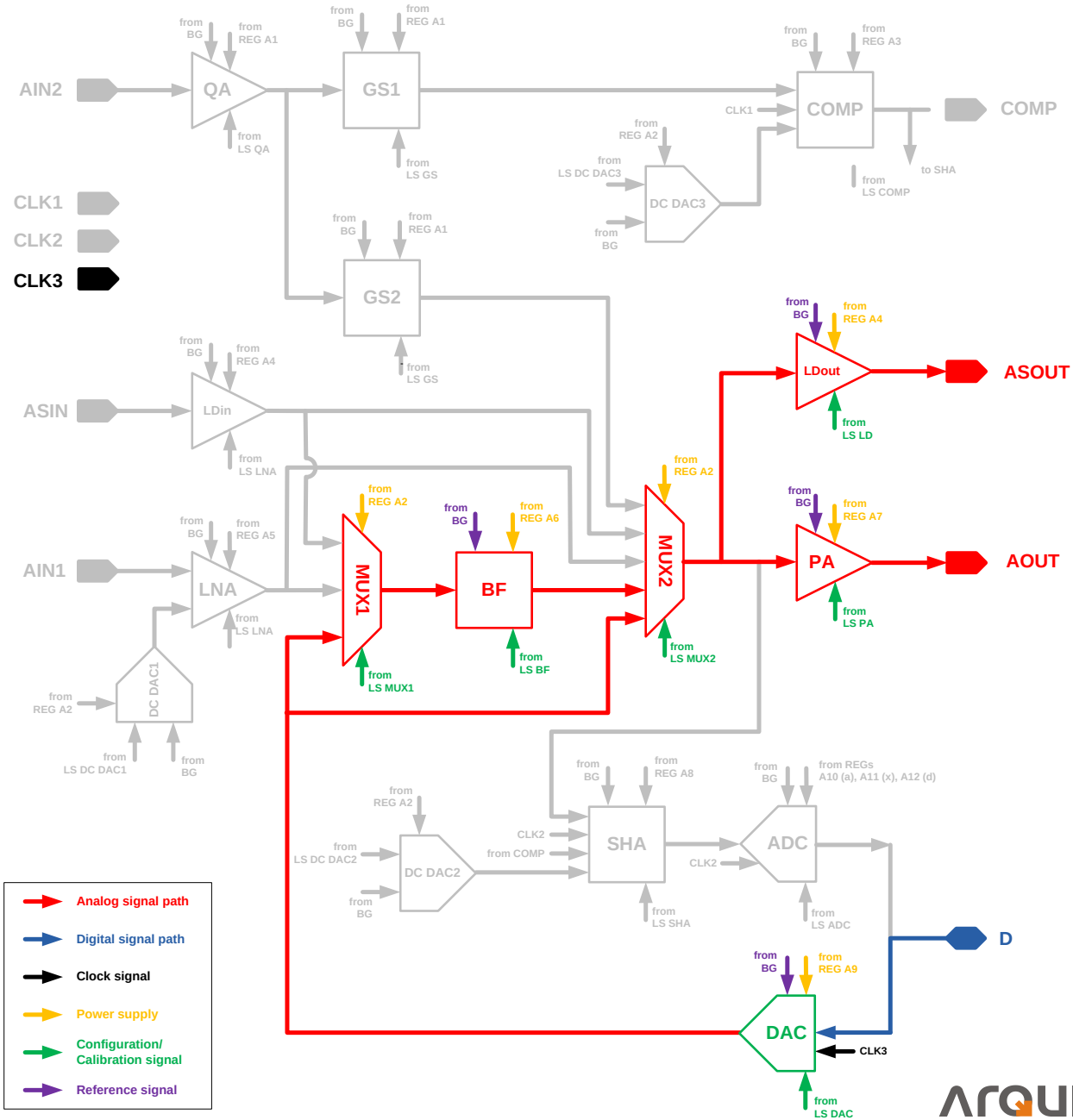
APPLICATIONS (DAC)



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APPLICATIONS (DAC)

Nº	Parameter	Value	Unit	Comments
1	Number of bits	15 @ 10 15 @ 100	Bits @ MHz	
2	Sample rate	[10 - 100]	MHz	
3	Effective number of bits	12 @ 10 9 @ 100	Bits @ MHz	
4	Output range	2	Vdpk	Differential output and nominal gain
5	Maximum gain flatness	0.44	dB	For 5MHz – 50MHz range with digital predistortion.
6	Maximum gain stability	0.1	dB	Overt the temperature range
7	Minimum THD	72@10 57@100	dB@MHz	
8	Minimum SFDR	74 @ 10 59 @ 100	dB@ MHz	
9	Current consumption contribution of DAC block	60 @ 100	mA@MHz	Typical

TEST CHIP (OBJETIVES)

- Be able to validate the functionality and the performance of the most critical blocks of the ASIC as separate entities
- Be able to test its behavior under radiation (done as a separate activity by ESA).
- To be fabricated on IMEC-UMC October foundry run (5x5mm^2 die)
- Encapsulated in a CQFP-120 package

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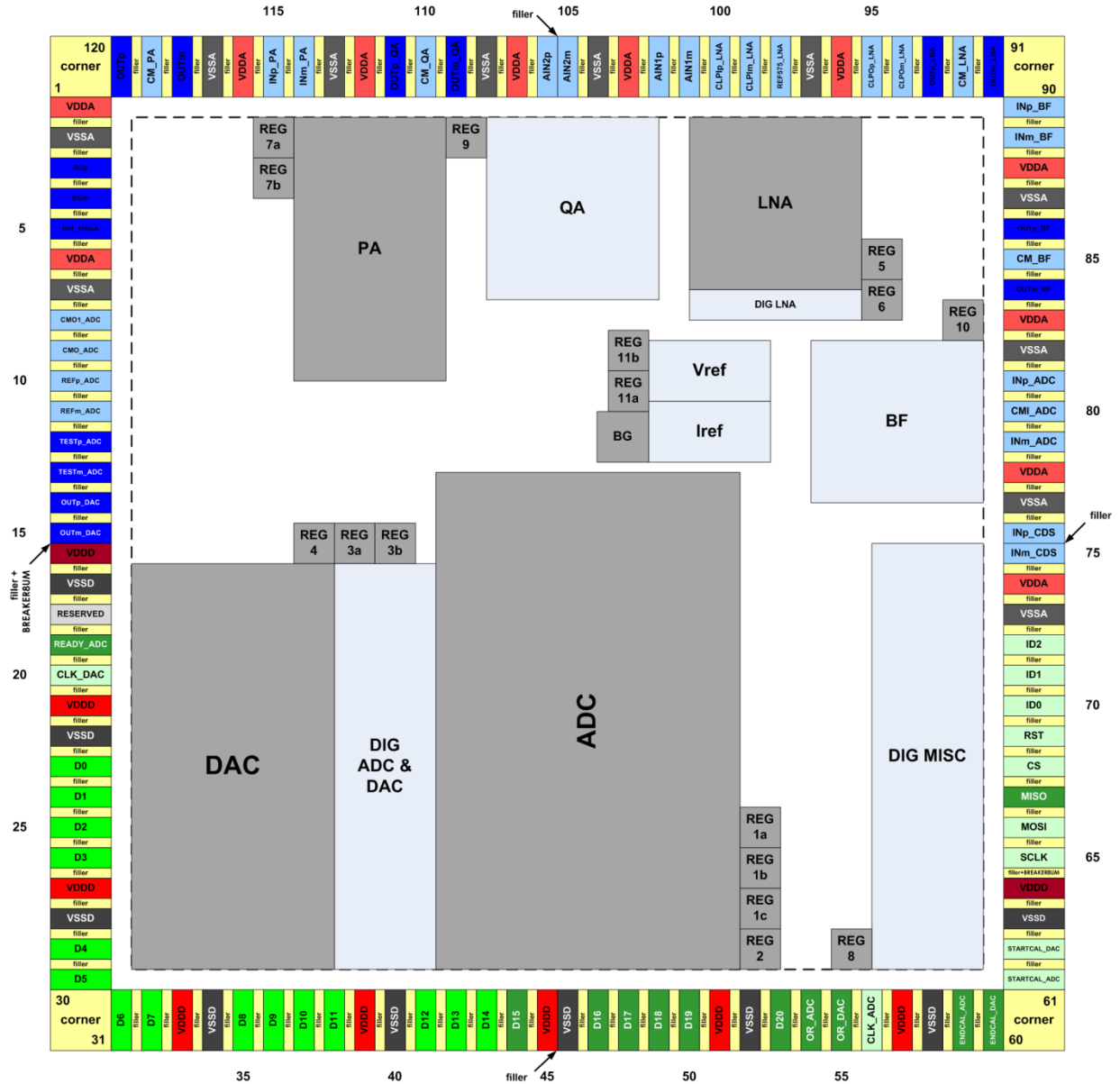
TEST CHIP (FLOORPLAN)



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TEST CHIP vs FINAL CHIP

- Multiplexors, line drivers, gaussian shapers and DC DACs included
- To be encapsulated in a CQFP-64 package
- It looks like we will have to move to a 10x5 mm^2 die
- Tape out expected in Q1-2013

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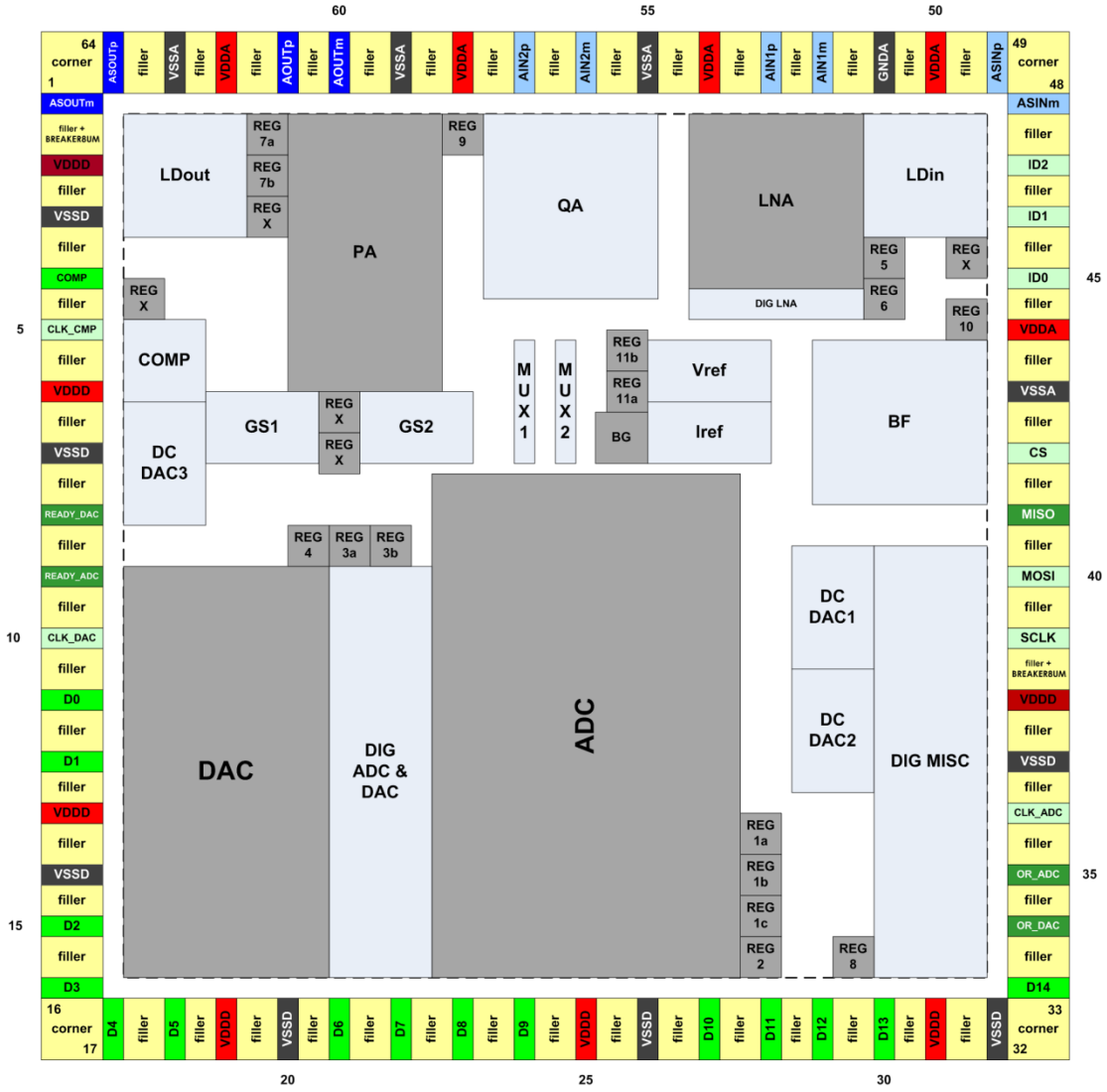
TEST CHIP vs FINAL CHIP (PRELIMINARY FLOORPLAN)



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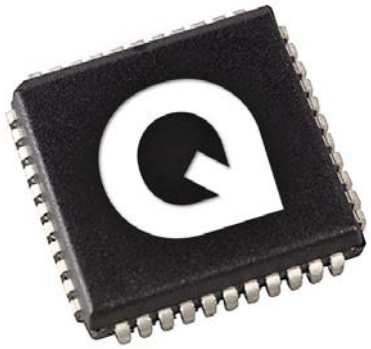
IPS AVAILABILITY

- The IPS can be re-used to build other ASICs
- This will help customers adjust the blocks to their needs in order to reduce pins, consumption, etc.
- The IPS will be included in the ESA database for ESA projects with the support from ARQUIMEA. (for other projects contact us for further details)



Acknowledgements

ESA

CSIC-CNM (ADC and DAC)

UPC (LNA and PA)

UC3M (Digital design)

USE (Filter)

IMEC (Digital Backend and fabrication)

And thank you for your attention!

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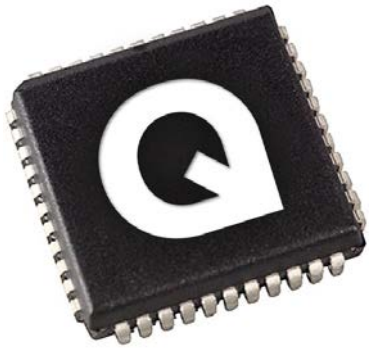

ARQUIMEA PARTICIPATES IN

APOLO DEVELOPING RADIATION HARDENING TECHNIQUES

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