The Essential Telemetry (ETM) ASIC

A mixed signal, rad-hard and low-power component for direct telemetry acquisition and miniaturized RTU

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AMICSA 2012

Design Motivation

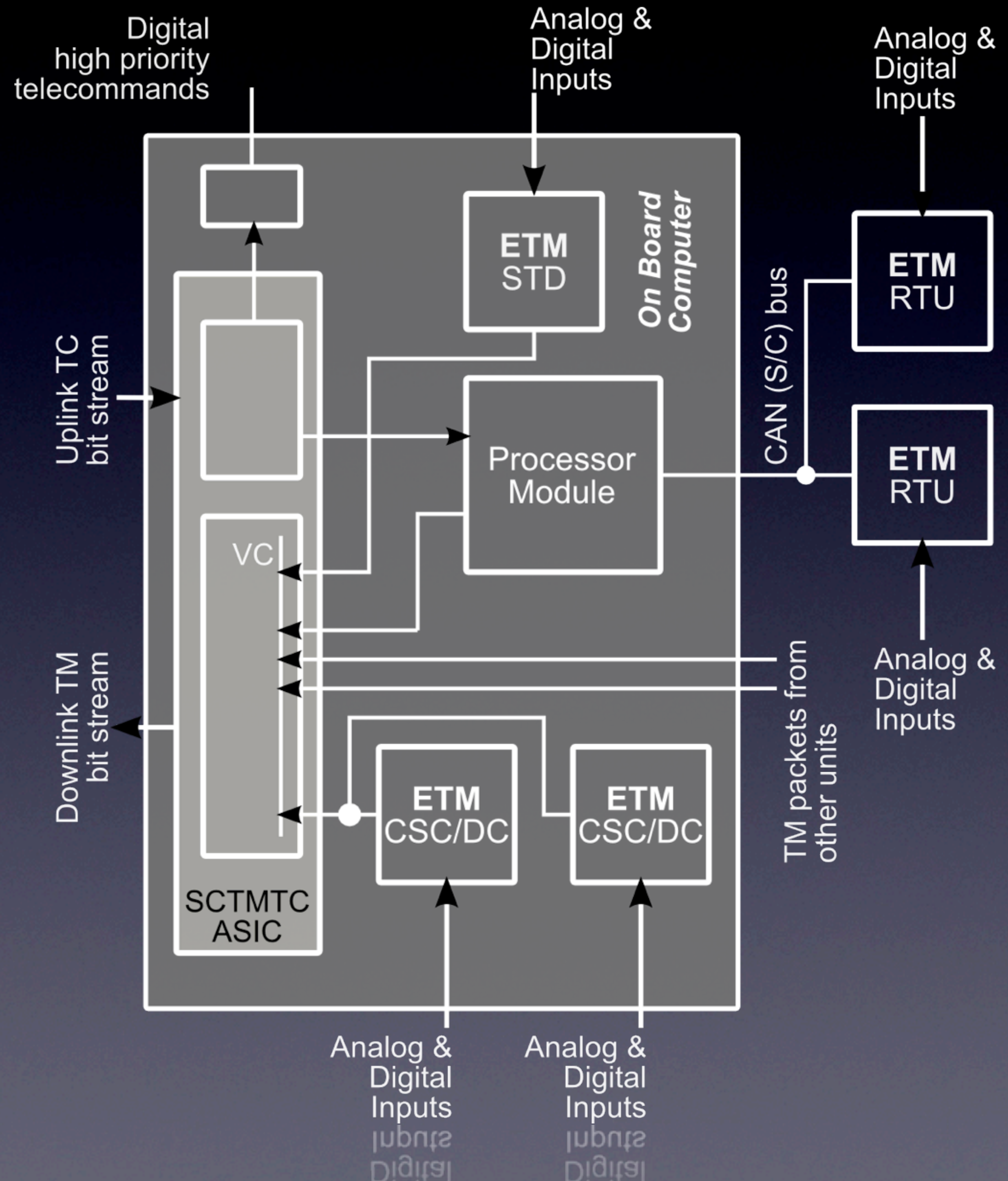
- Develop an **RadHard low power** ASIC capable of autonomous analog & digital data acquisition and formatting for transmission to ground without the need of a S/C computer (Essential Telemetry).

- Interface with existing Telemetry Encoding and Telecommand Decoding systems
    - Single Chip TeleMetry & TeleCommand (SCTMTC) ASIC developed under ESA

- Use the ASIC as a miniaturized low power Remote Terminal Unit (RTU) for telemetry acquisition via CAN bus.

Applications of the ETM ASIC

- **Stand Alone** (STD)
  - ETM is connected to a VC of the SCTMTC ASIC.
  - Functionality can be configured only through hard pins.
- **Cascaded Daisy Chain** (CSC/DC)
  - Many ETM devices are connected to a VC of the SCTMTC ASIC.
  - Functionality can be configured only through hard pins.
- **Remote Terminal** Unit (RTU)
  - ETMs are connected on the S/C CAN bus.
  - Functionality can be configured through the CANopy layer.



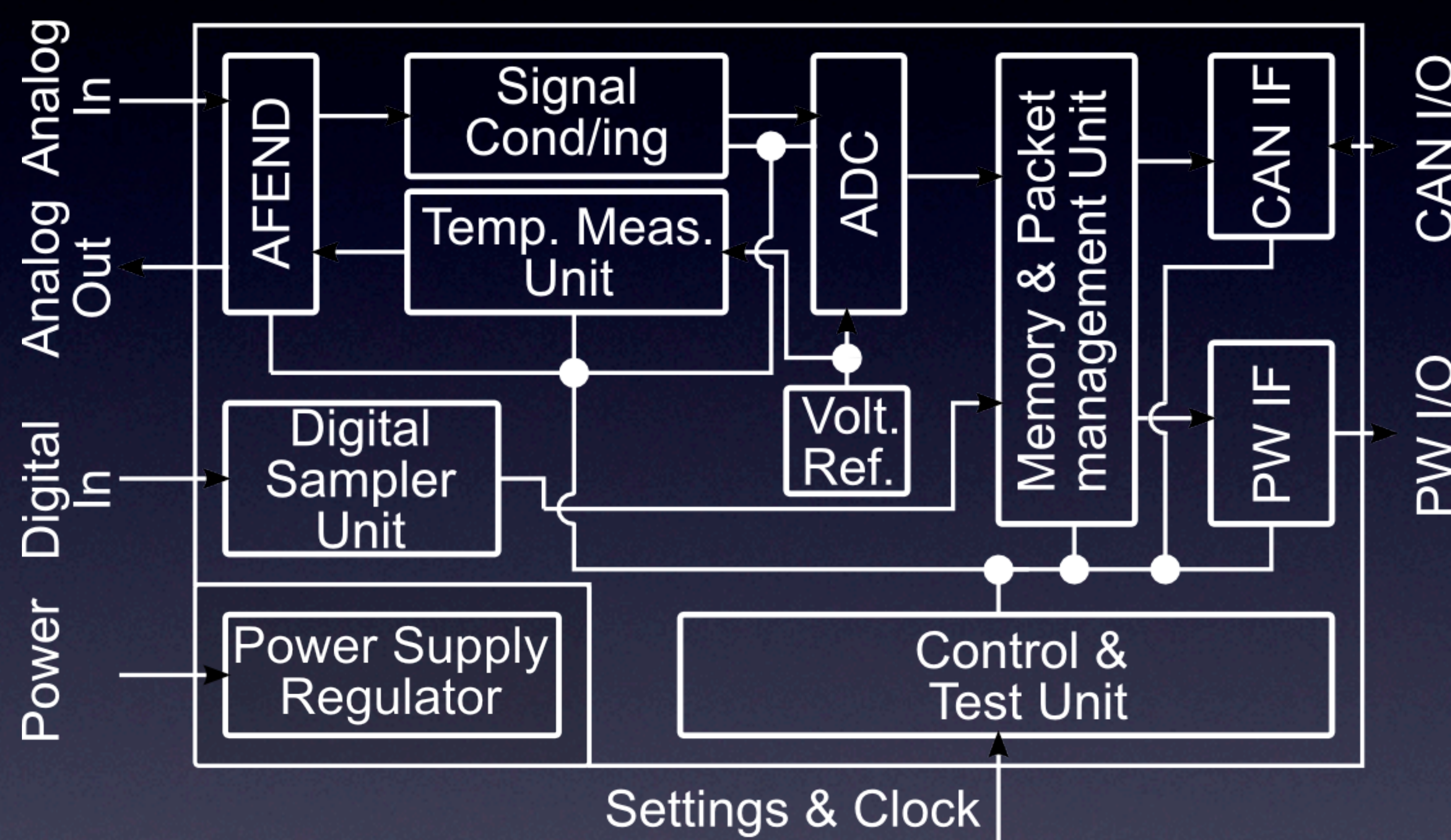
ETM configurable functionalities

- Communication interfaces
- Number of channels that are sampled
  - Channels are organized in groups (Ch0-3, Ch4-7, Ch8-15 & Ch16-31)
- Channel group measurement type (Voltage/Temperature or 1 bit ADC)
- Sample period (256us to 60sec)
- Packet Characteristics (Time of Origin, CRC, Header)
- Sample condition (continuous or upon change)

ETM ASIC block diagram

Consists of

- an analog front end mux/demux that directs the 32 analog inputs to the ADC and also selects the temperature sensors that will be biased by the ASIC.
- a signal Conditioning Unit
- a temperature measurement unit which directs a constant current to the external temperatures sensors
- a 12 bit digitally auto zeroed ADC
- a digital Input Sampler capable of handling differential inputs
- a voltage reference unit
- a memory unit
- a space Packet Generation unit
- a PacketWire IF
- a CAN IF
- a Control and Test unit
- a power supply regulator used to power the core of the device from the I/O power supply of 3.3V.



Control and Test Unit consists of:

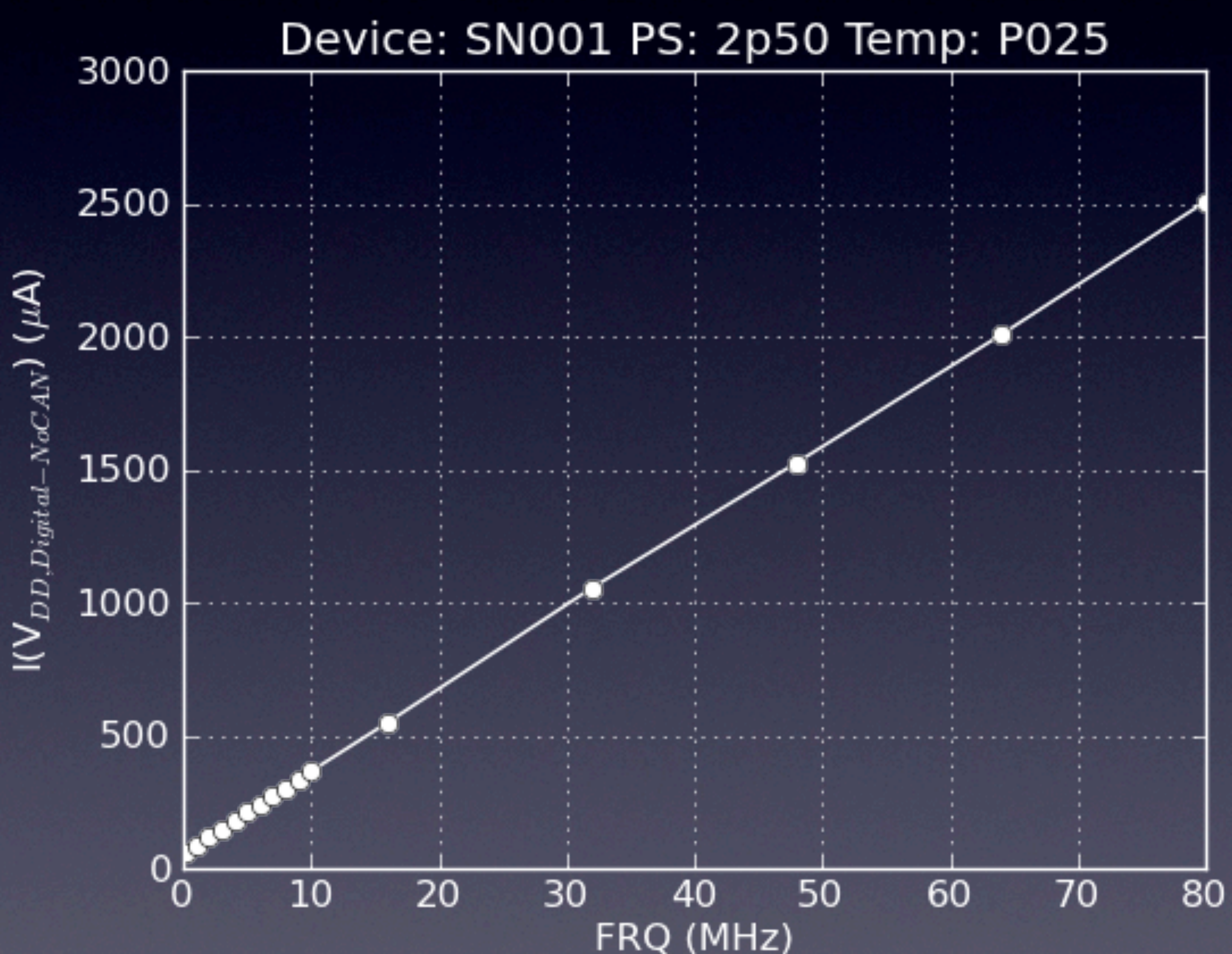
- Main FSM
- Internal clock oscillator
- BIST schemes both for the analog and digital sections

Status

- Fabricated at IHP 0.25um SiGe Process
- Die size is 5.2 x 5.2 mm^2
- Assembled in CQFP 256 and PGA 256 packages
- Characterization of FM devices has been concluded
- Qualification process to start in Q3 2012

Operating Currents

- Total Current = Frequency Dependent Current + Non Frequency dependent Current
- Frequency dependent Current: Digital current except from CAN/CANopen
- Non Frequency dependent current: CAN/CANopen + analog



Operating Currents

OSC	Measurement type	Configuration	Total Current (mA)
Ext	Voltage Only	STD	2.7
Int	Voltage Only	STD	3.2
Ext	Voltage Only	RTU	3
Ext	Voltage and Temperature	RTU	4
Int	Voltage and Temperature	RTU	4.5

- Single Power Supply with on chip voltage regulator
- WC Power consumption is *14.85mW*
- Power for essential telemetry measuring voltages and temperatures is *12mW* including sensor power

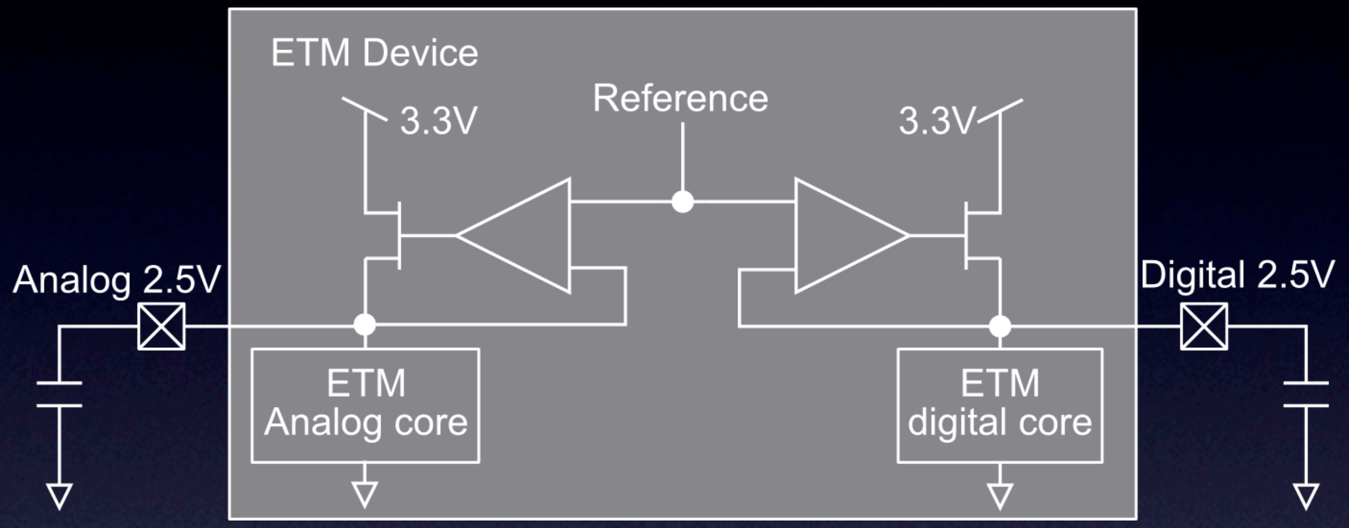
Power Supply Regulator

- Low drop out (LDO) Linear regulator chosen over buck topology

- Core 2.5V power supply is generated from the 3.3V.

- Device is low power and thus efficiency is not important

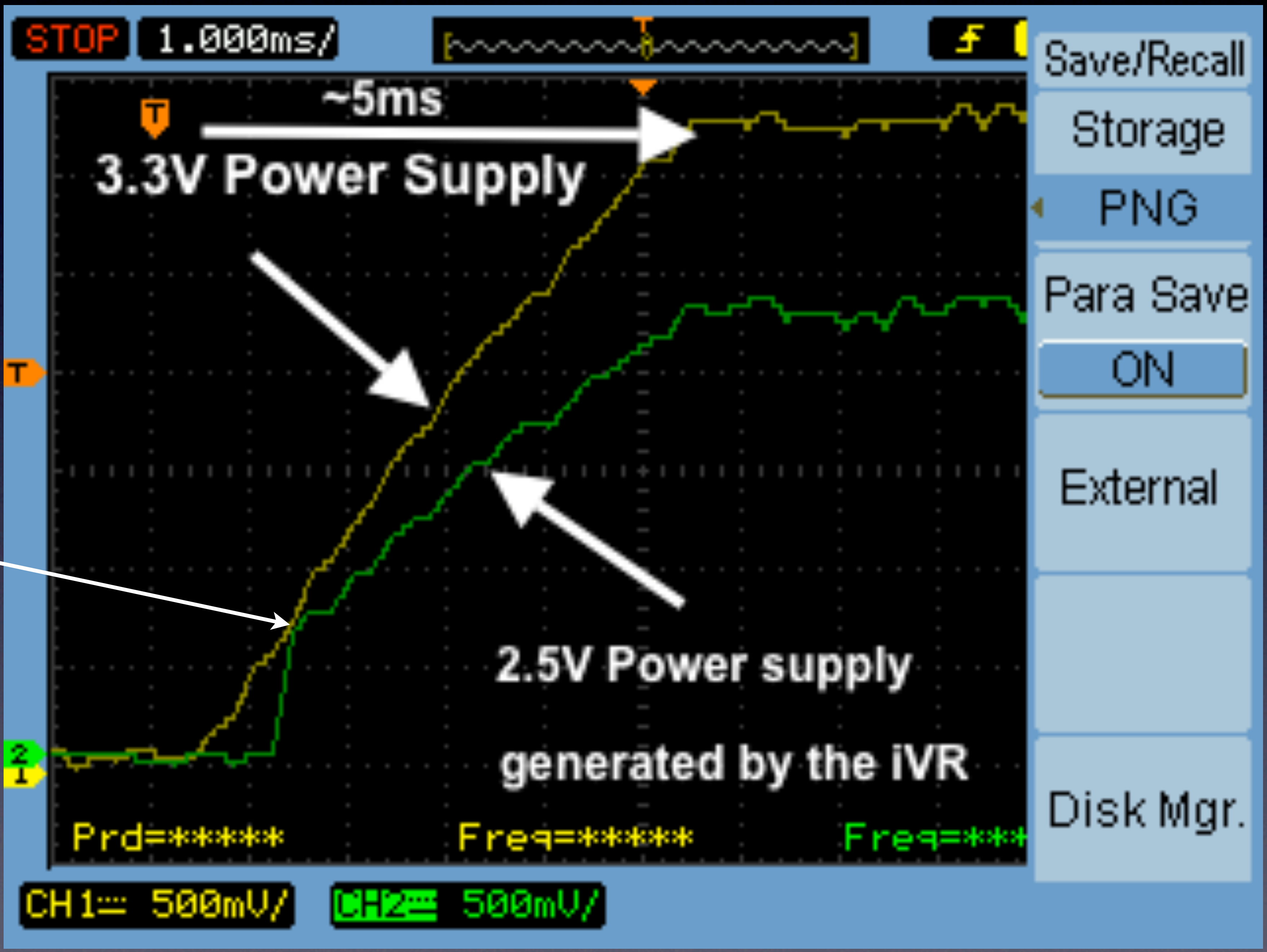
- 3.3V is more standarized for the S/C with respect to 2.5V



- With this topology it is easy to power down the regulator and provide the 2.5V externally

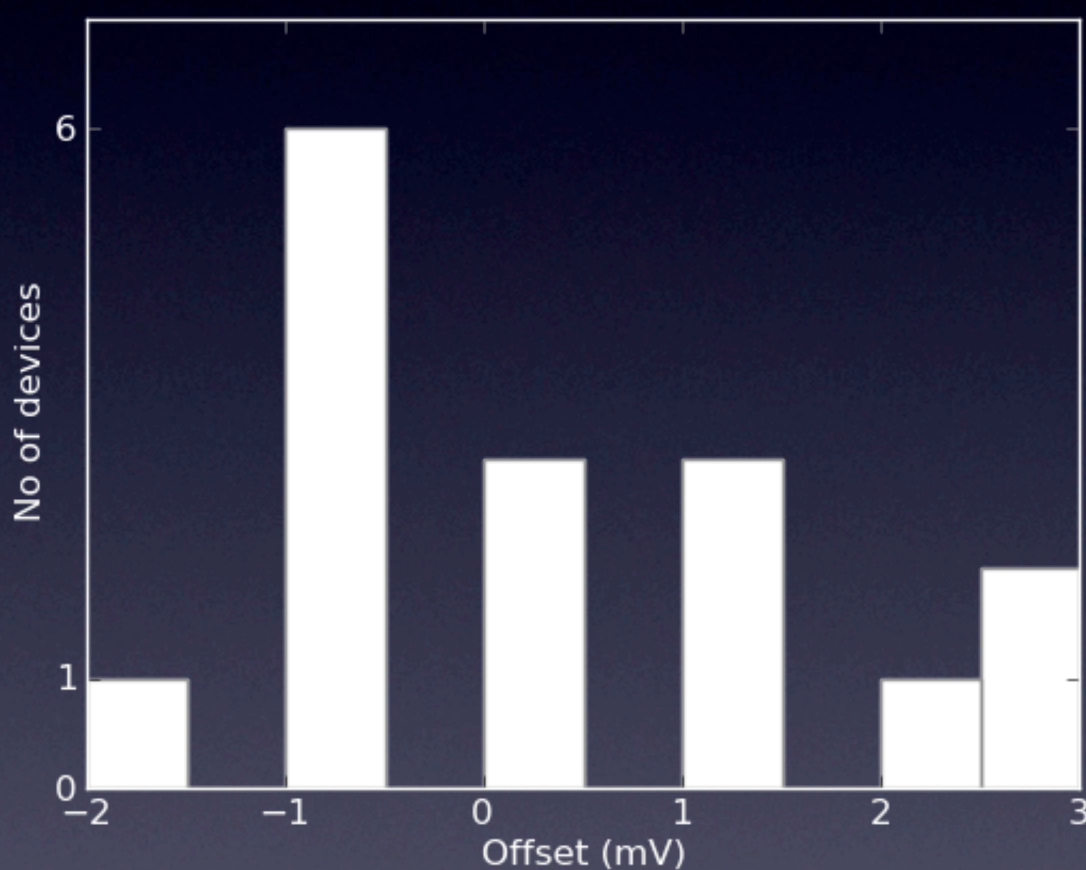
Power Supply Regulator

- Power up sequencing
- After 700mV Vdd2p5 follows Vdd3p3
- Power supplies are established in the device simultaneously
- No latch up susceptibility due to power supply sequencing

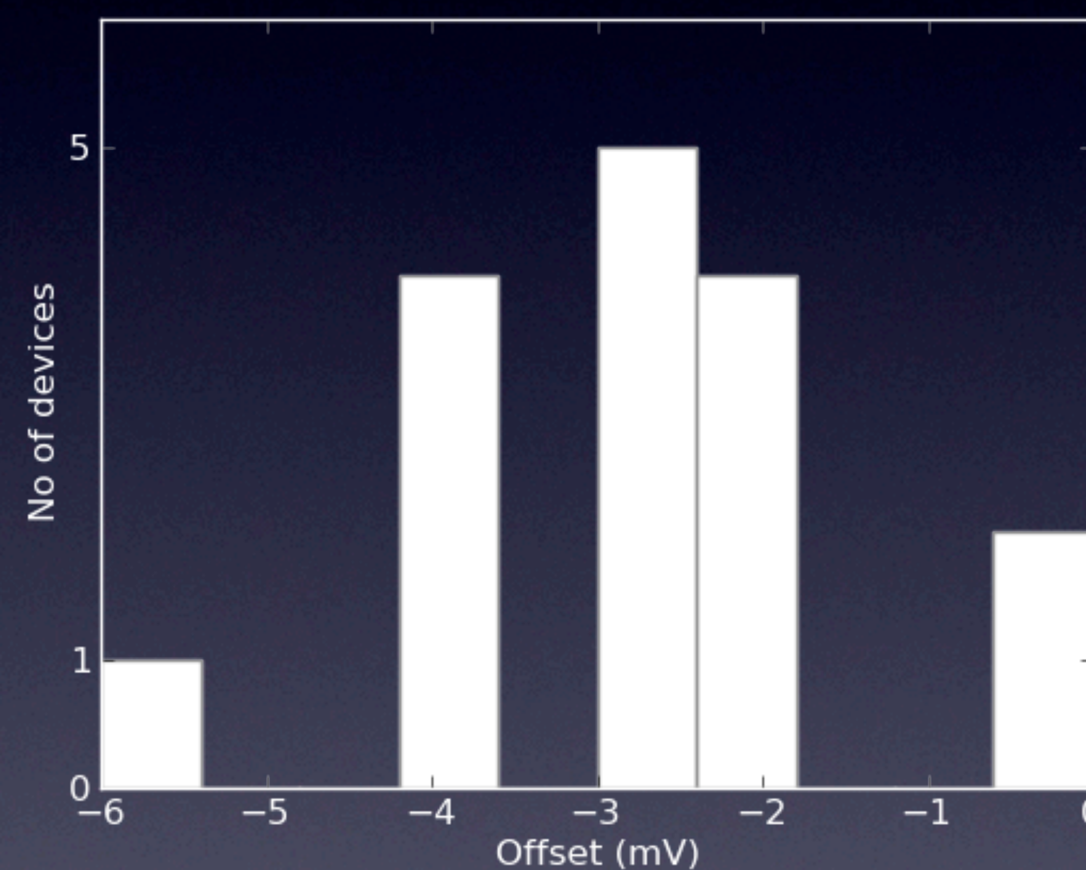


Power Supply Regulator

Analog Power Supply Voltage Regulator

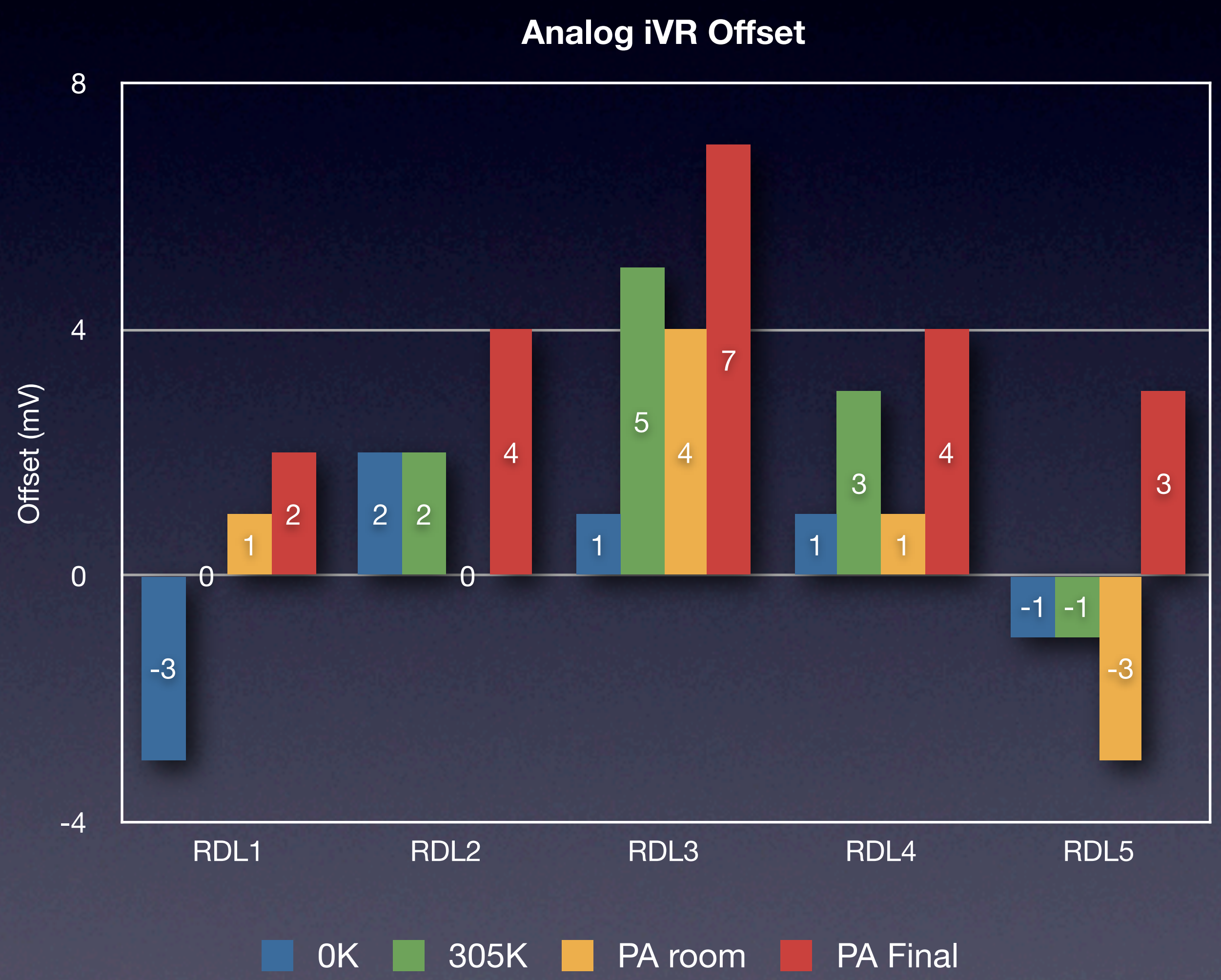


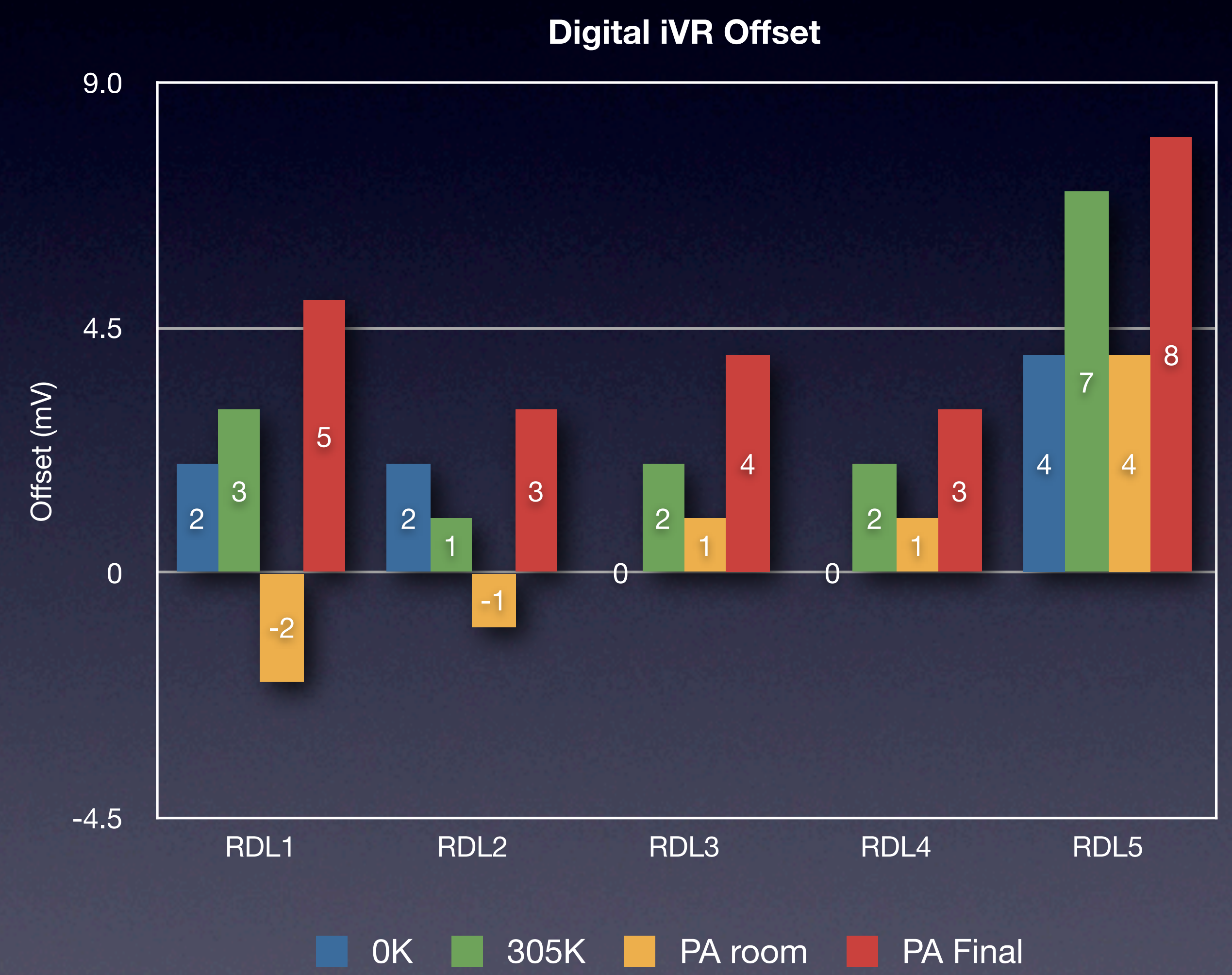
Digital Power Supply Voltage Regulator



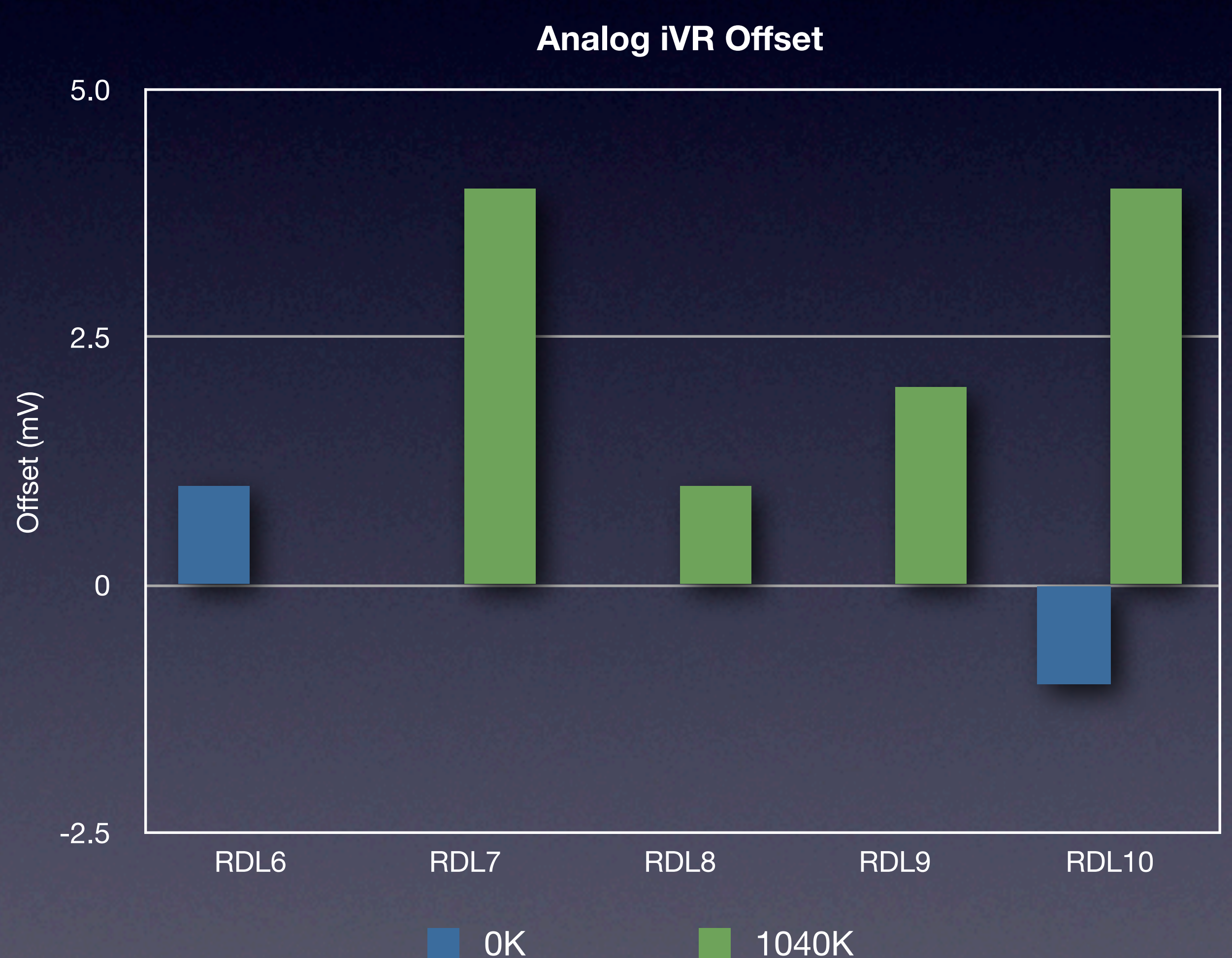
- Offset shows the error in the generated power supply
- 6mV of offset is well within the ETM's capabilities (10%@2.5V=250mV)

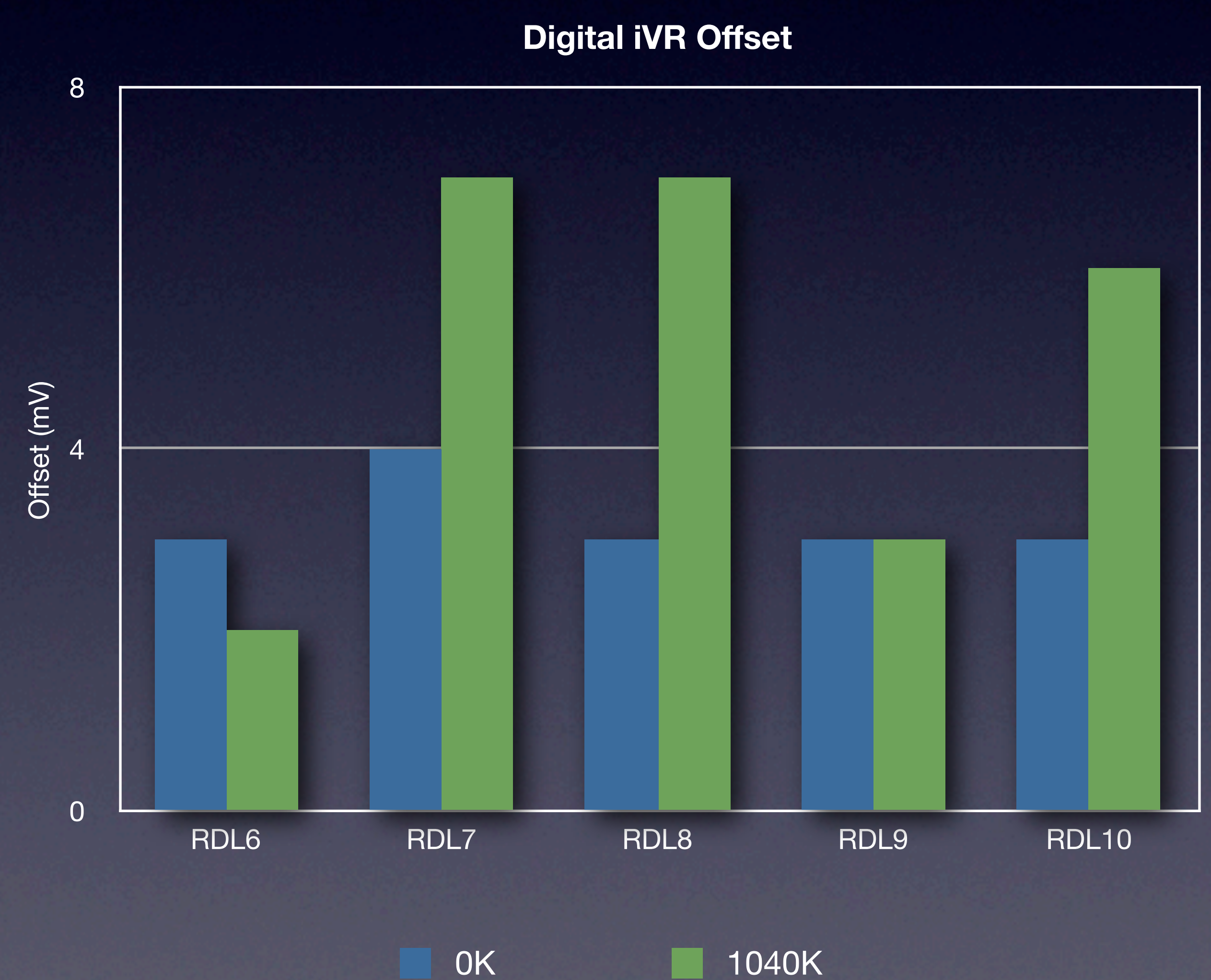
Power Supply Regulator





Power Supply Regulator



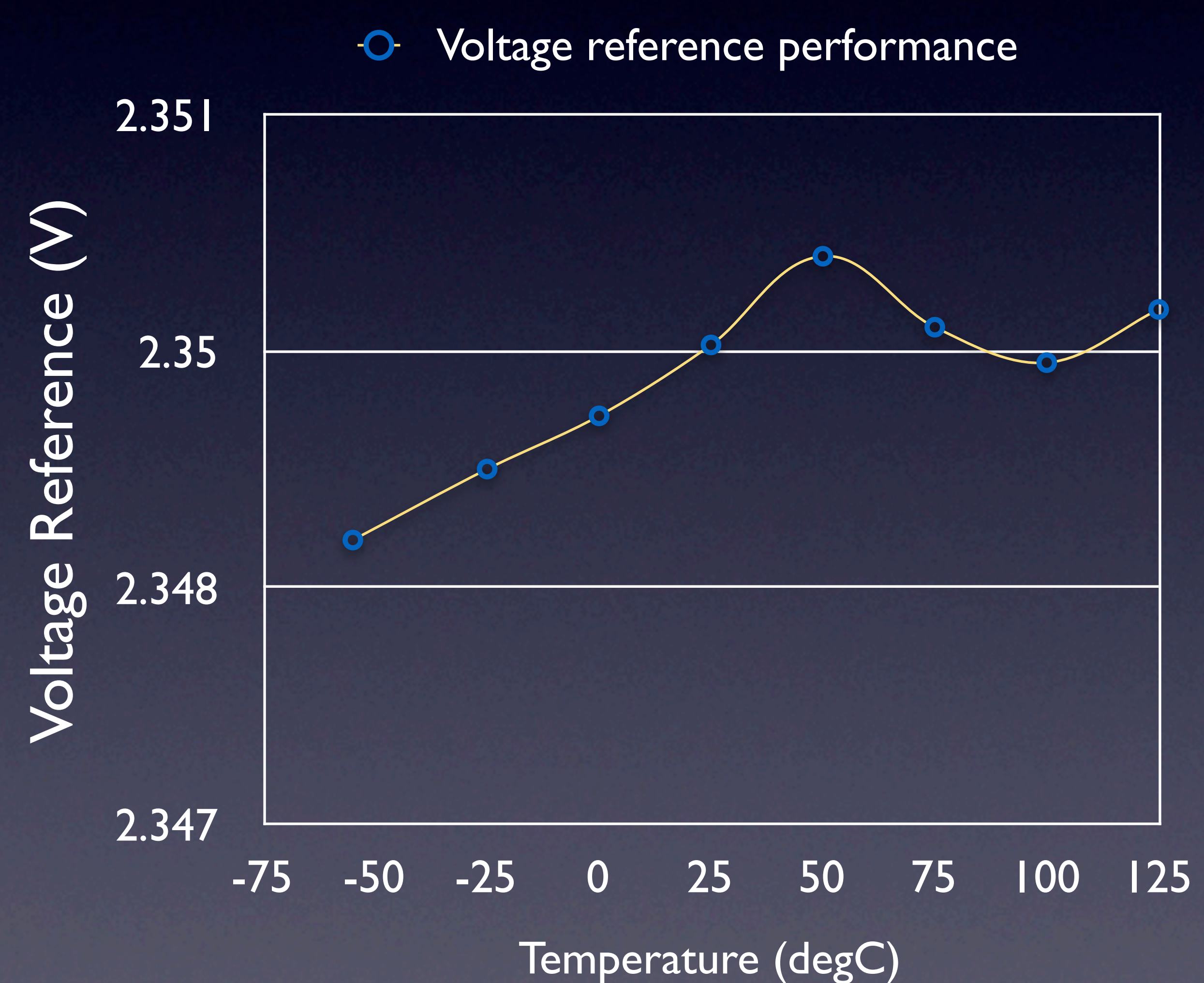


Power Supply Regulator

- Offset between reference and generated power supply <5mV.
  - Very good matching in the amplifier
- DC current driving capability is 70mA
  - At all cases it can power ETM2 device (STD/CAN Temp Measurement,etc)
  - After TID it is still higher than 60mA
- Can support clock speeds above 32 MHz.
- Efficiency close to 90%.
- Separated structure for digital and analog core power supplies reduces noise on the analog power supply.

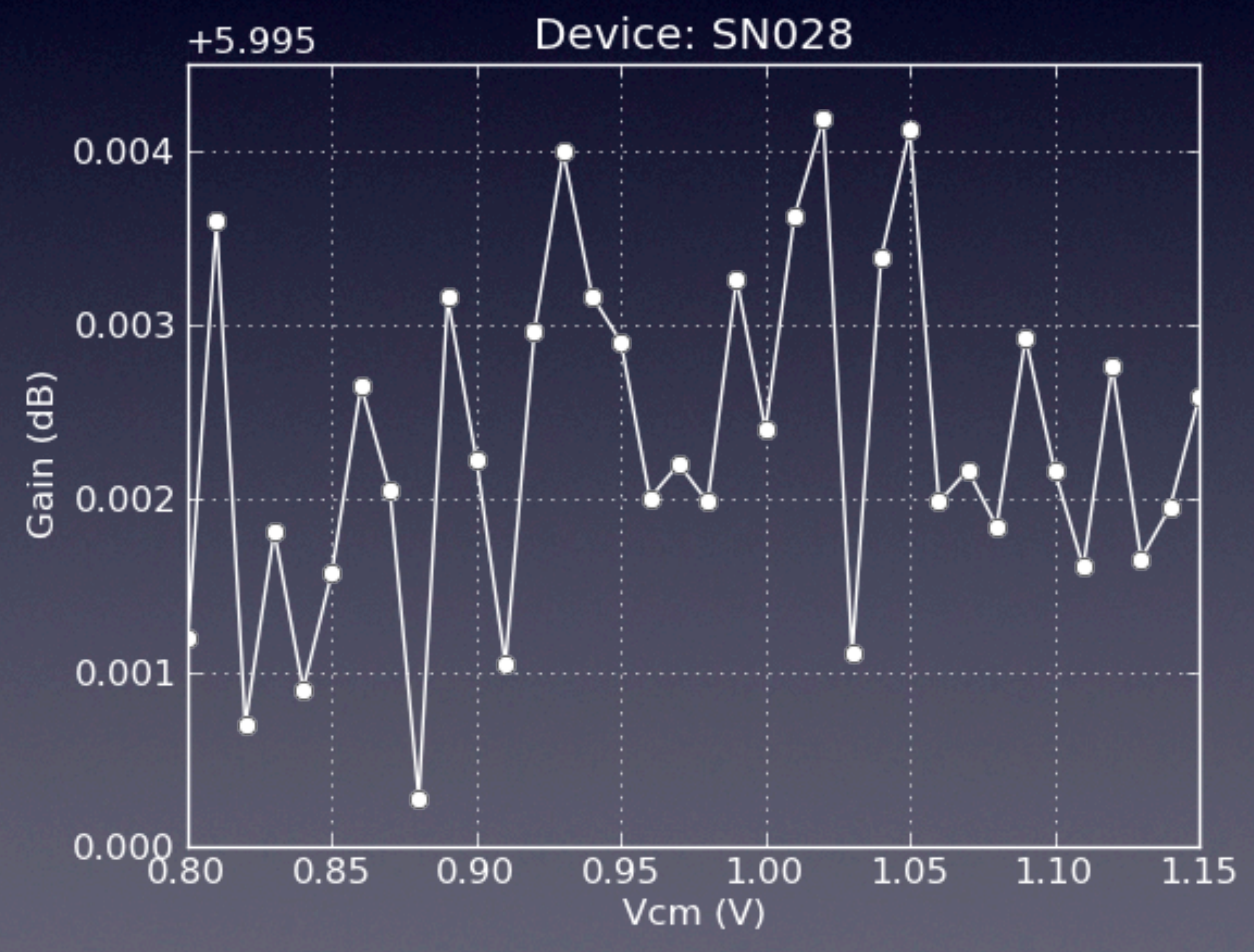
Voltage Reference

- ETM has an on chip voltage second order temperature compensated voltage reference which can be by passed if the user want to.
- Voltage reference power is 1.8mW
  - Optimized value for increased TID hardness
  - TID performance of voltage reference is dependent on the current density of the bipolar transistors
- Power supply rejection >84dB up to 100KHz



Voltage Reference Amplification

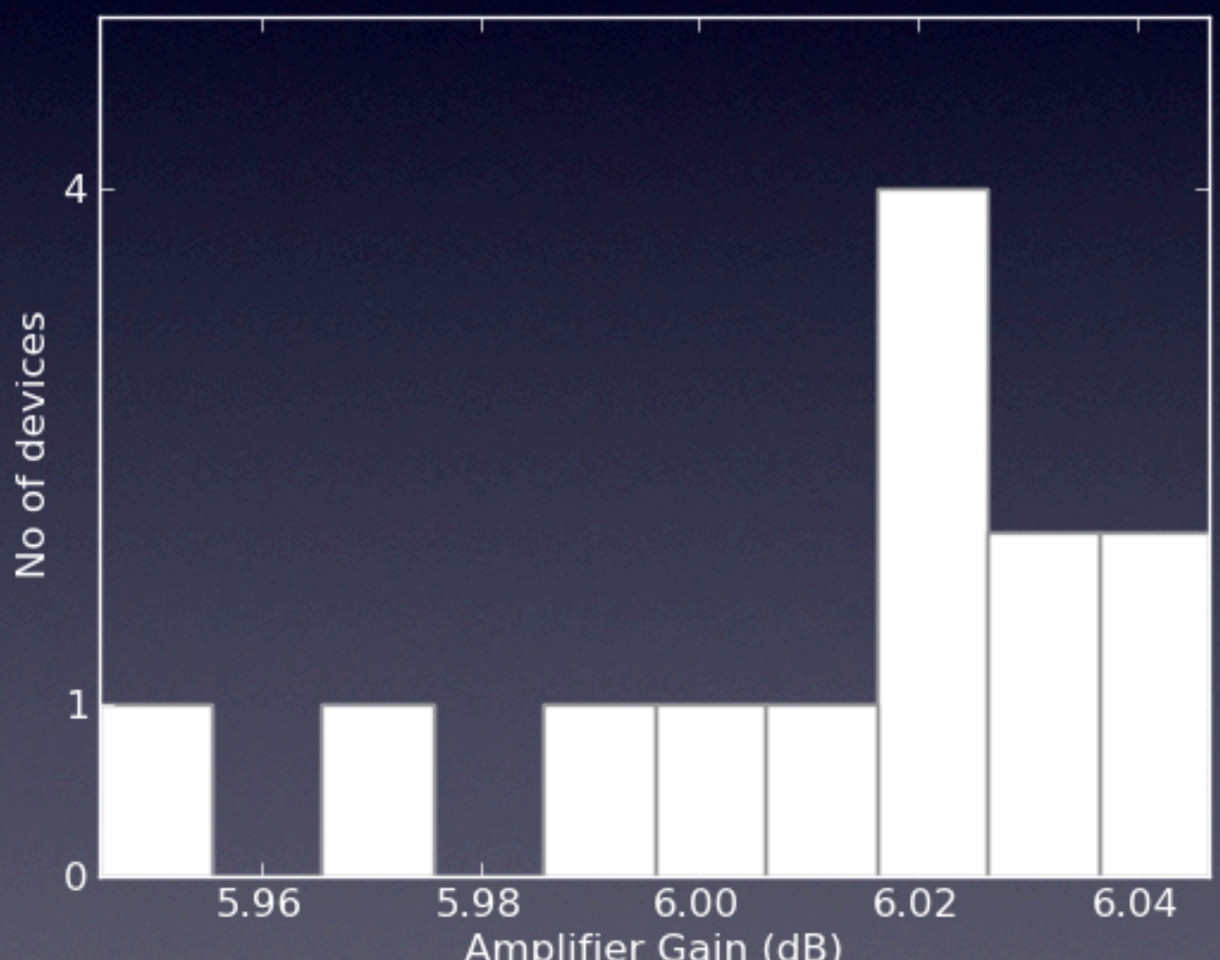
Gain Stability versus Input



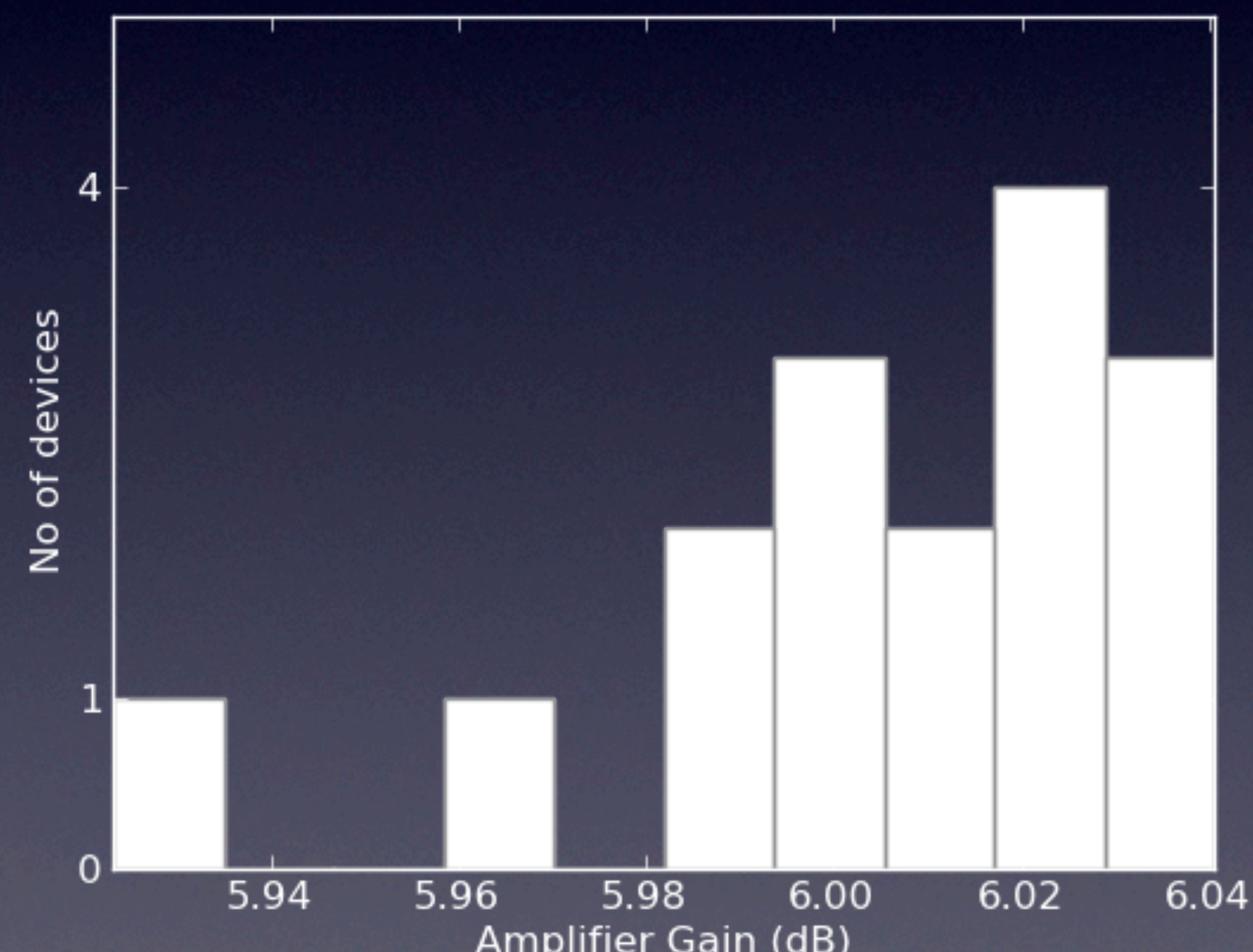
The amplification unit can be used for amplifying an external voltage reference (if needed)

Voltage Reference Amplification

Assembly lot 1145



Assembly lot 1203

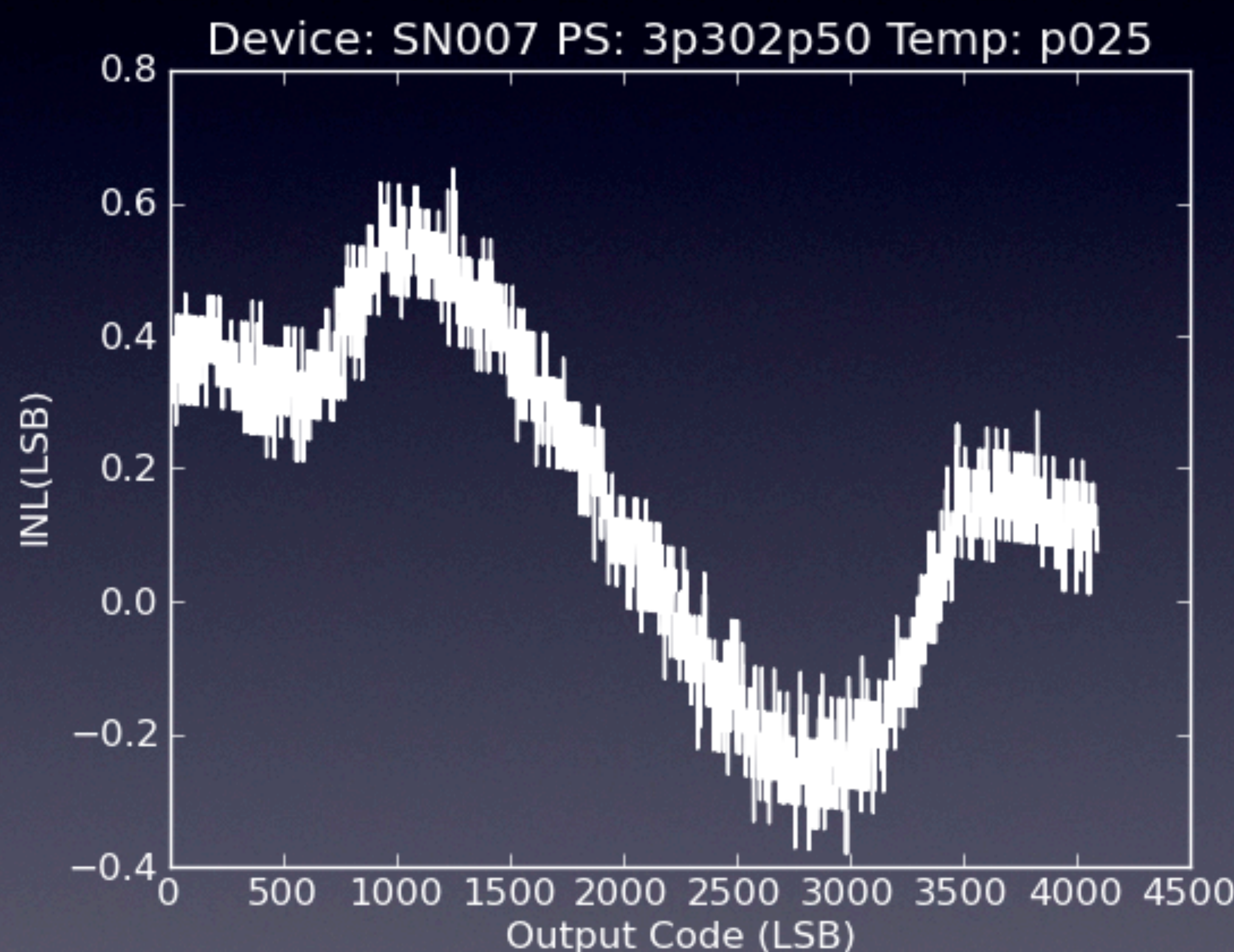


Voltage Reference

- Overall Performance is <15ppm/degC.
- At 300K no big variations
- At 1 MRad performance falls to 20-25ppm/degC
  - More than enough for the ETM application
- User can provide an external one if he wants to

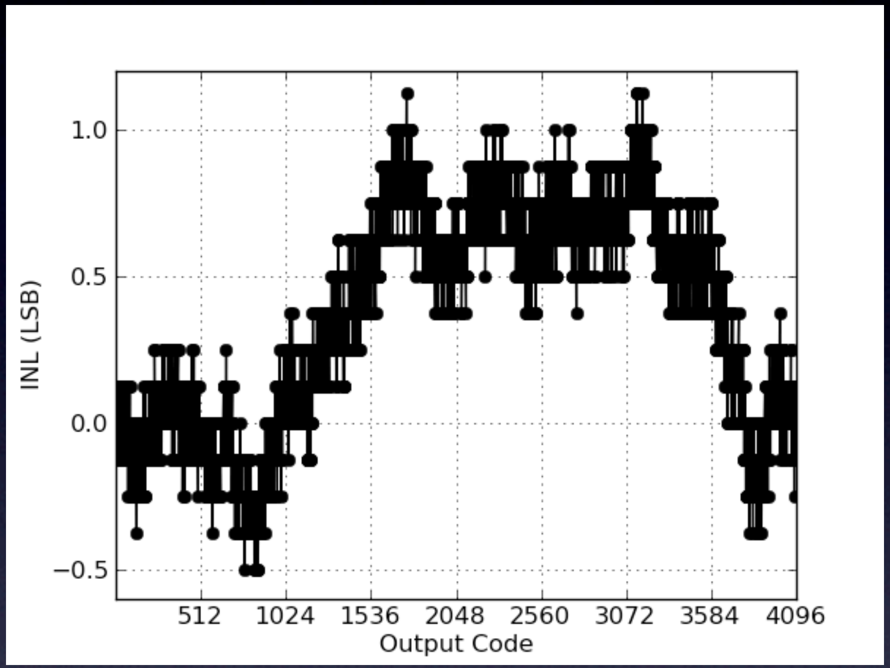
ADC

- SA ADC with a digital auto-zeroing (DAZ) algorithm
- DAZ employes a second conversion to remove comparator offset at the speed of reducing the sampling speed
- DAZ is employed only at TID levels above 300 KRad
- Typical ADC INL curve
- Residue is from resistive ladder mismatch
- Comparator offset is minimal

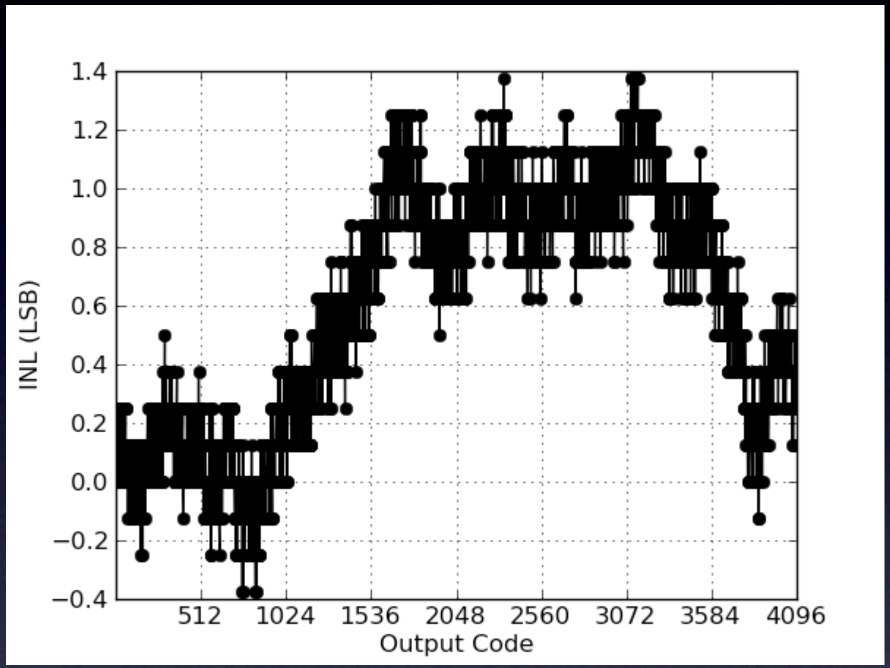


TID Performance of the ADC

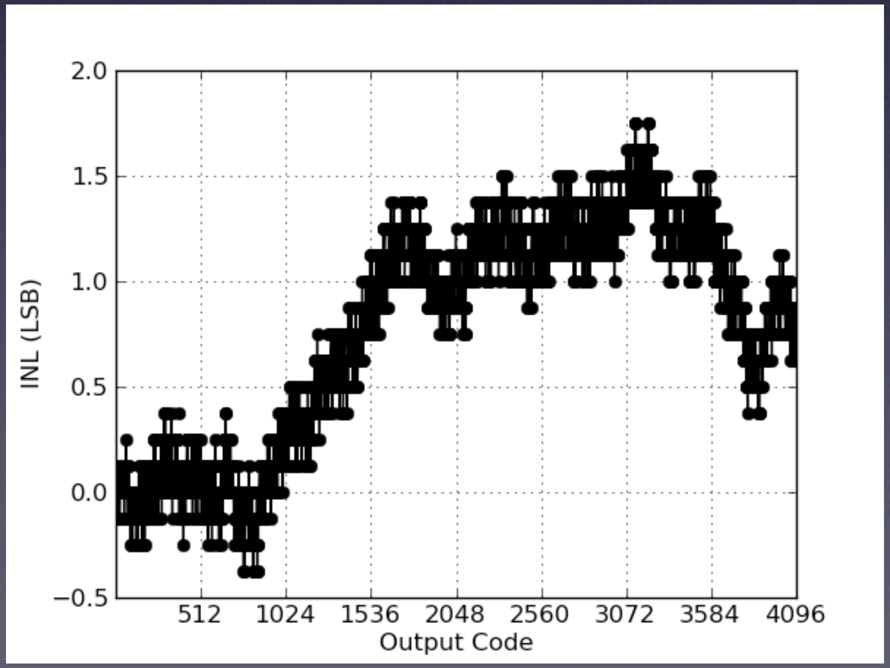
Pre-RAD



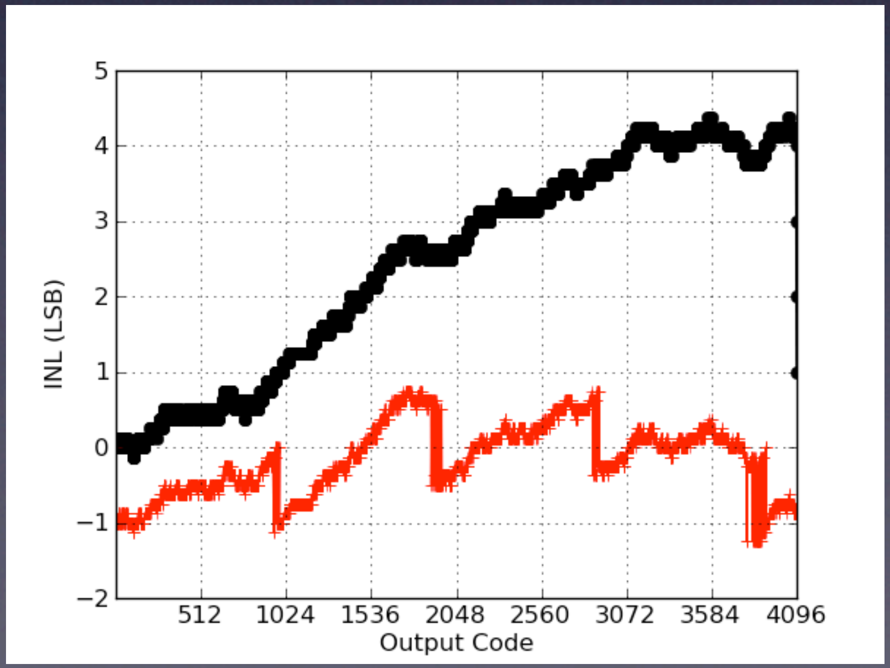
100 KRad



300 KRad

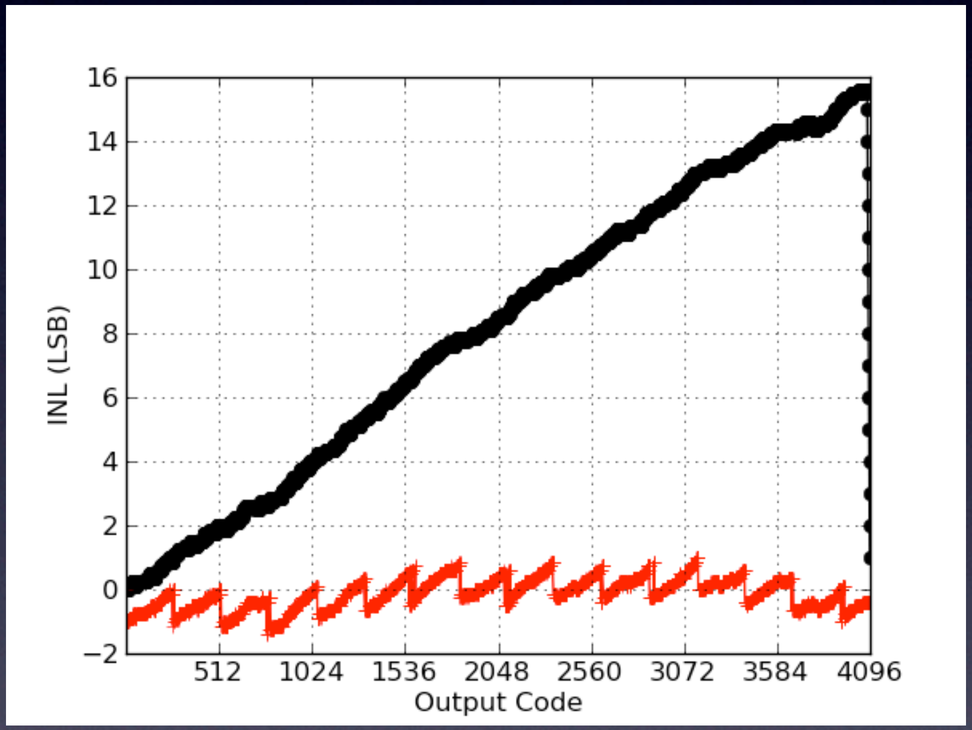


1000 KRad

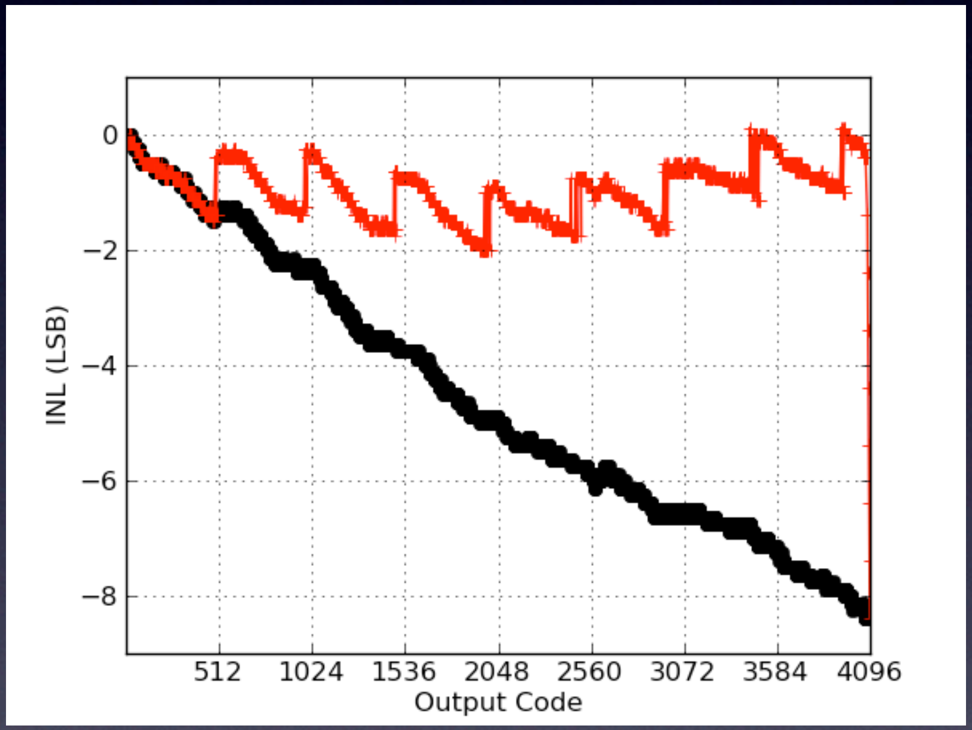


Red is INL with DAZ

TID Performance of the ADC



Red is INL with DAZ



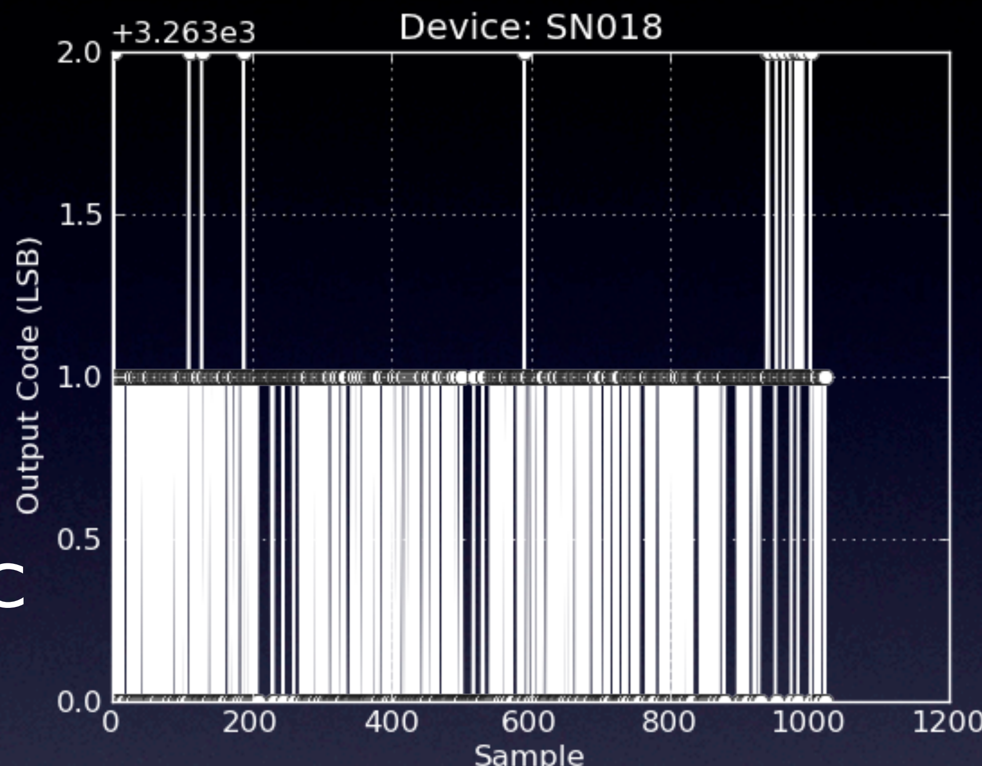
Red is INL with DAZ

TID Performance of the ADC

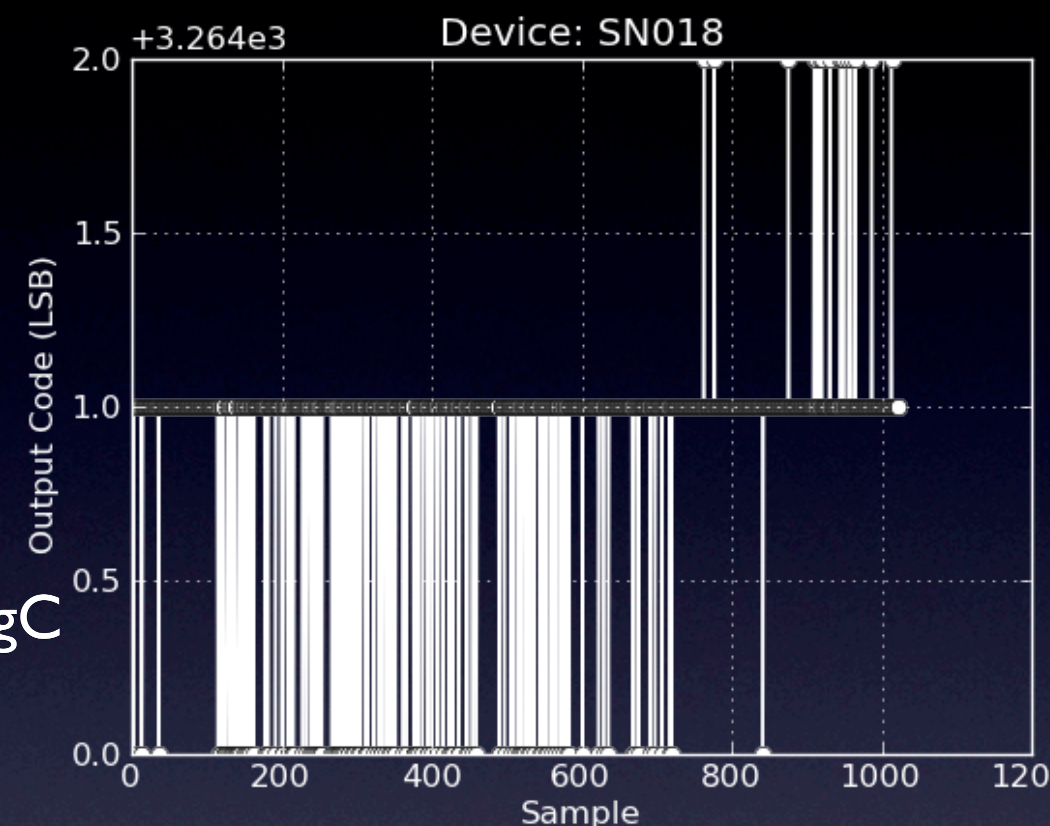
	300K	1040K
INL drift with DAZ OFF	<1	>20
INL drift with DAZ ON	<1	1

ADC performance in the mixed signal environment

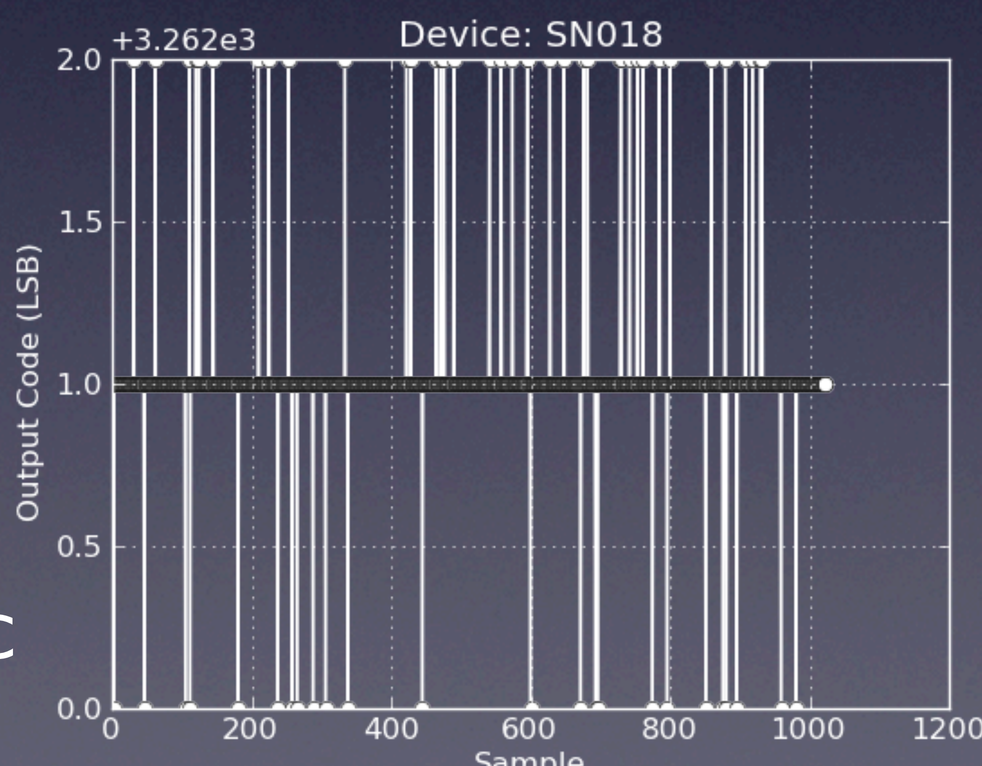
-55degC



125degC



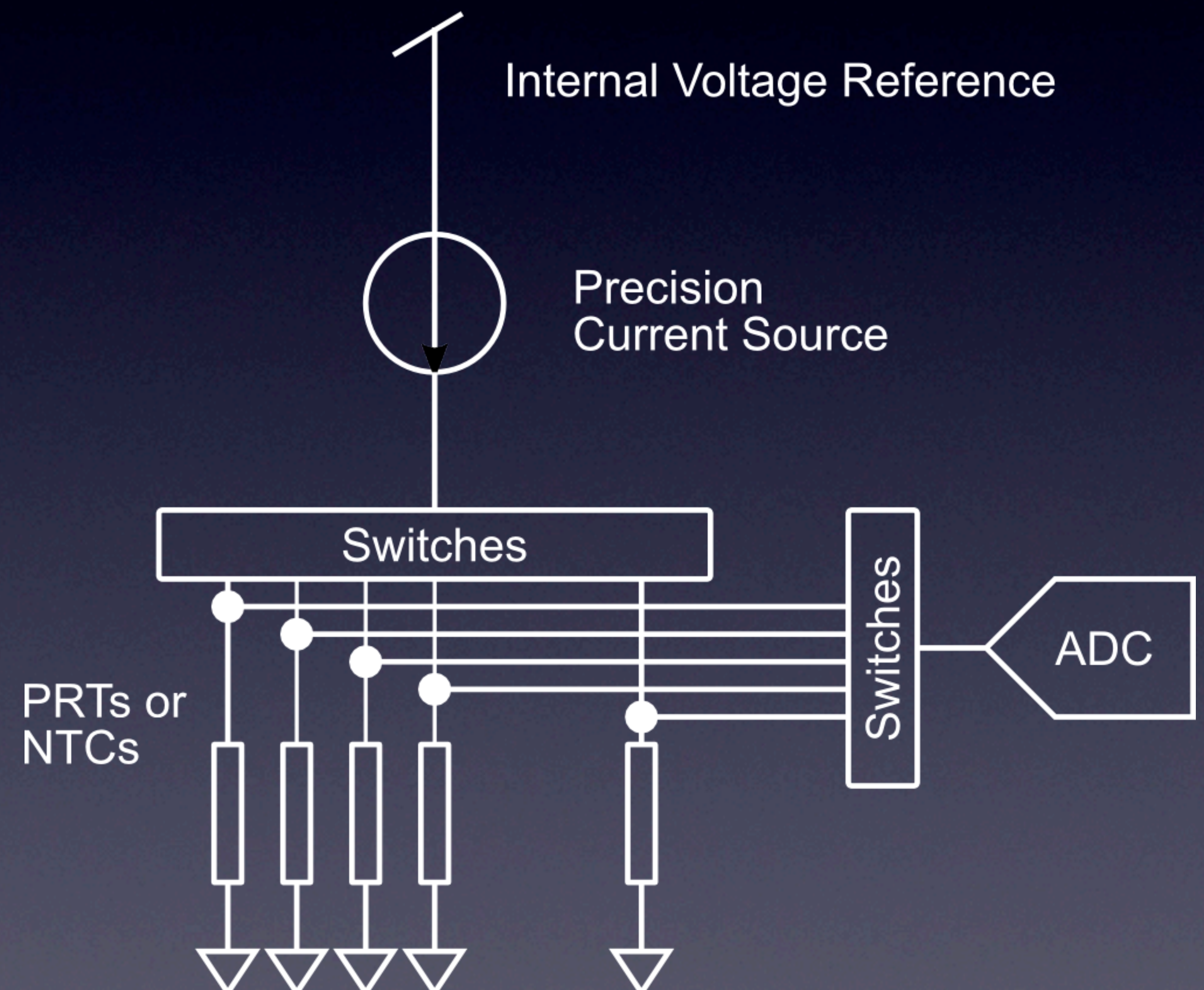
25degC



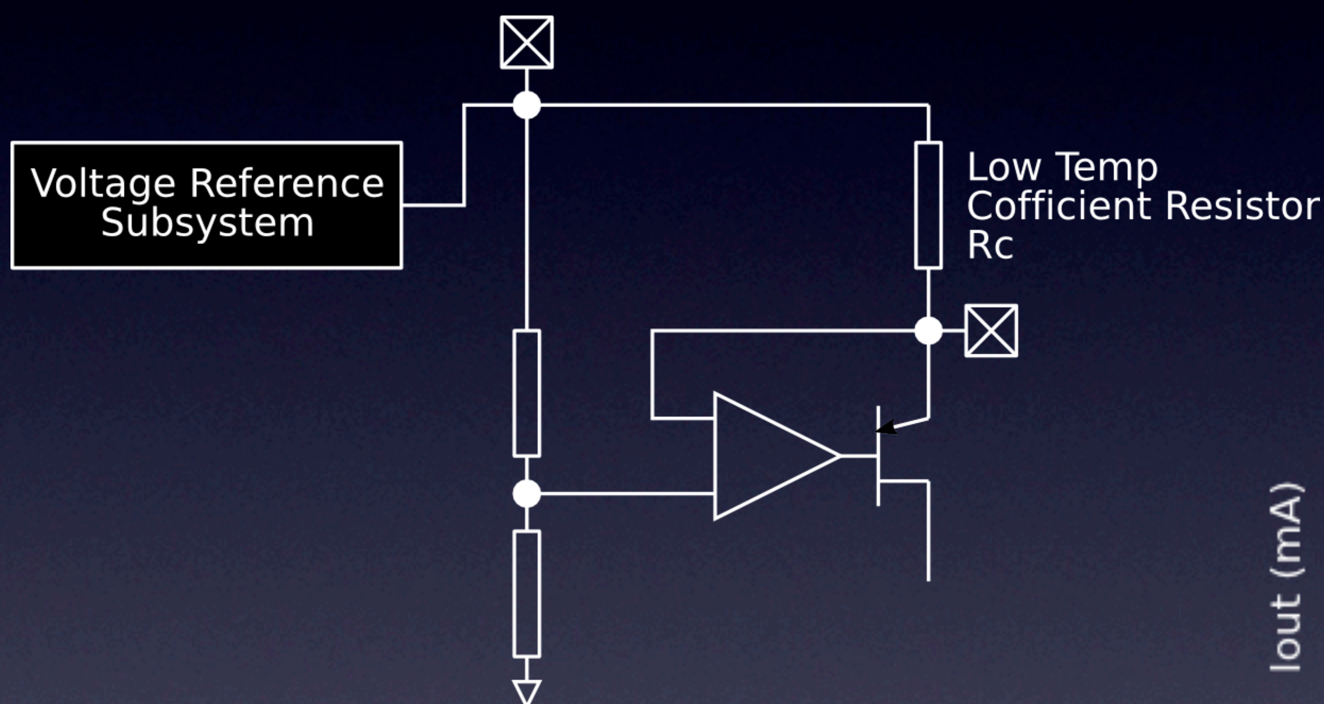
- Code Stability
- Sample Interval: 2ms
- Conf: STD/32MHz
- CSC/RTU have no effect on code stability
- At low T more noisy (3 output codes)

Temperature Measurement

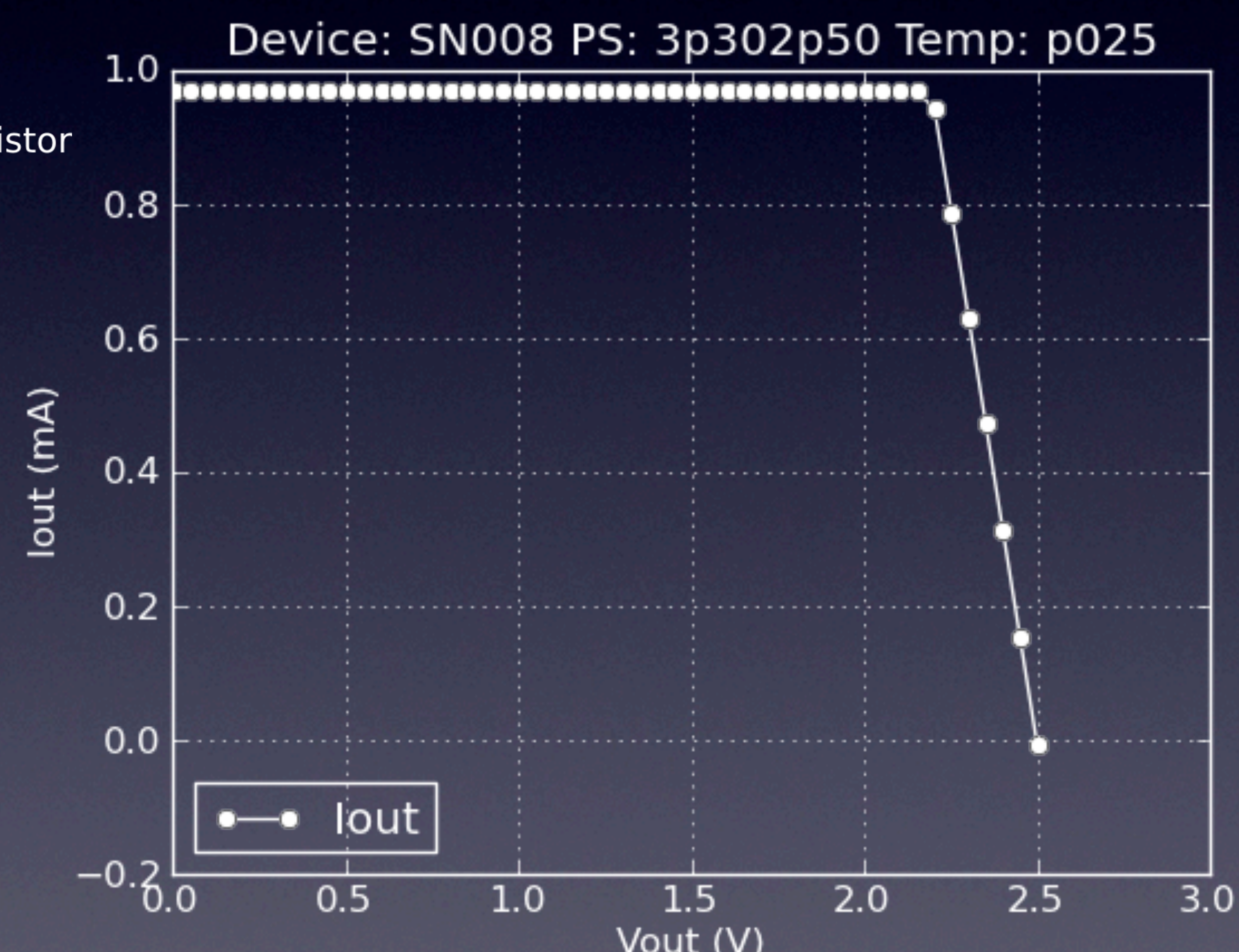
- Current Source used for Temperature Measurements
- Sources a user defined constant current to a PRT
- ADC quantizes the voltage
- Rout of the Current Source is of importance



Temperature Measurement



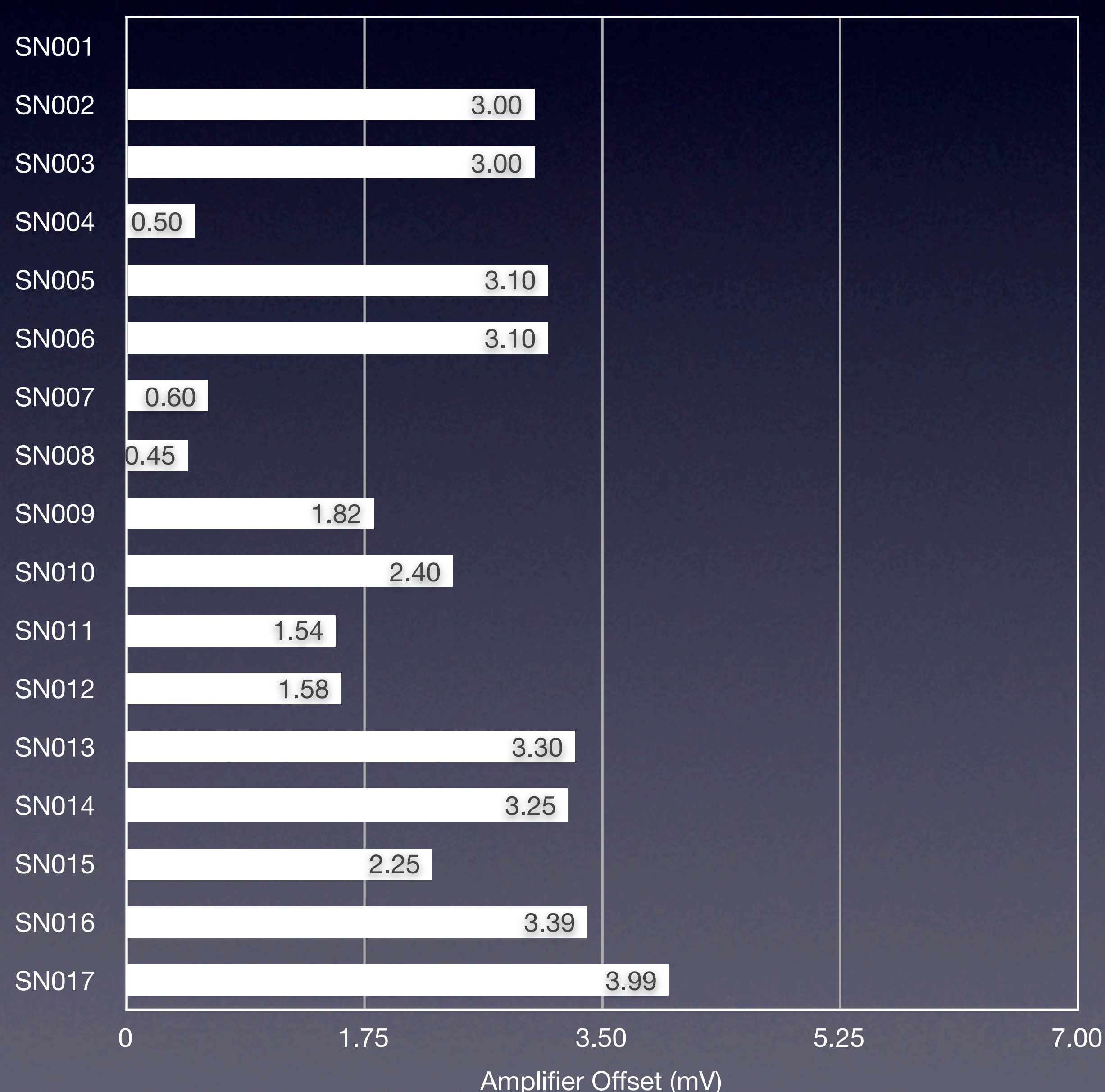
- Rout > 100 MOhm!!!



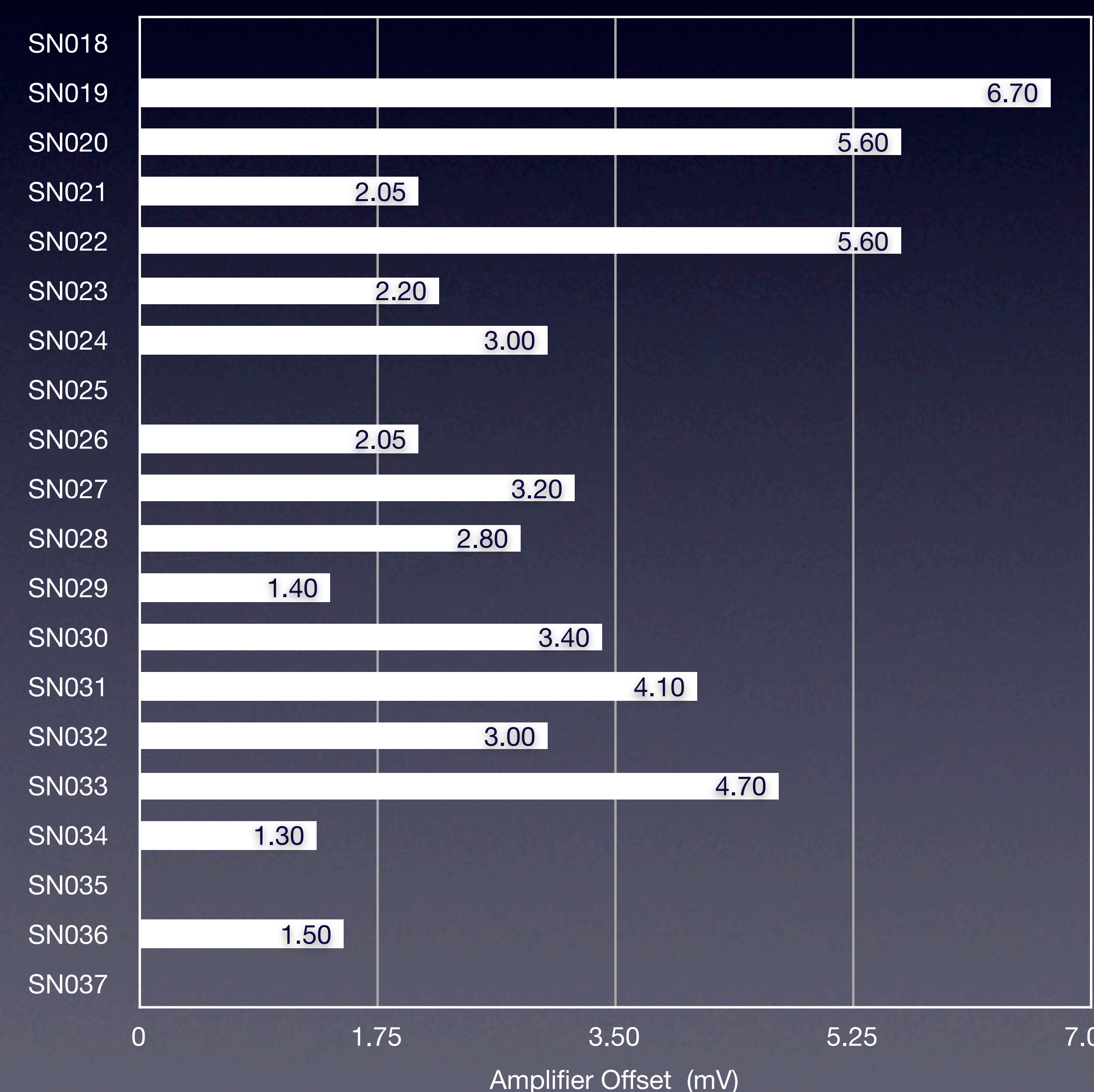
Temperature Measurement

Current Source OpAmp Offset

AS1145

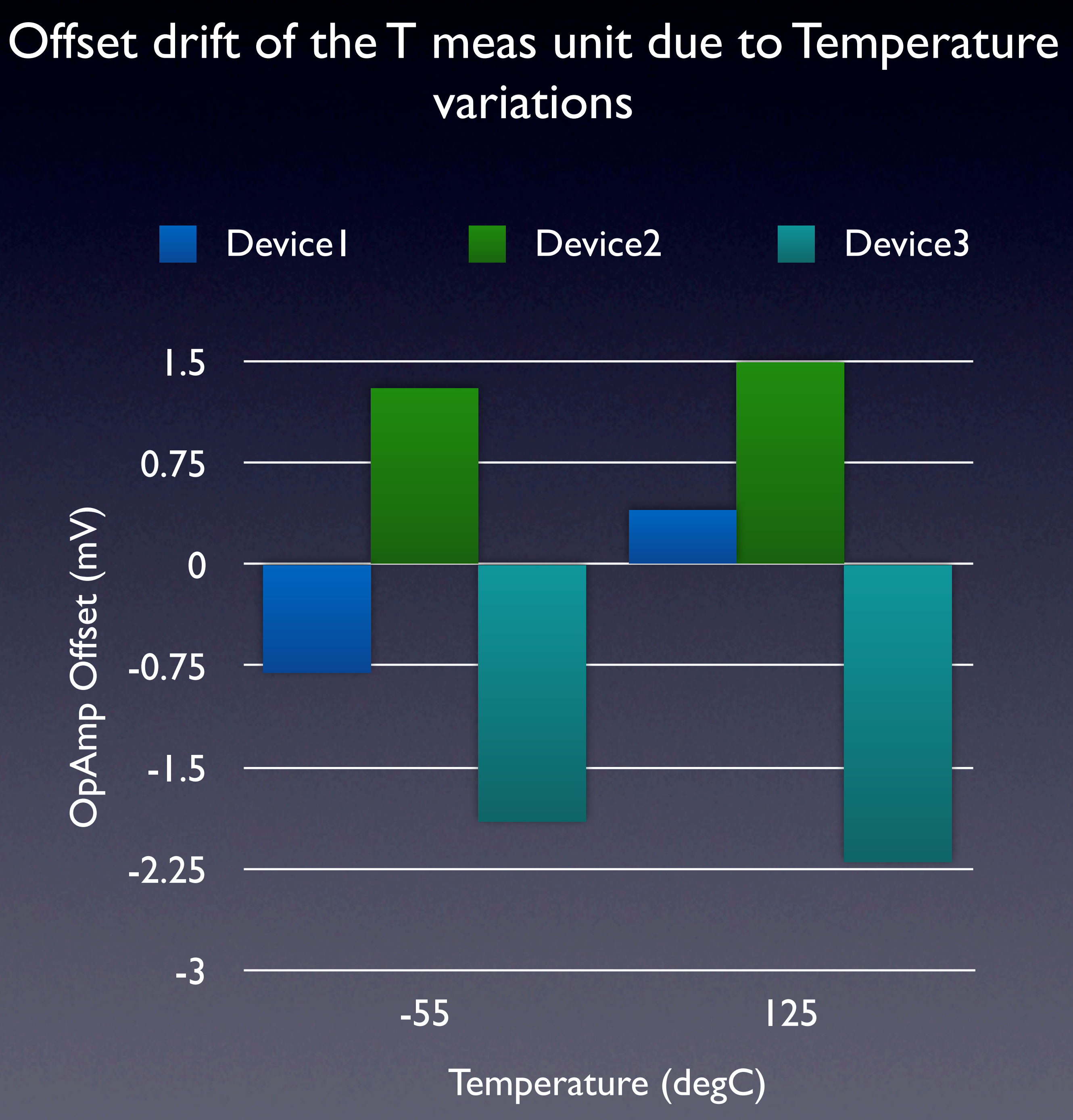


AS1203



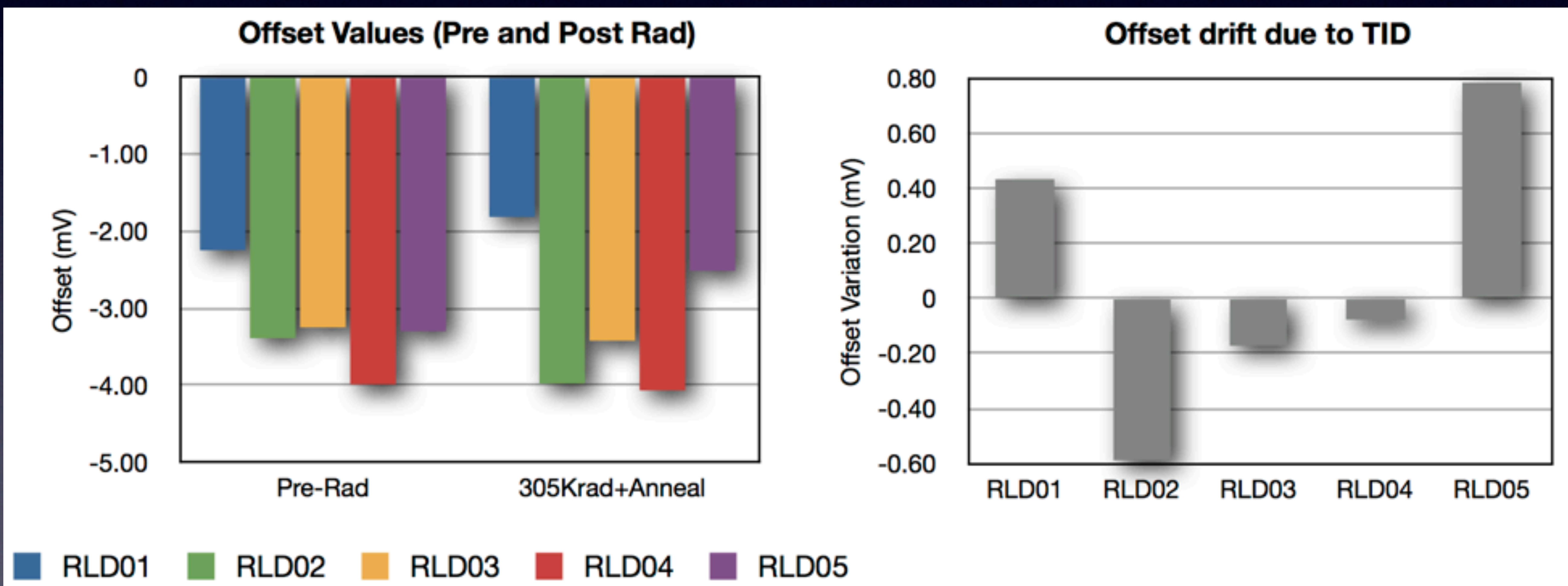
Temperature Effects on the Temperature Measurement Unit

- Drift less than 1mV
- Temperature measurement error less than 0.1degC



Temperature Measurement

- Current Source offset (Pre and post Rad)
- Anneal has no effects



Temperature Measurement

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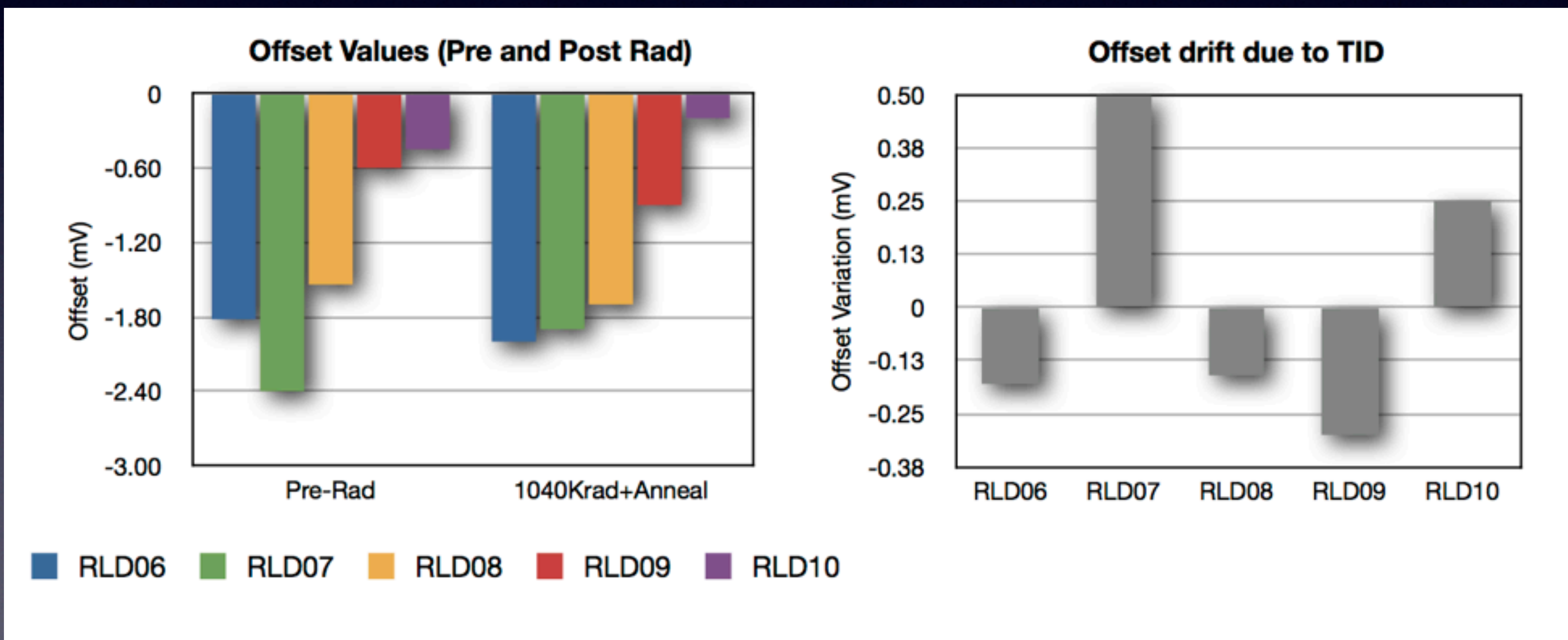
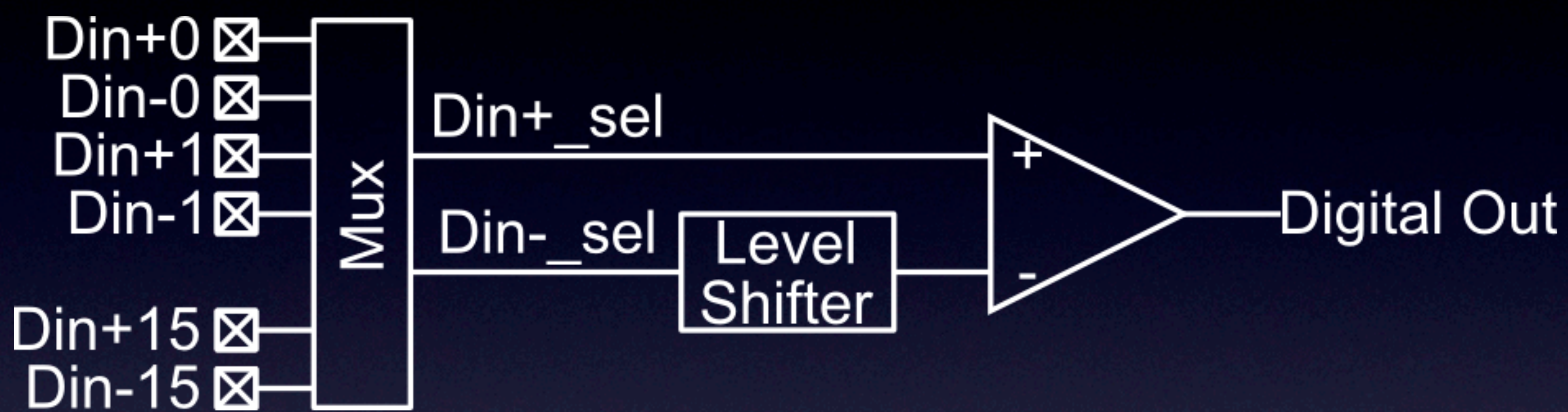


Digital Sampler

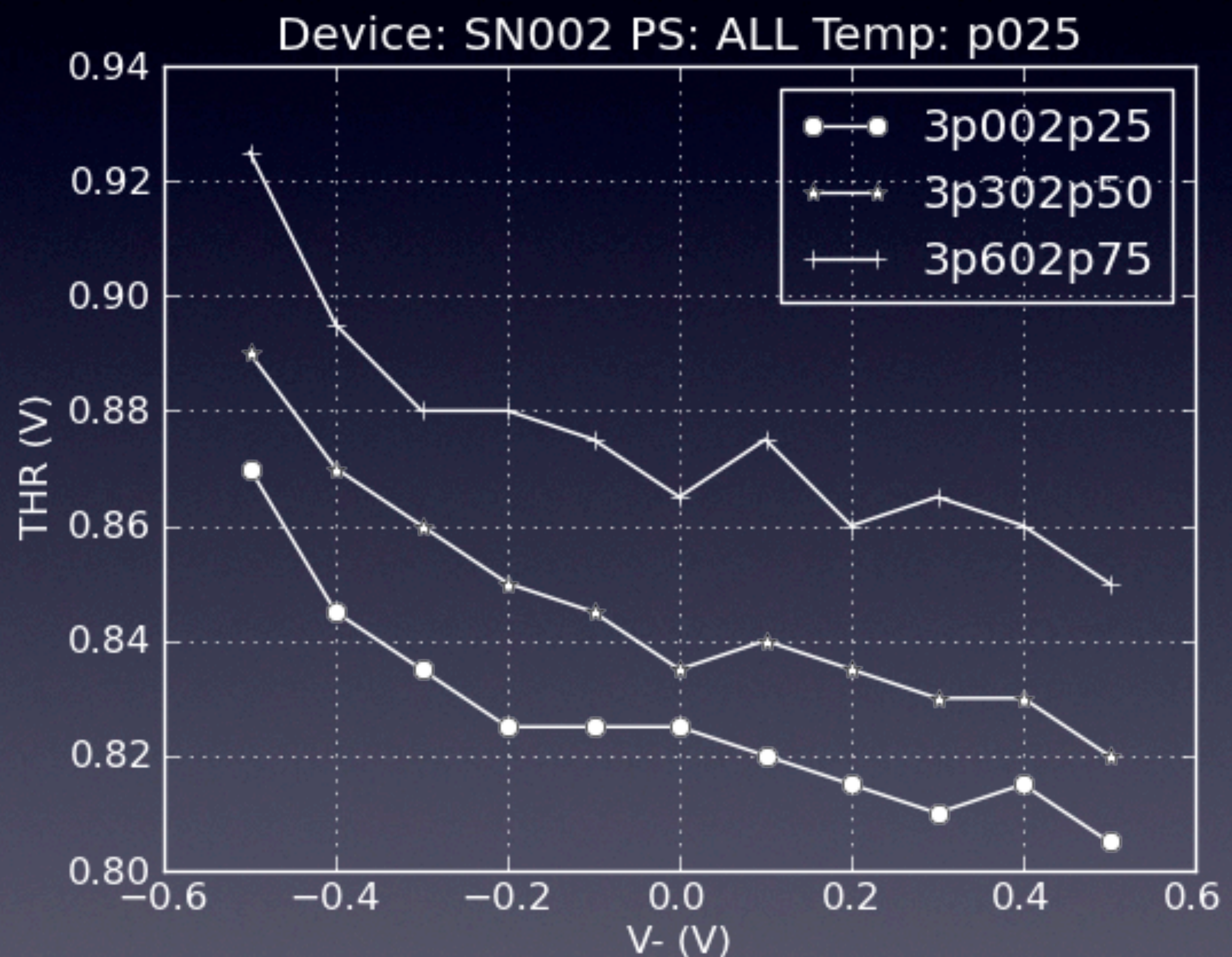


- Level shifter and analog comparator
- Speed is adequate for 64MSPS operation
- Level shifter is a simple p type source follower
- Threshold can be adjusted through the bias voltage of the follower

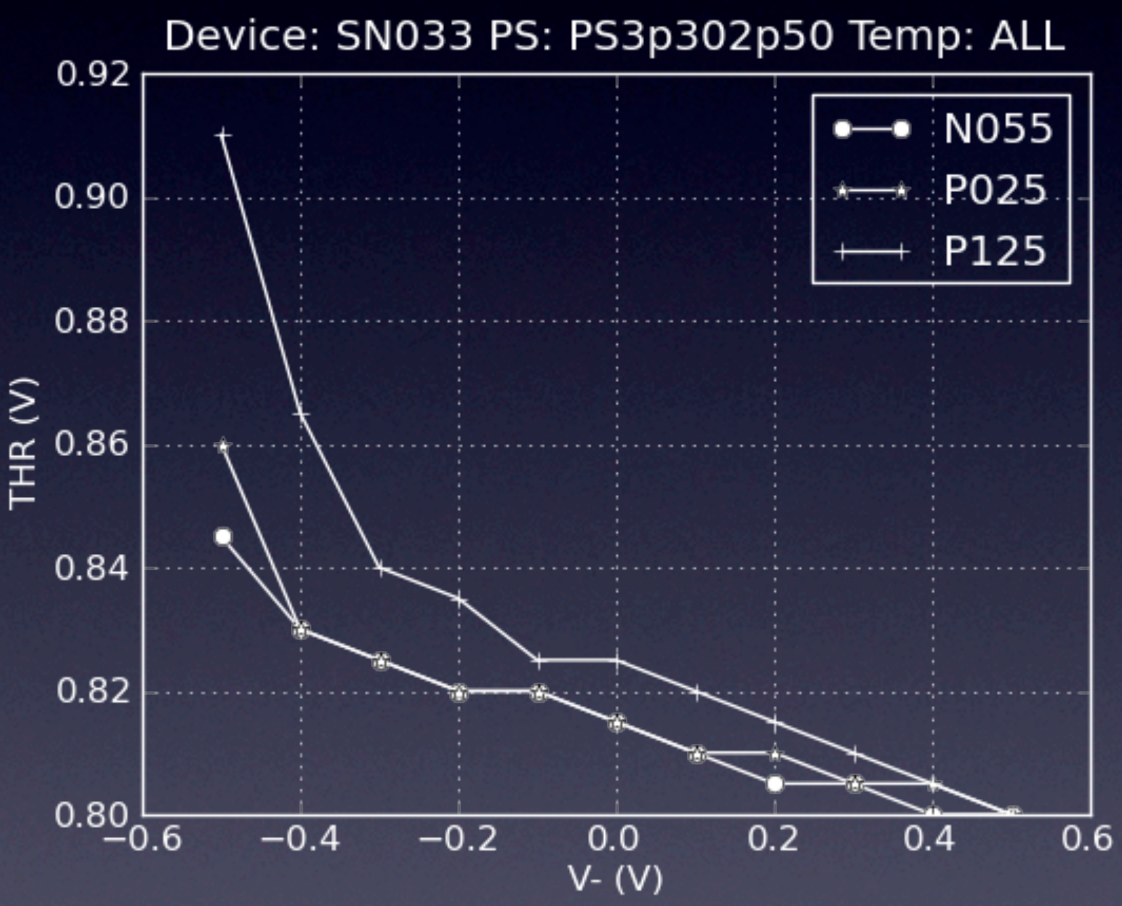
Digital Sampler

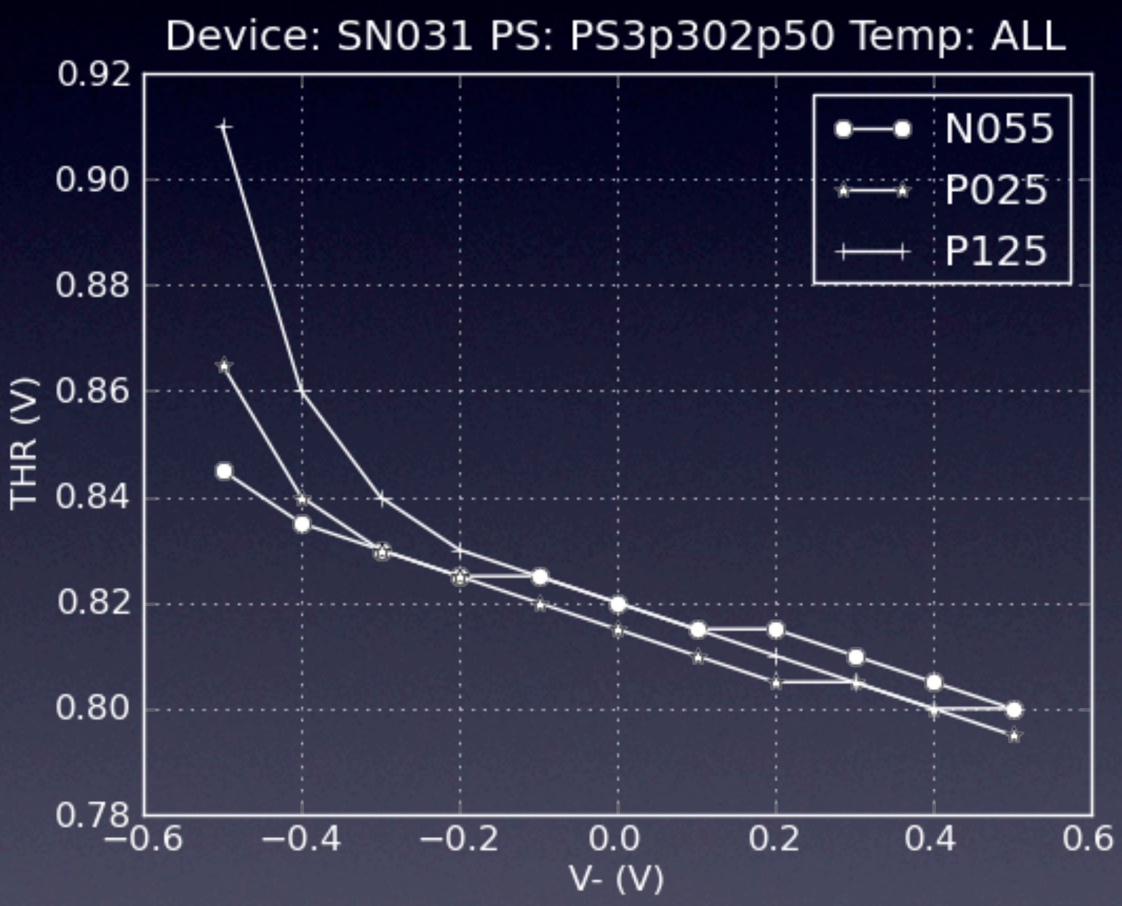
Rbias=47K
Threshold is adjusted through Rbias
If Din_{+} - Din_{-} > THR
then output is high

Power Supply Variation is ~50mV
(acceptable)



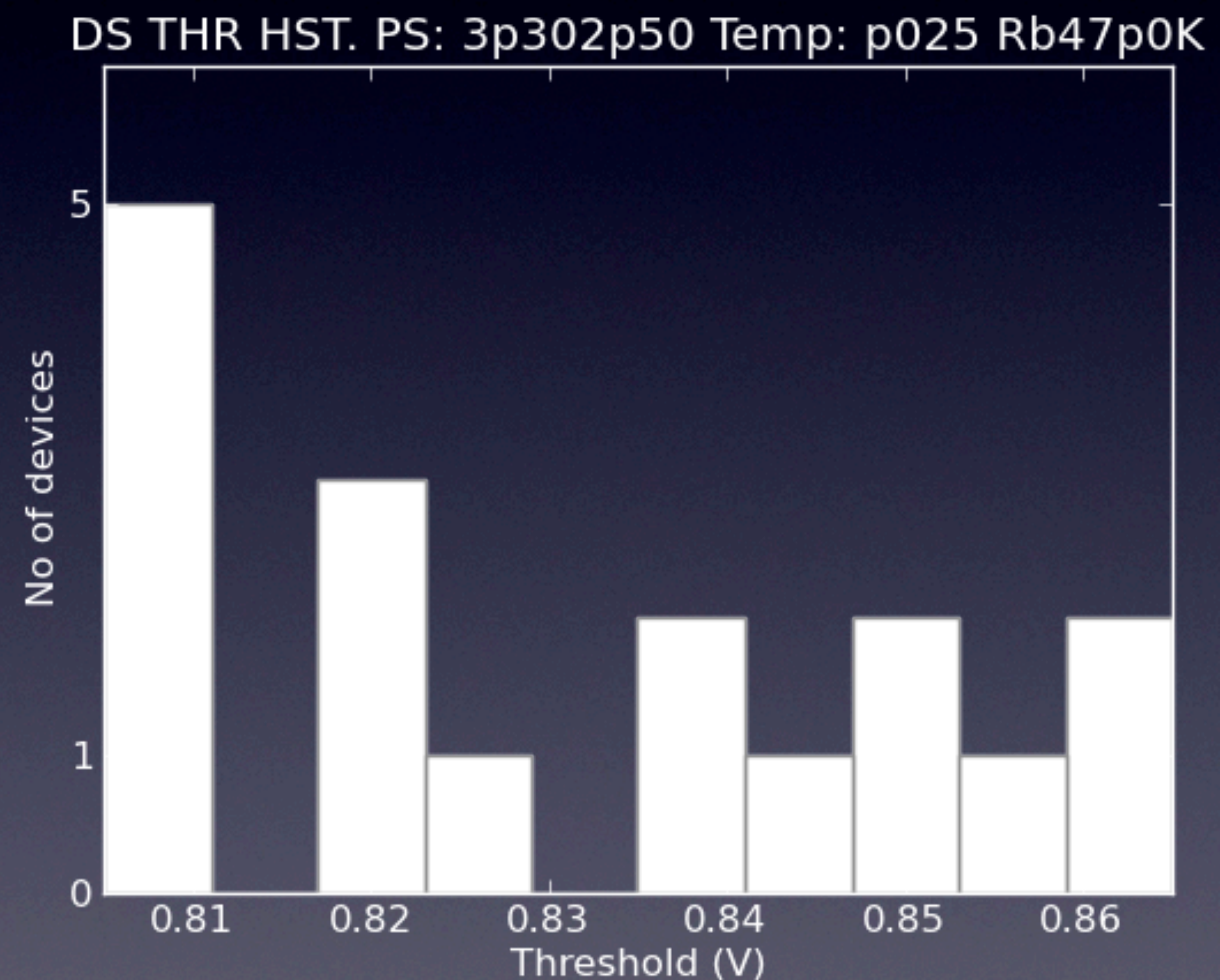
Temperature Effects on the Digital Sampler



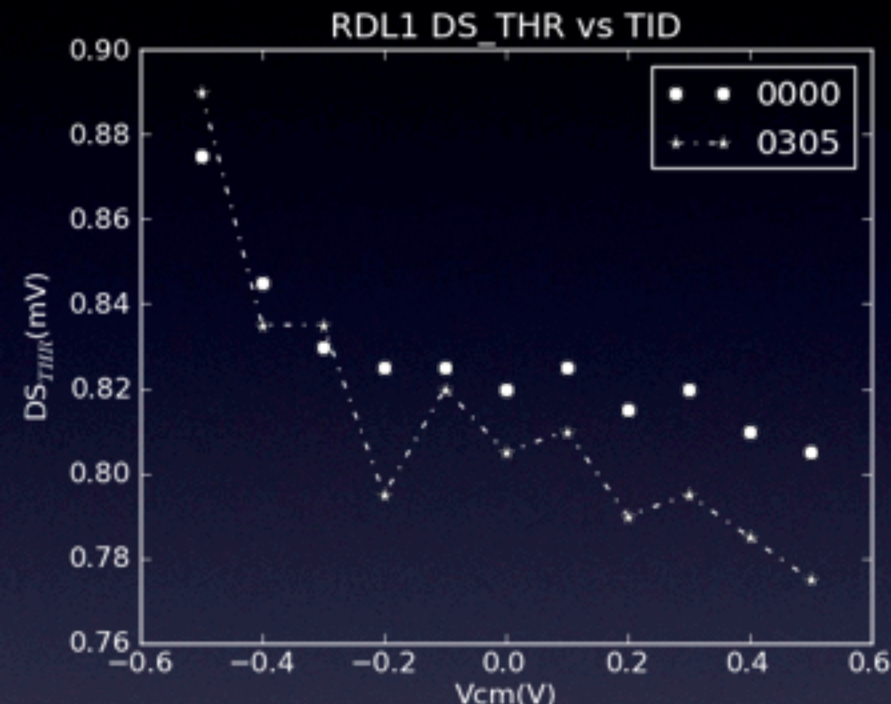


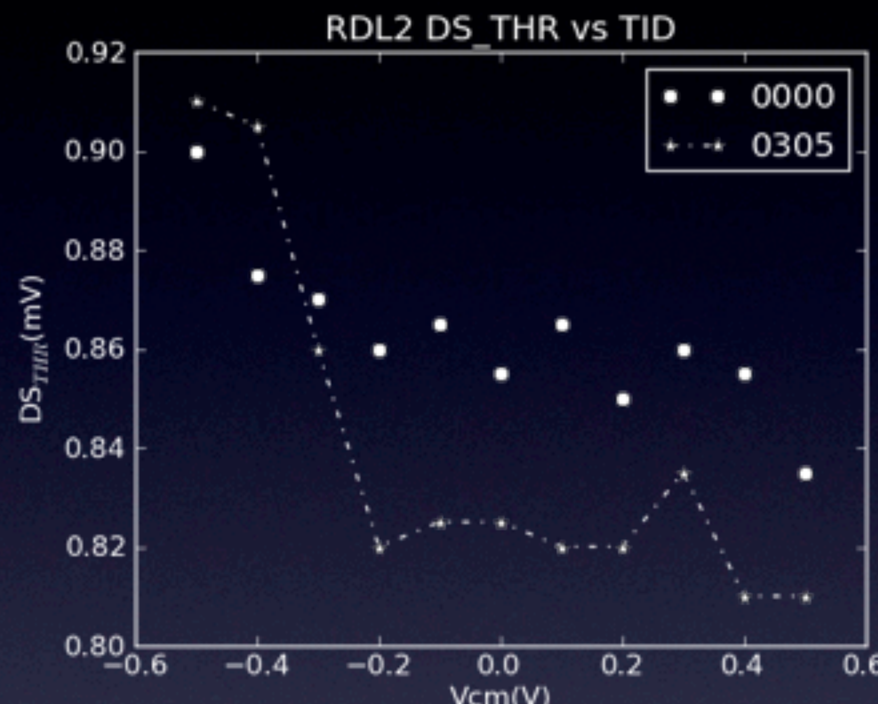
Digital Sampler

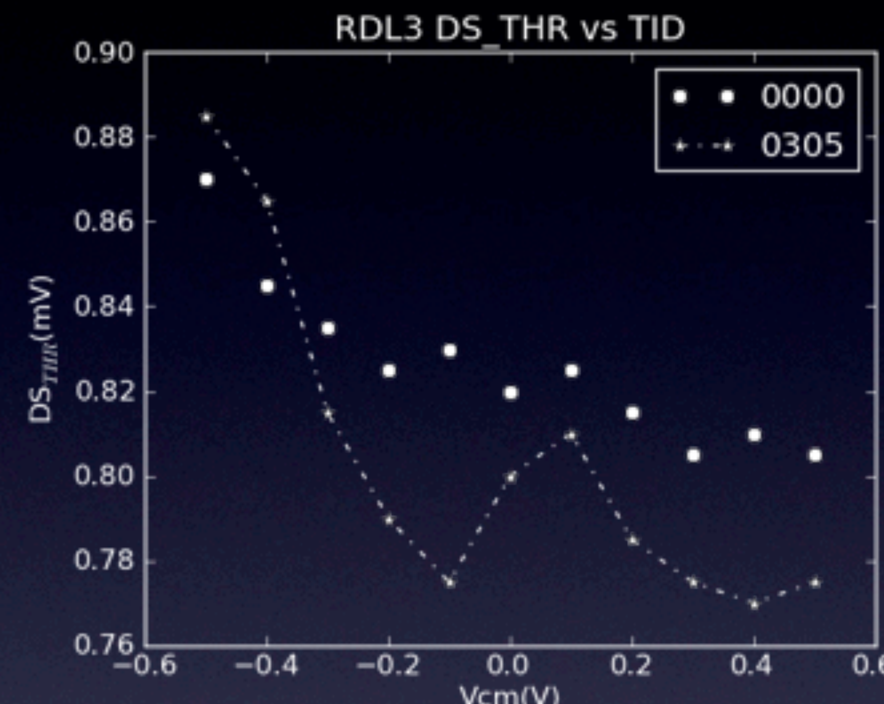
- Device to Device Variation for AS1145
- Variation is 60mV
- No Calibration Tables needed

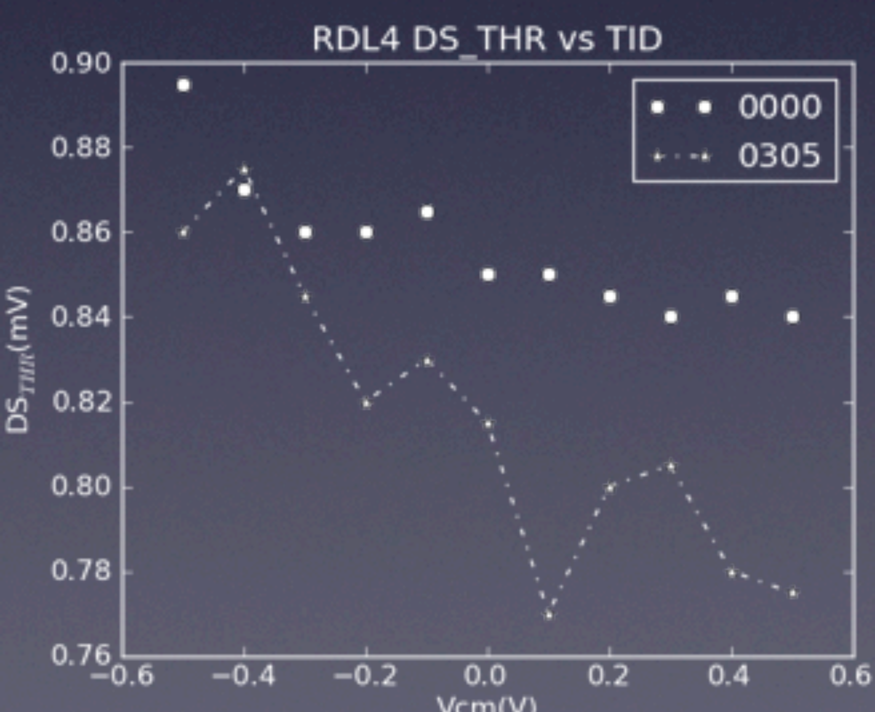


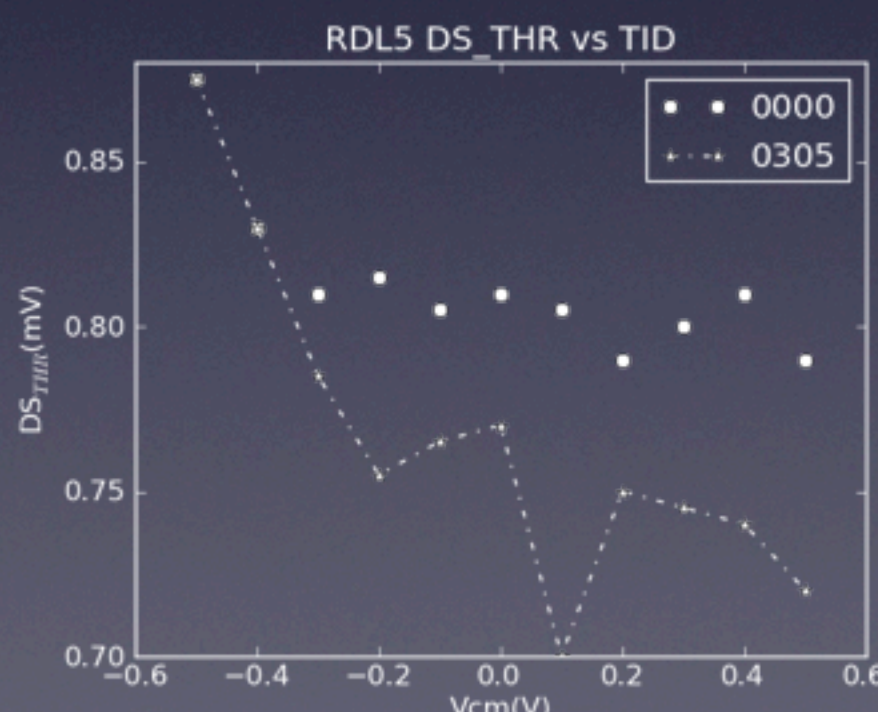
TID Test Campaign





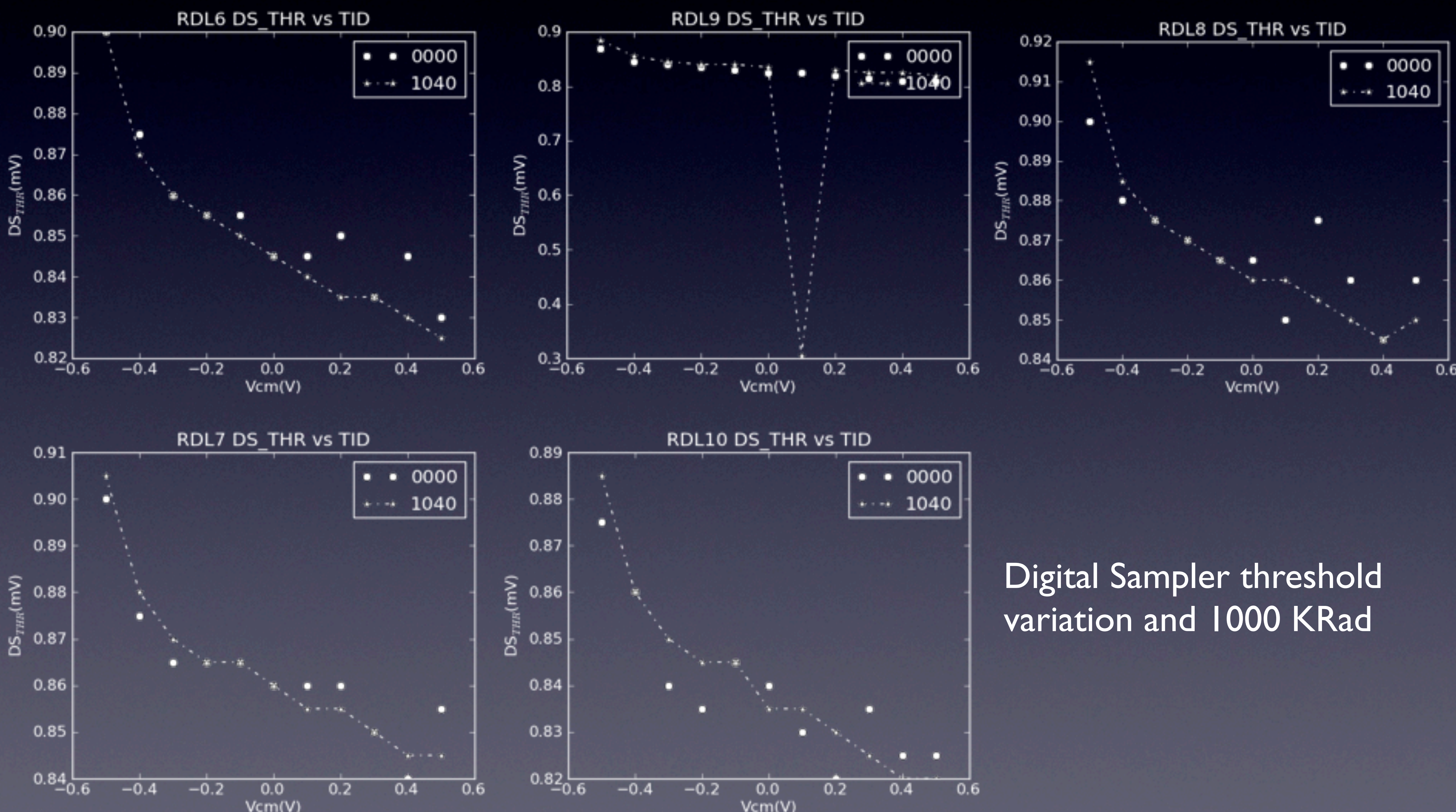






Digital Sampler threshold variation and 300 KRad

TID Test Campaign



Digital Sampler threshold variation and 1000 KRad

Leakage Currents

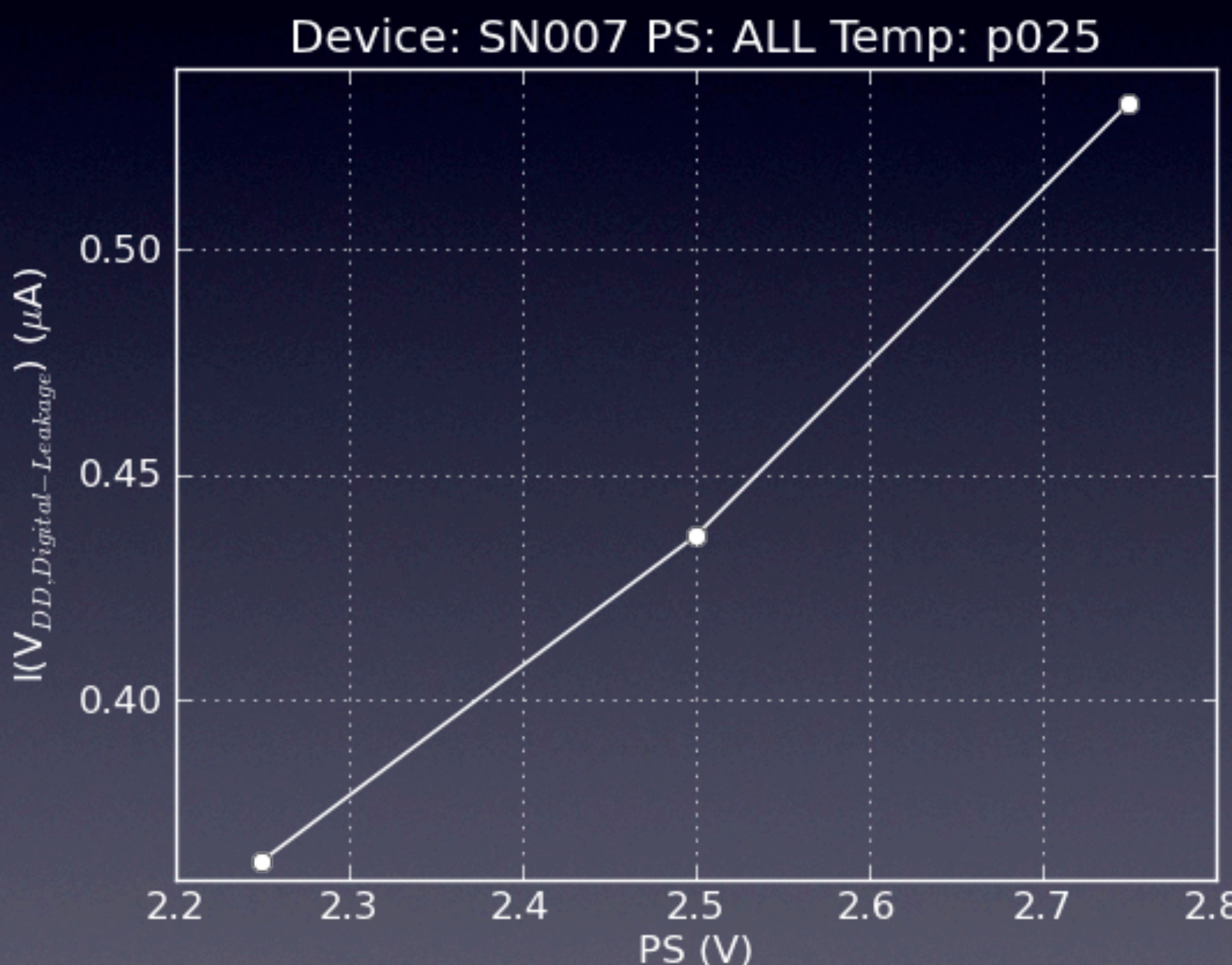
- Digital Leakage Current varies from device to device from 400 to 1500 nA
- Total W of nfets = 177 mm
- Total W of pfets = 531 mm
- Measurement in line with expected values
- ETM is nearly all NAND design (stacking effect factor is high)
- Multifinger layout topology in the drivers

Parameters from IHP

	Ioff (pA/um)	
	Target	Max
Nfet	2.5	100
Pfet	3.5	50

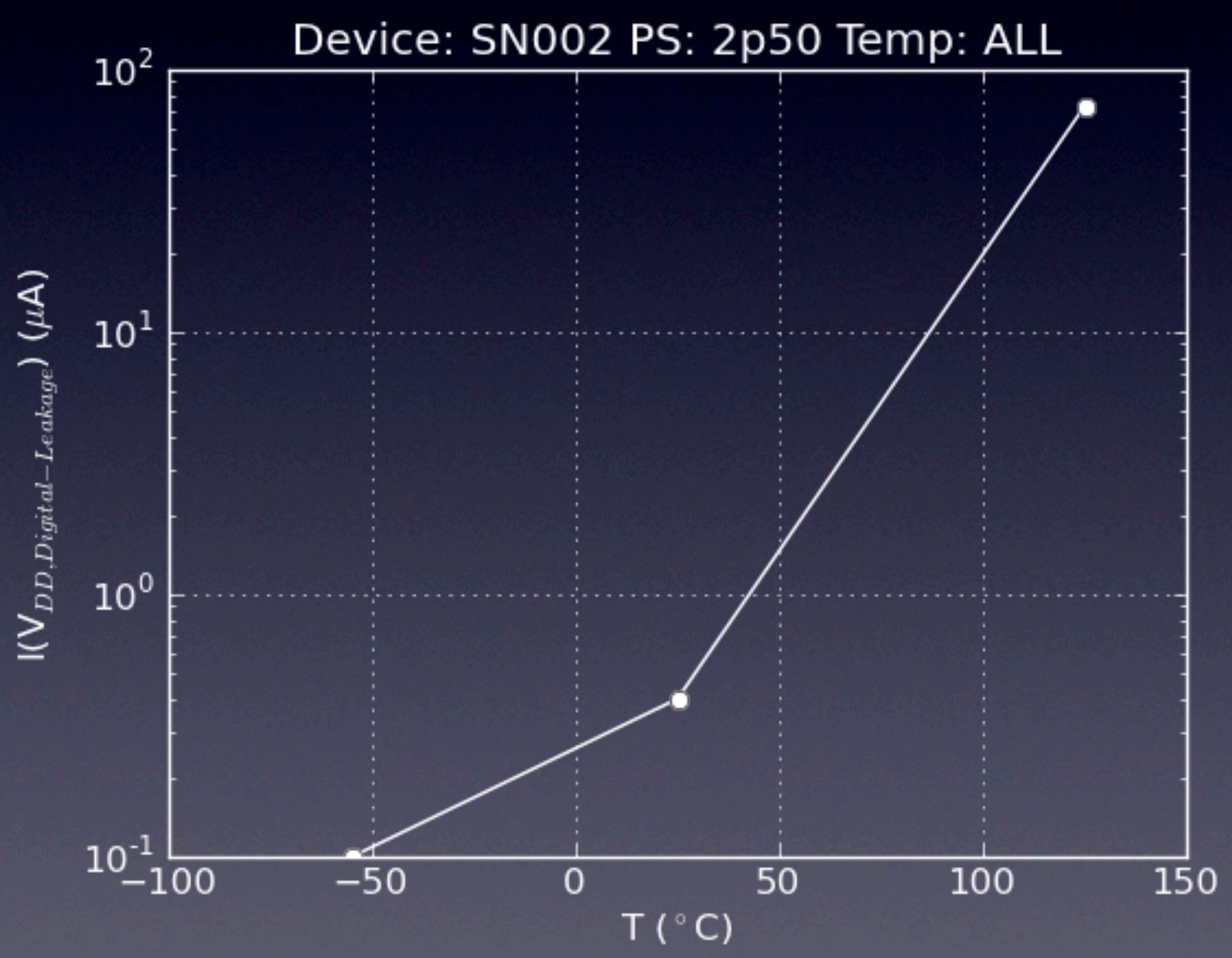
Leakage Currents

- Linear Dependency on power supply

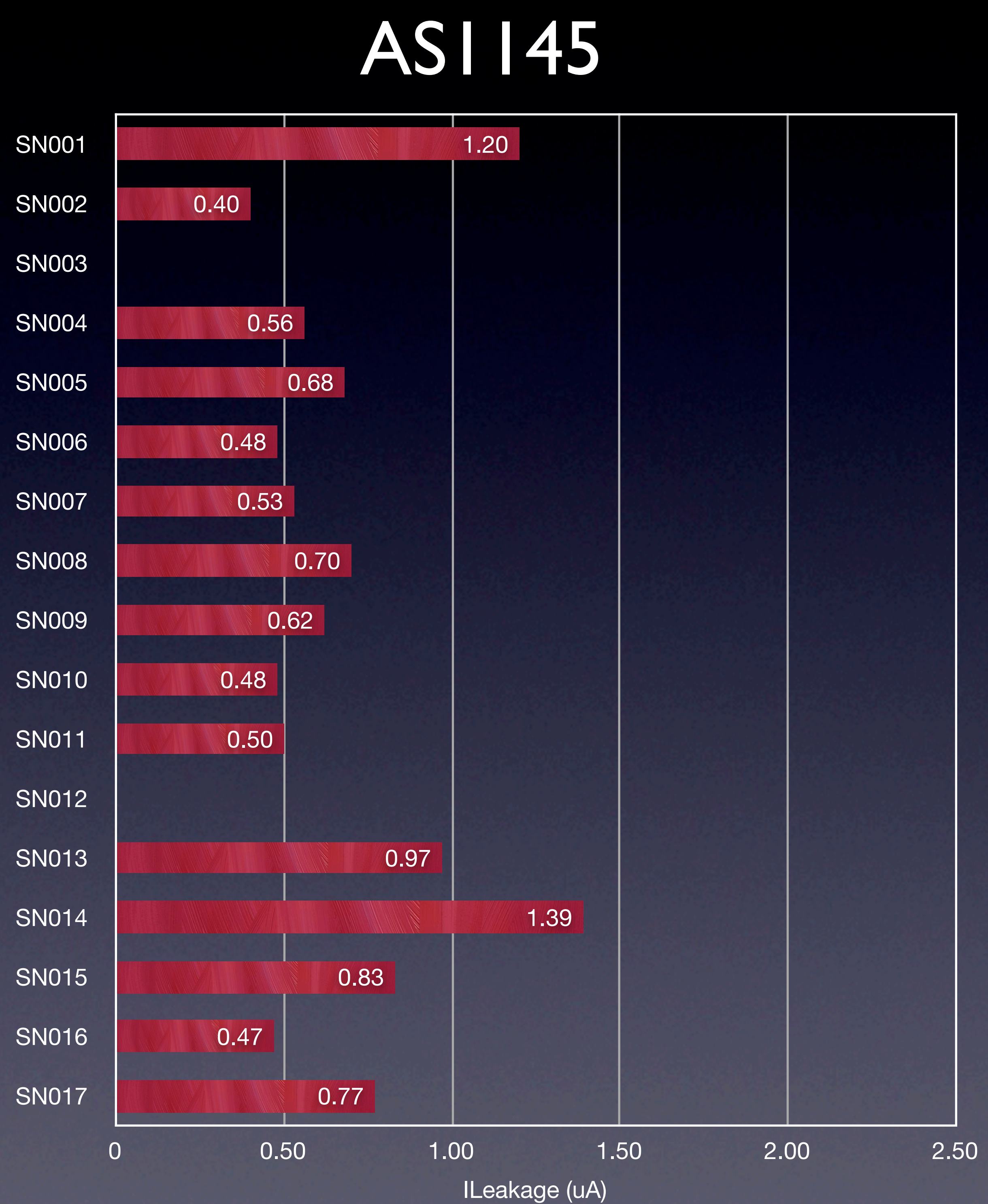


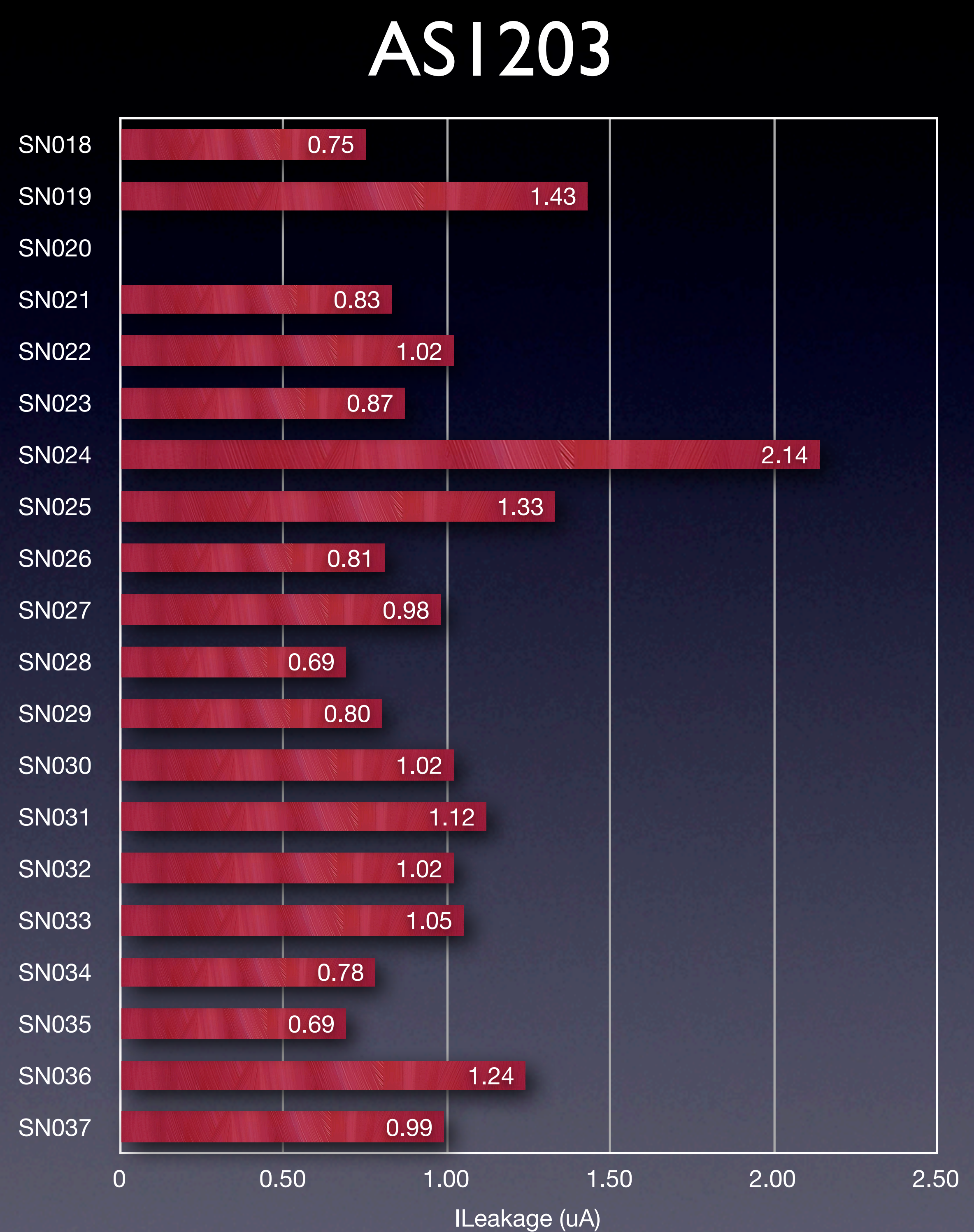
Leakage Currents

- Temperature Dependency
- 25 to 125 degC:
- ~200x

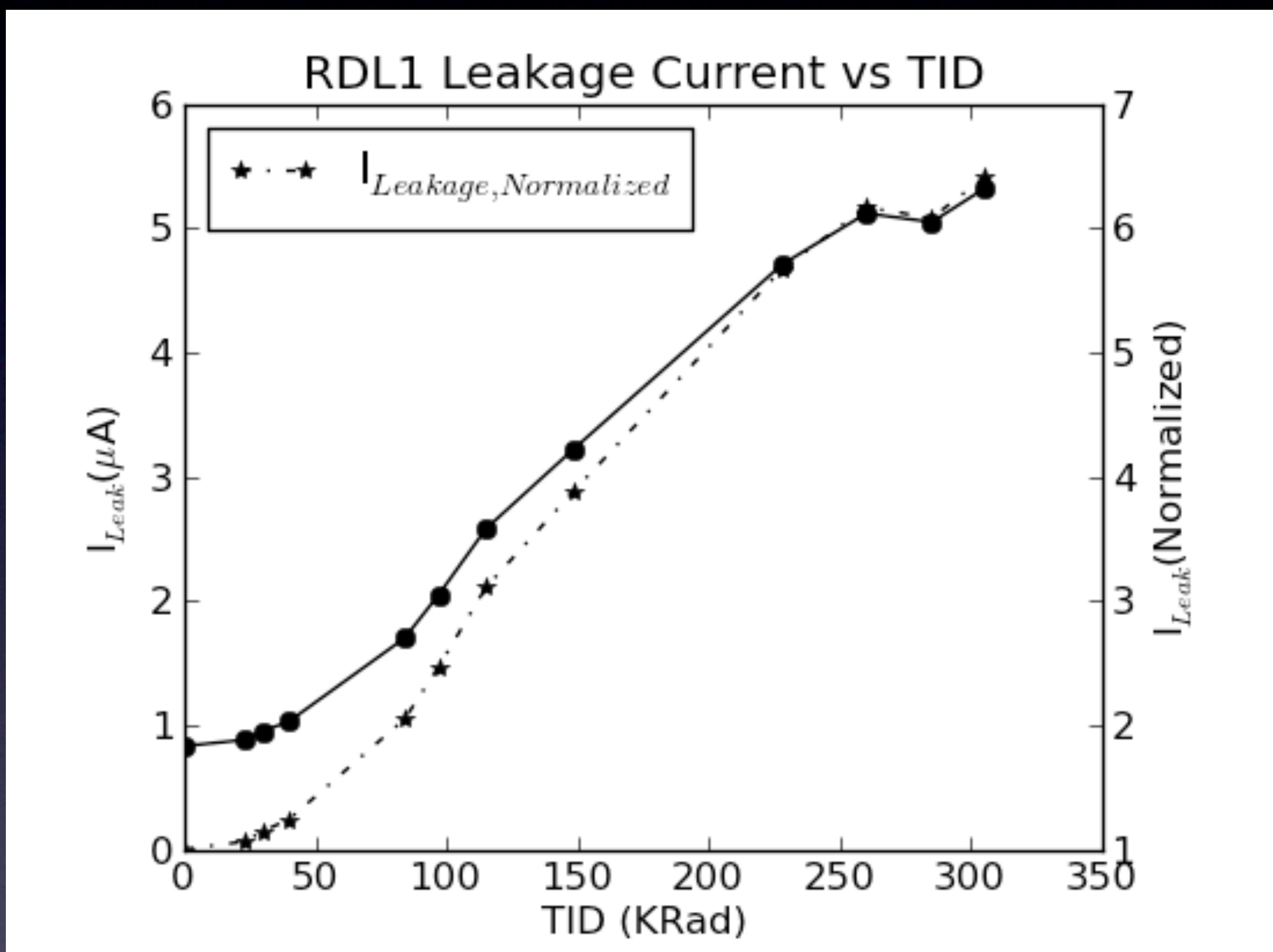


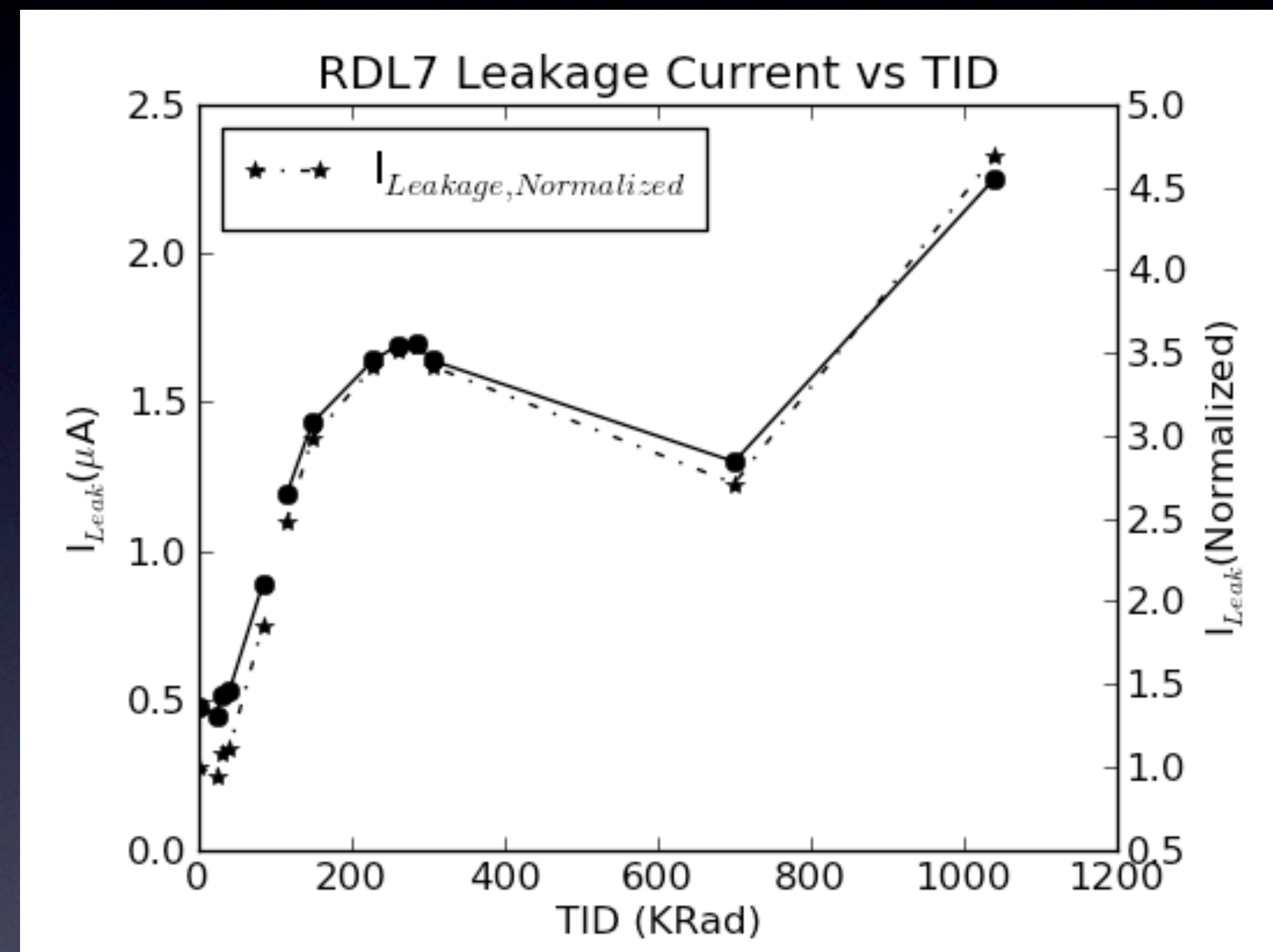
Leakage Current



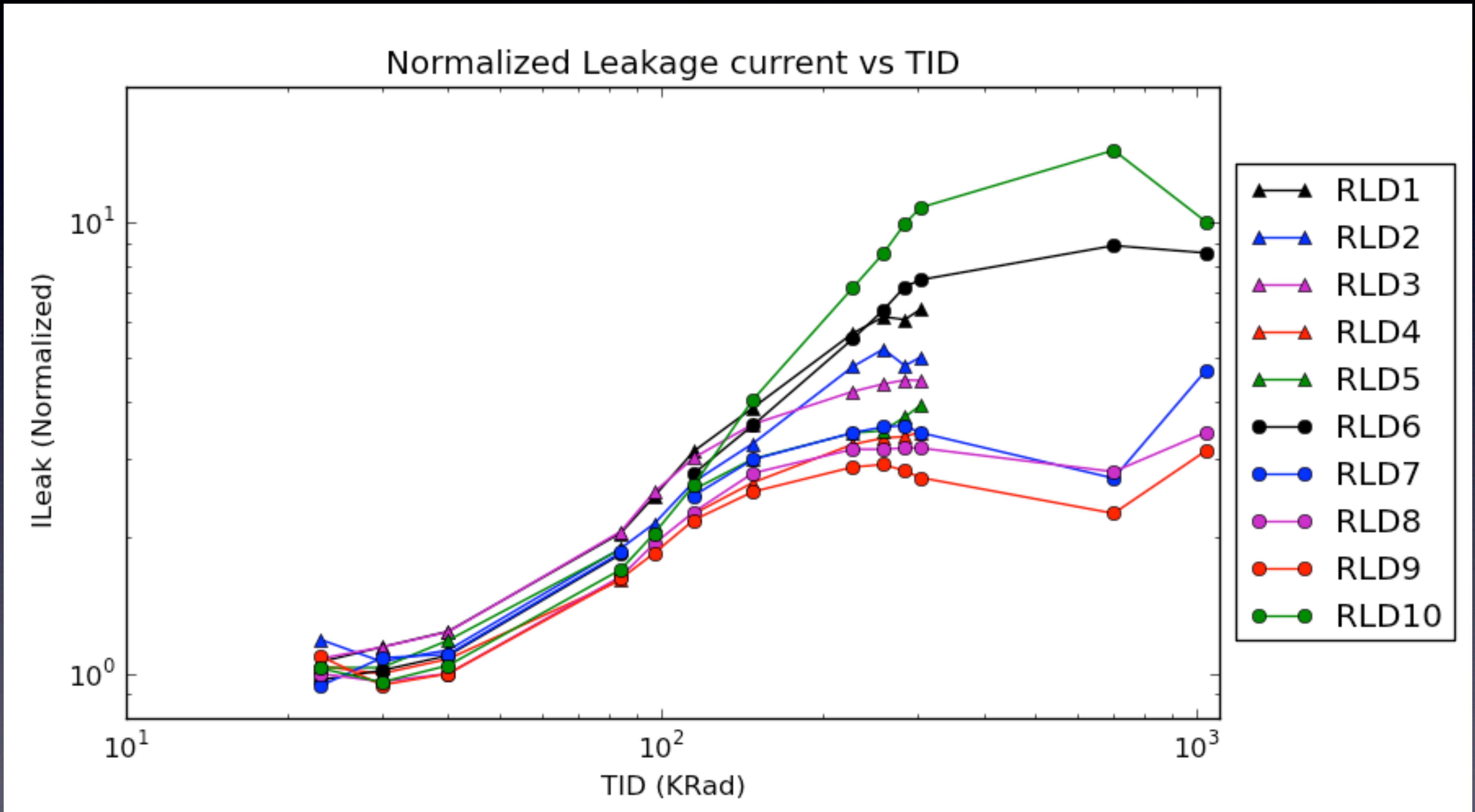


Leakage Current

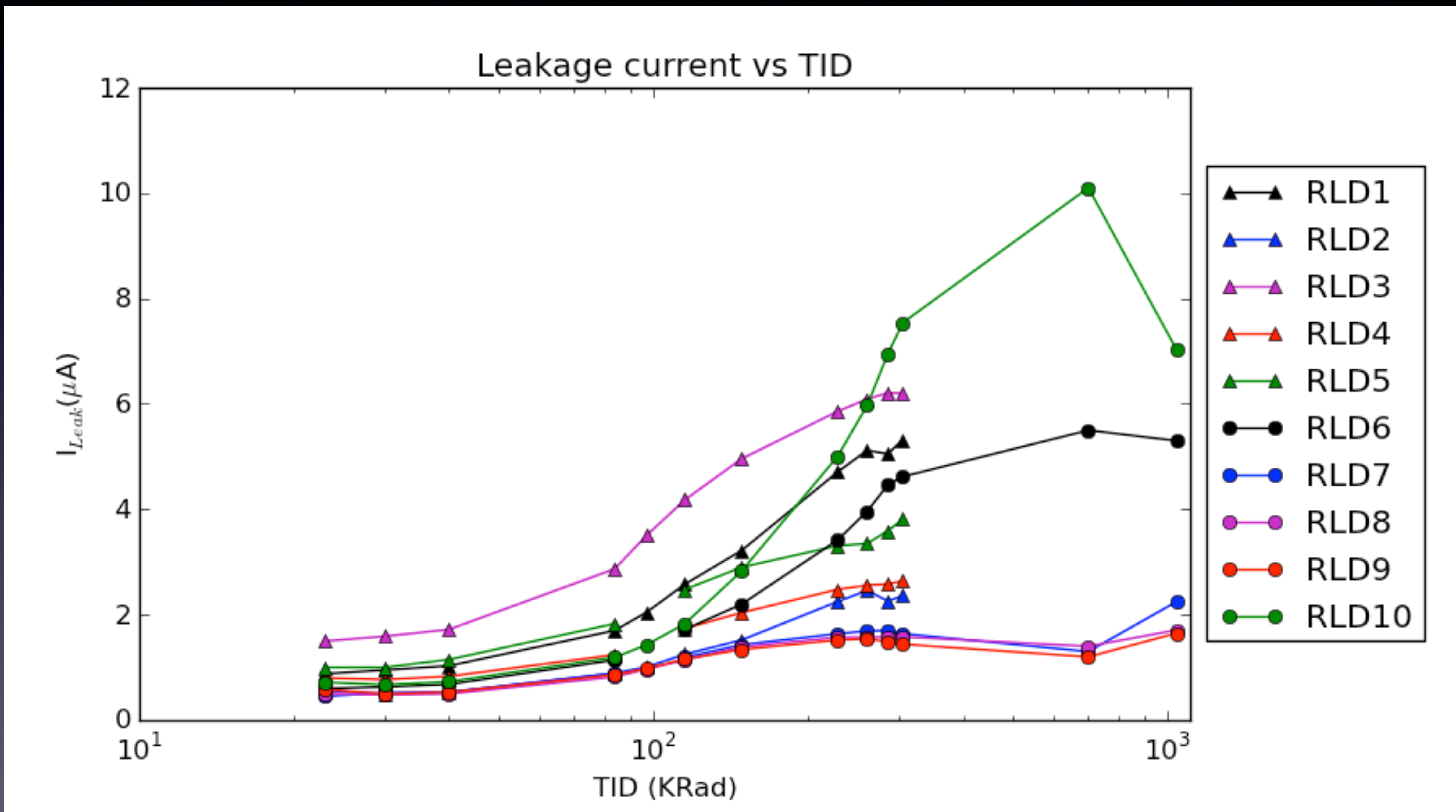




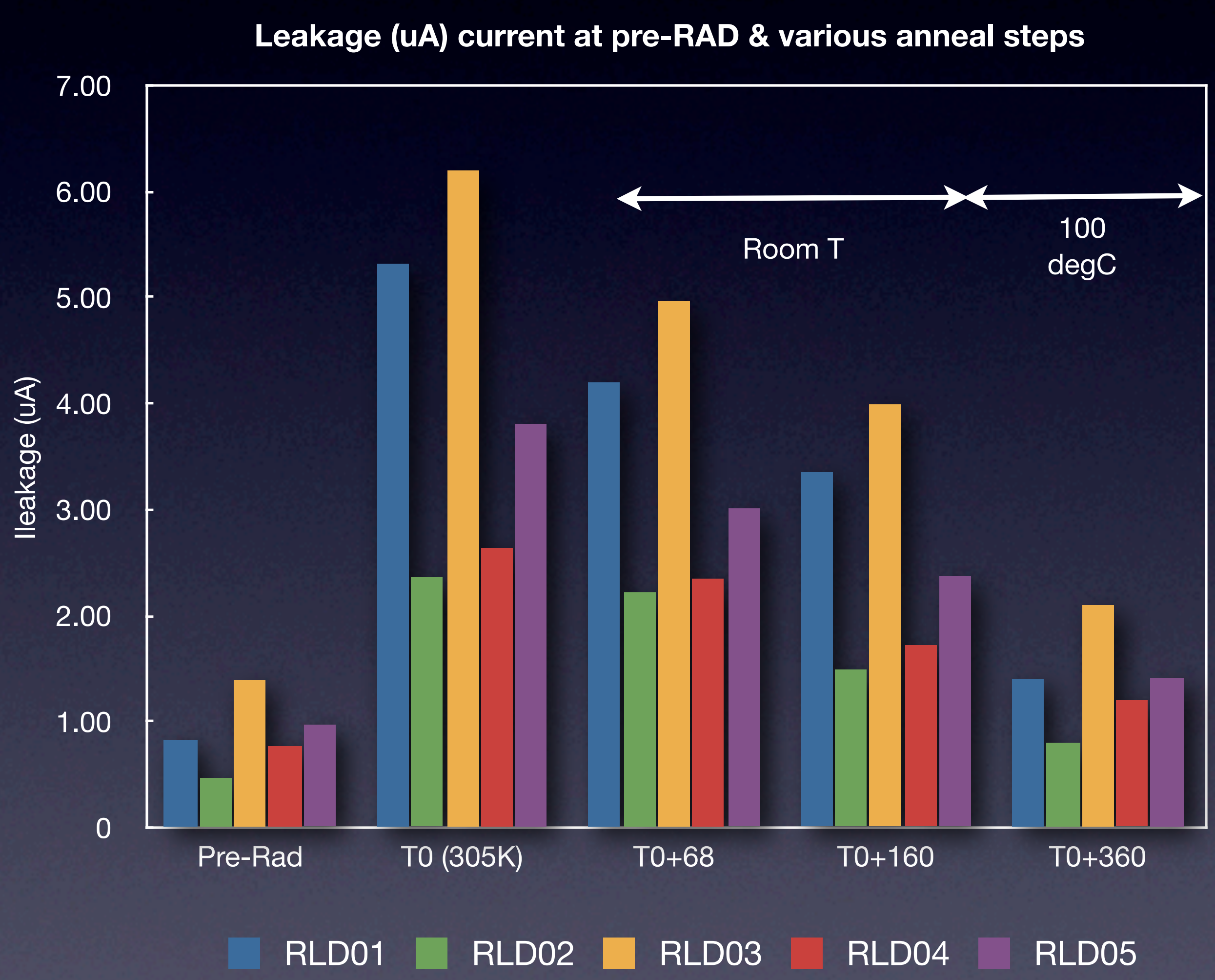
Leakage Current

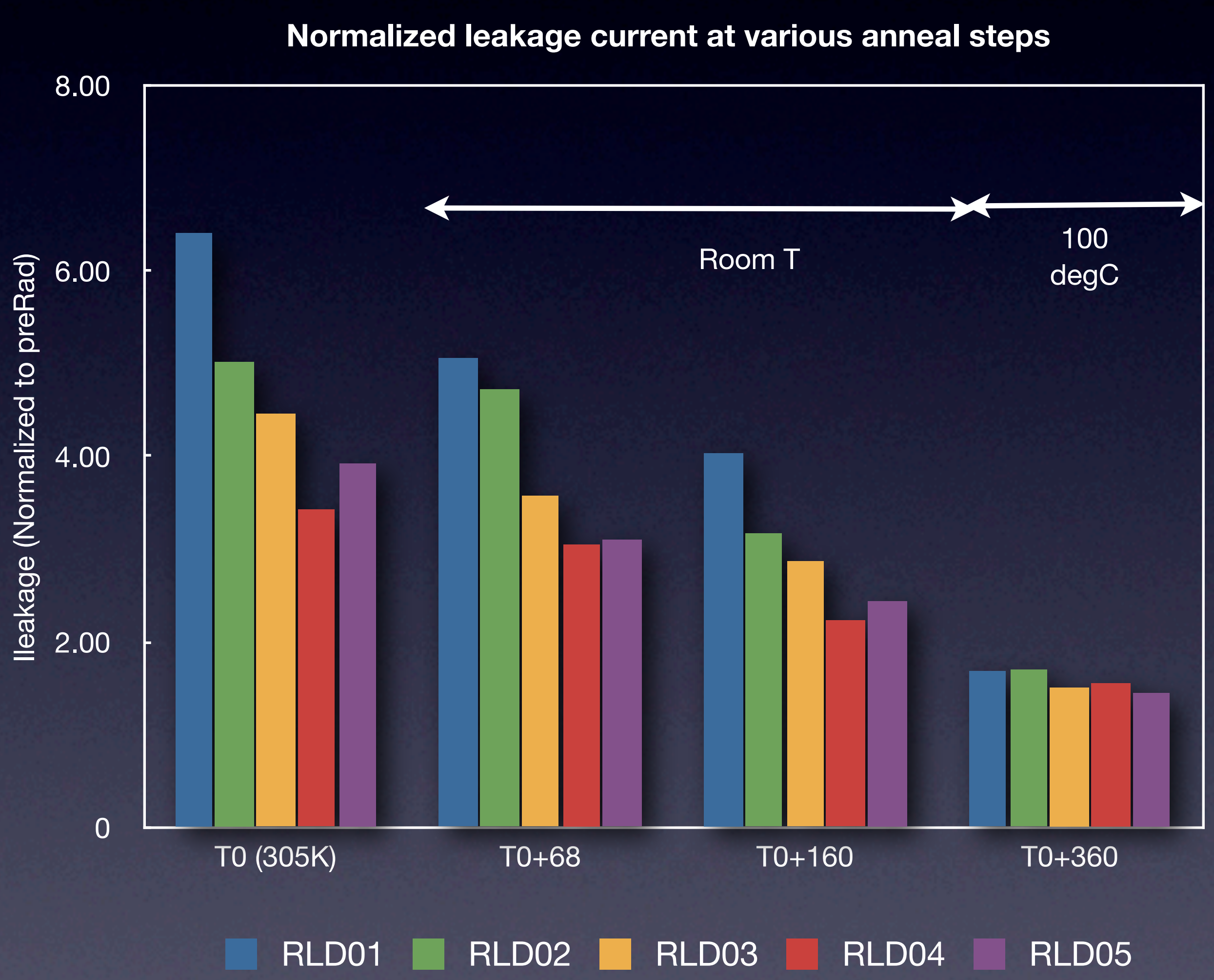


Leakage Current



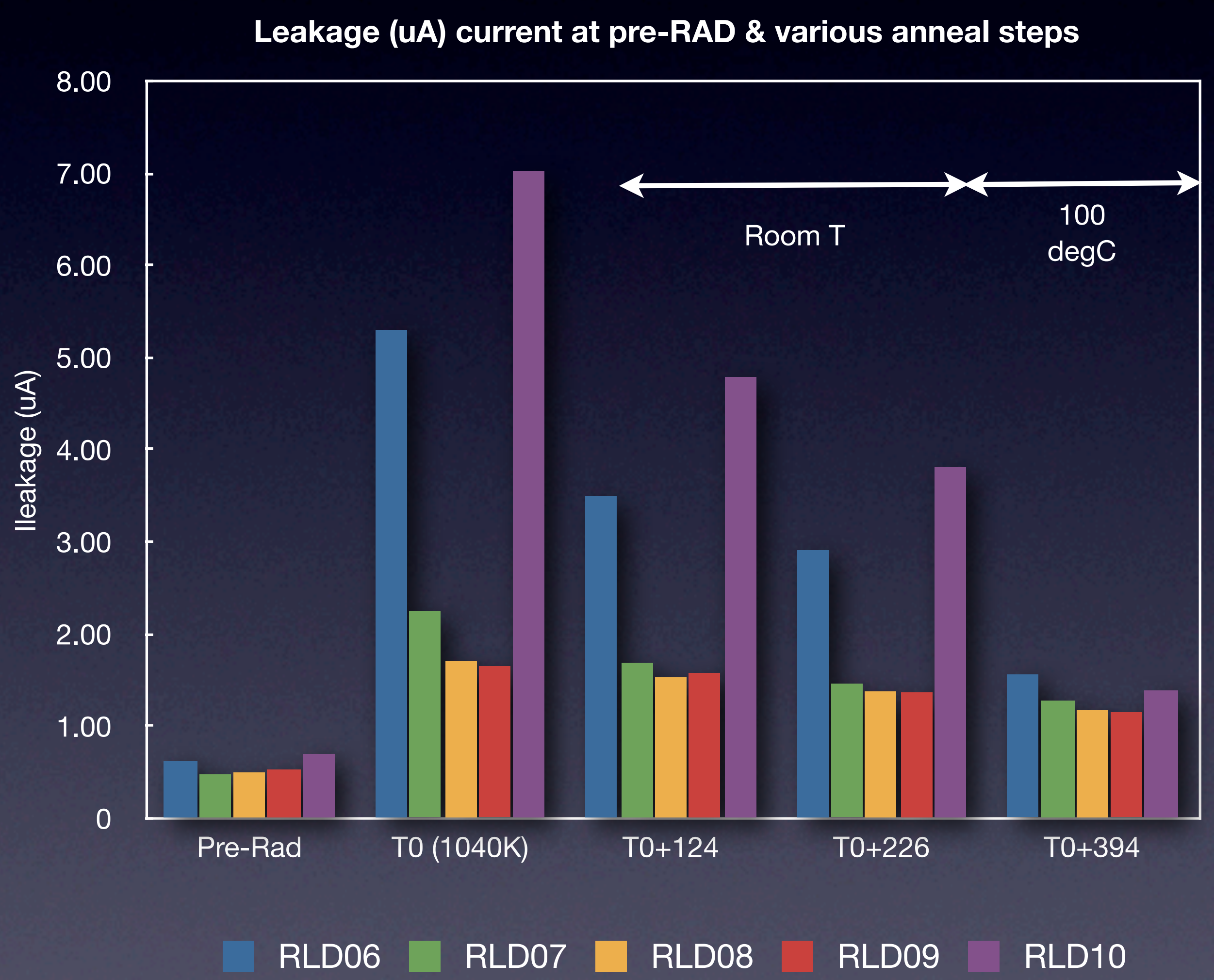
Leakage Current

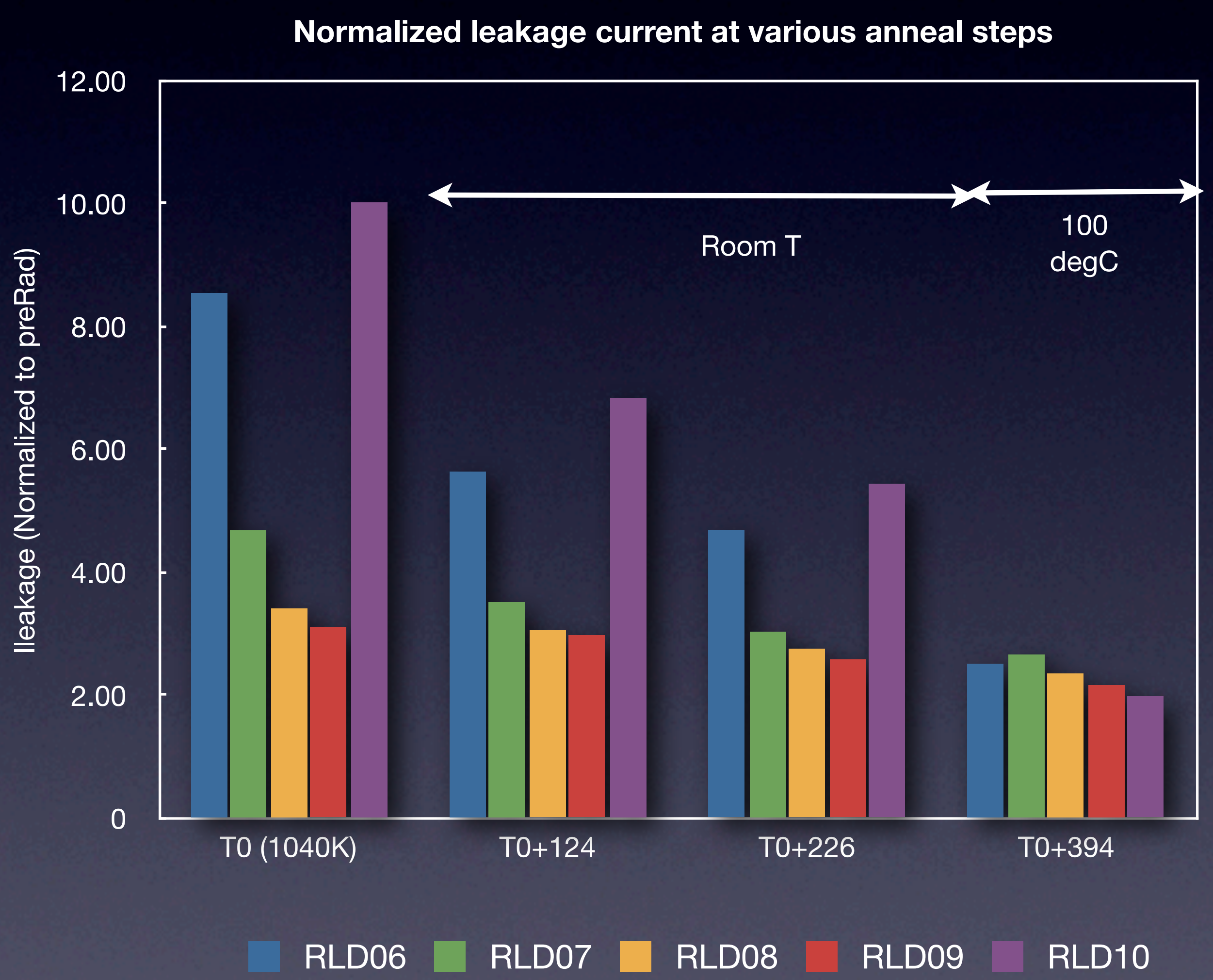




At the end of the anneal process leakage currents fall to 1.7x their respective pre-rad value

Leakage Current





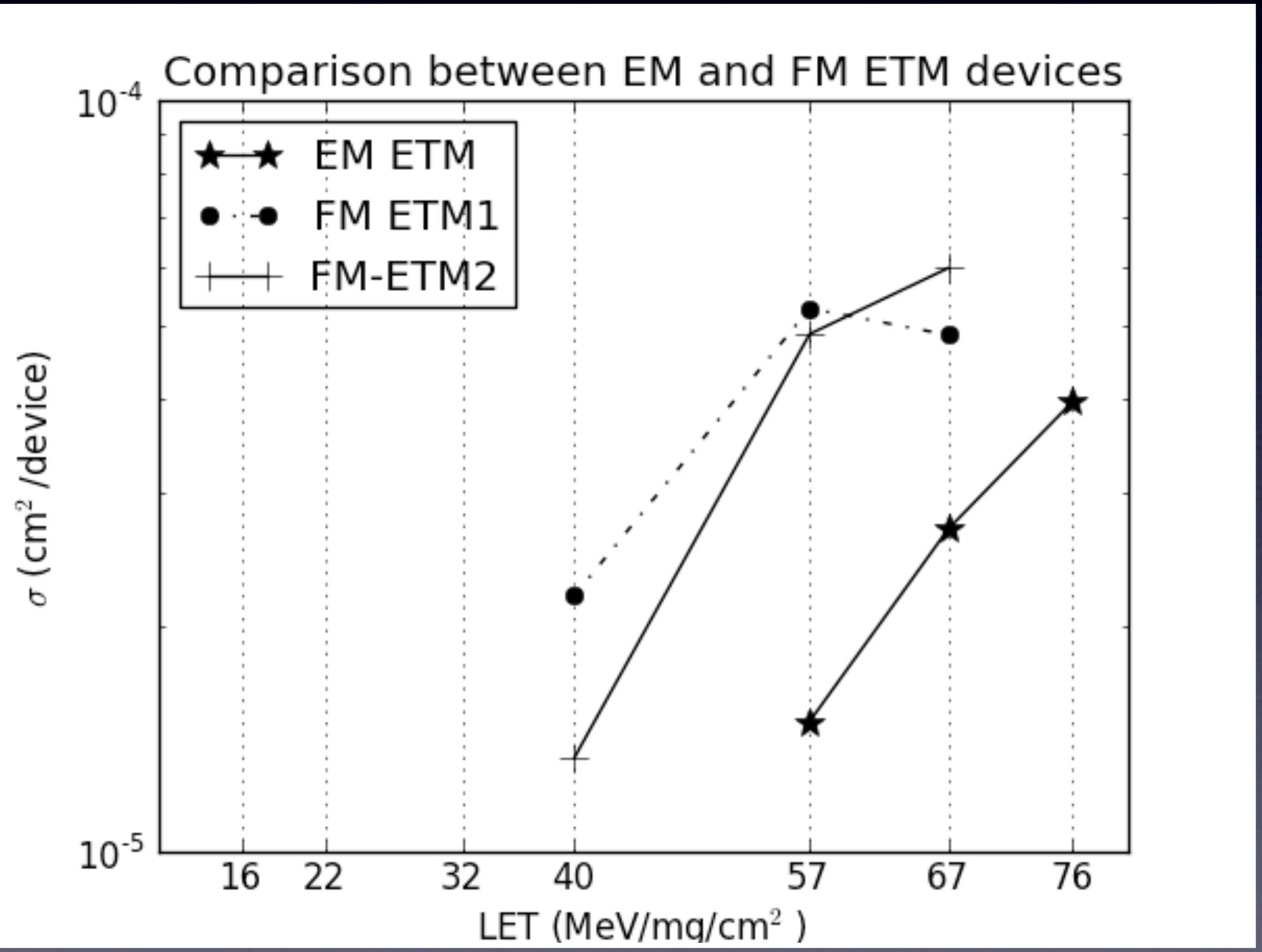
At the end of the anneal process leakage currents fall to 2.5x their respective pre-rad value

SEE Tests

- No SELs up to 67 MeV-cm^2/mg at 85 degC
- SEU cross section is at 57 MeV-cm^2/mg for the nominal core power supply of 2.5V
- Falls down to 40 MeV-cm^2/mg if power supply is reduced to 2.2V
- SEUs types are balanced

SEU Type	Counts
0 to 1	195
1 to 0	203

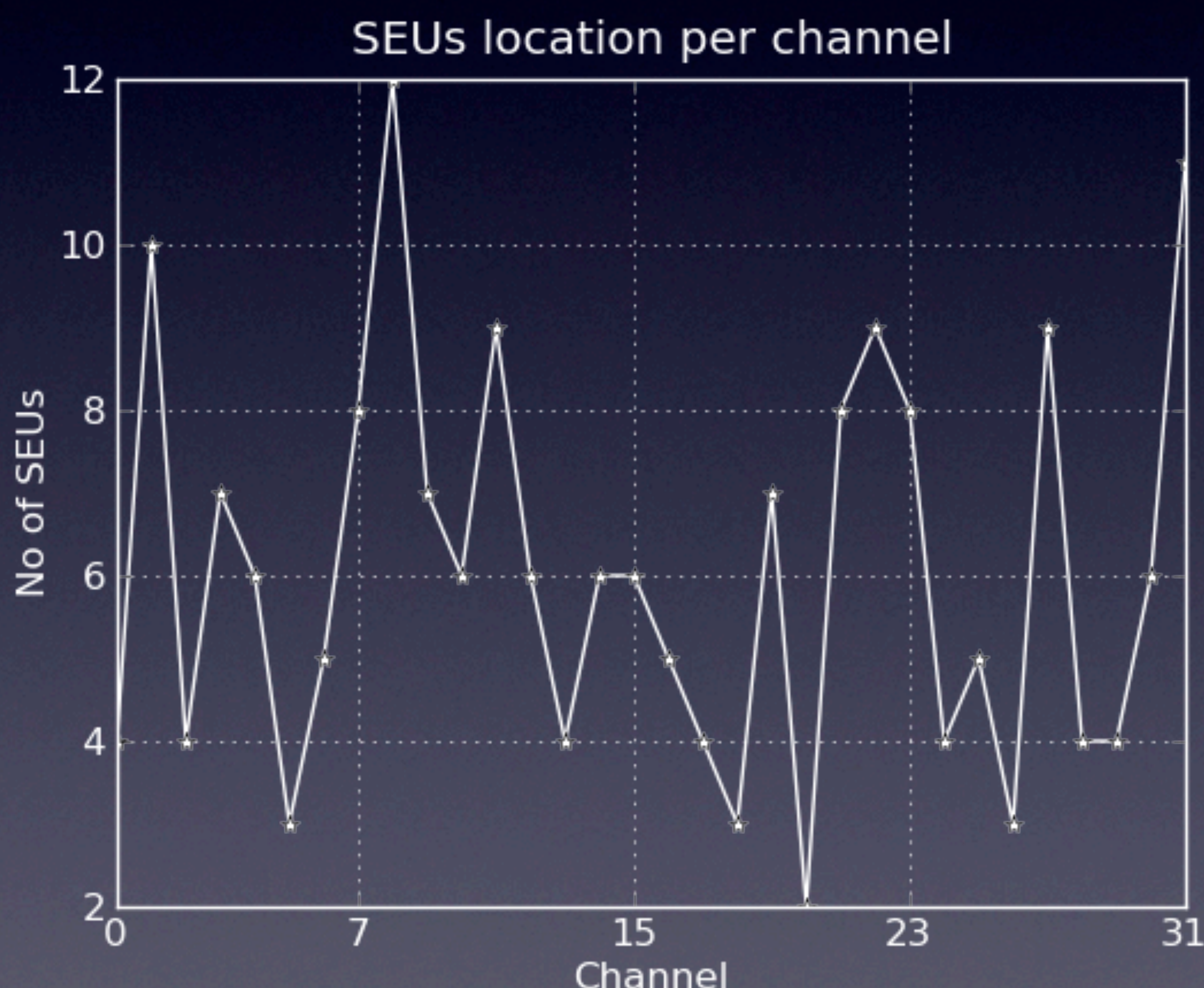
SEU Cross Section



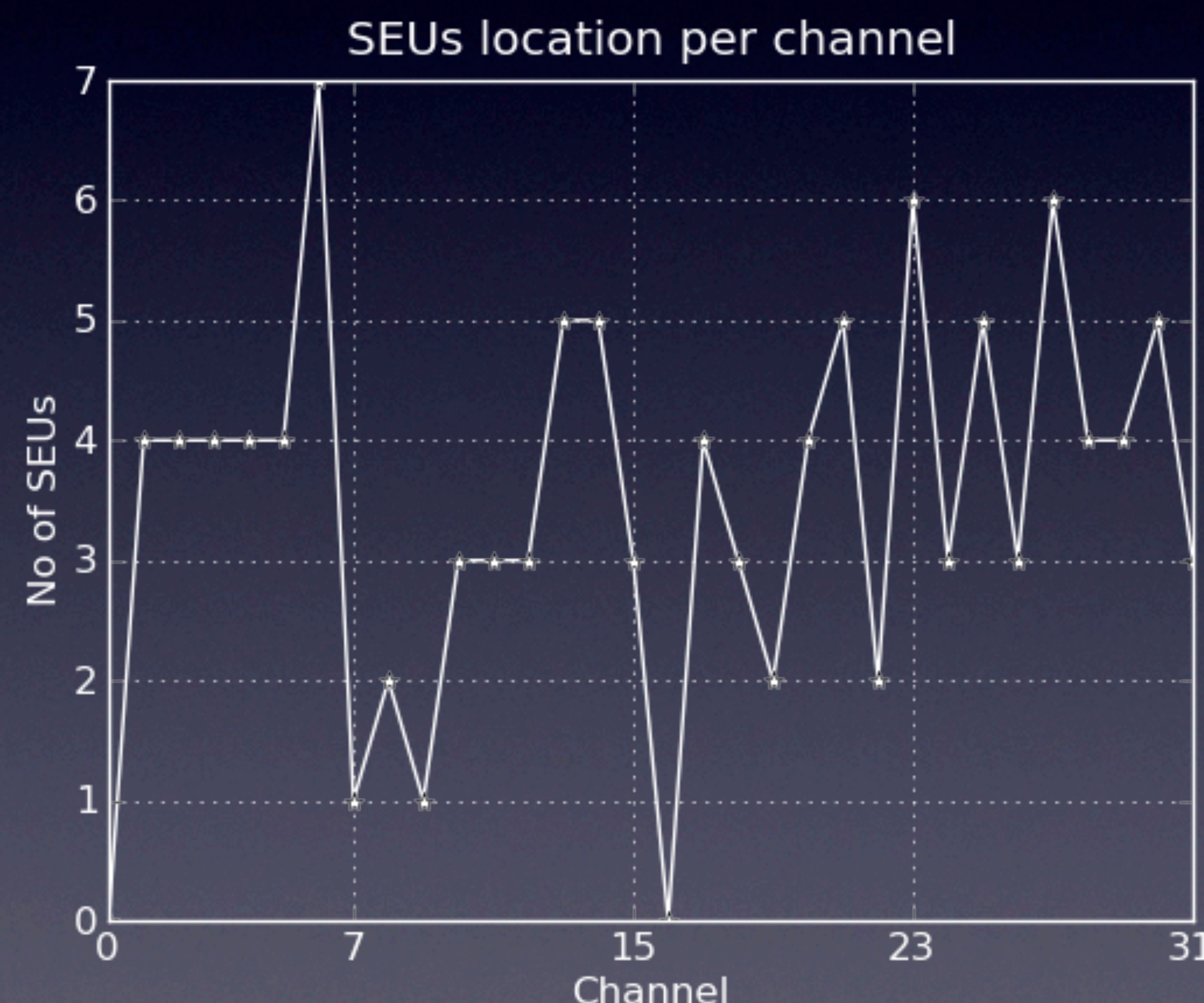
Channel Mapping of SEUs

ETM1

STD

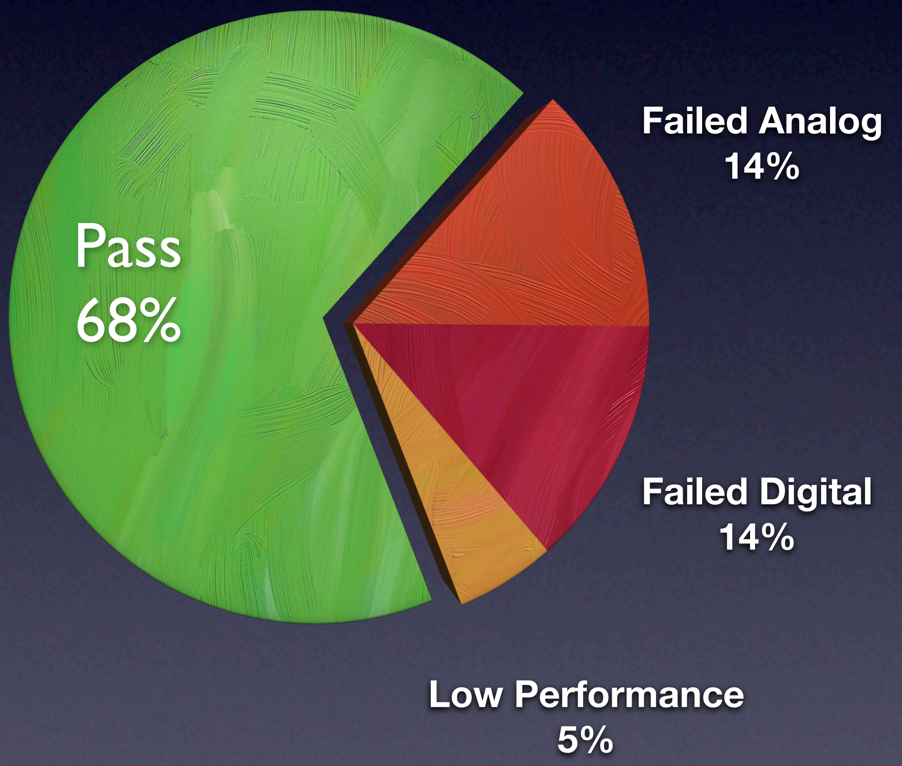


RTU



FM ETM Yield

	AS1145	As1203	Total
Failed Analog	3	2	5
Failed Digital	2	3	5
Low Performance	0	2	2
Good	12	13	25



Conclusions

- ETM is a mixed signal rad hard low power telemetry acquisition ASIC
- It can replace boards with discrete components for essential telemetry, RTU and instrument housekeeping applications