Qualifying a CMOS Instrumentation Chain for Charged Particles Detection in the Space Environment

Bouyjou, F.[1,2]; Bernal, O.[1,2]; Tap, H. [1,2]; Picaut, G.[3] and Sauvaud, J-A.[3]

[1] Univ de Toulouse, INP, LAAS,

F-31400 Toulouse, (France)

[2] CNRS, LAAS, 7 avenue du colonel Roche,

F-31400 Toulouse, (France)

Email: bouyjou@enseeiht.fr, bernal@enseeiht.fr and tap@enseeiht.fr

[3] CNRS, IRAP, 9 avenue du Colonel Roche,

F-31400 Toulouse, France

Email: guillaume.picaut@thalesgroup.com and jsauvaud@irap.omp.eu

ABSTRACT

For the solar system exploration and the distant universe study, the in-situ particle energy measurement and/or the electron/ion event detection are needed. For our on-board satellite application, the particle sensor that is used to convert particle momentum into measurable electrical charges is a Microchannel plate (MCP). The performances of such a sensor depend on the Analog-Front-End (AFE) circuit used to process the incoming charges. Consequently, a CMOS instrumentation chain for charged particle detection has been designed and tested under space environment. This AFE contains 16 channels, all of which includes a charge pre-amplifier (CPA), a pulse shaper (PS) and a monostable circuit to perform the detection. Using a standard 0.35 µm CMOS process, the proposed AFE has a conversion gain of 0.9 mV/fC for electrons and a power consumption of 2.15 mW per channel. Its dynamic range is 79 dB and it is possible to convert charges up to 1.5 pC. The circuit works properly from -20 to 80°C with a measured analog gain variation of 1 $\mu V.fC^{-1}.K^{-1}$. As far as crosstalk is concerned, experiments show that the proposed instrumentation chain can detect negative charges down to 122 fC without any ambiguity. Further, the proposed chain was irradiated at an average rate of 140 rads (Si) per hour up to 360 krad without any functionality loss.

INTRODUCTION

Solar system exploration and distant universe study are mainly based on in situ particle energy and/or event measurements, and on remote electron and ion detection. The performances of particle sensors [1], mostly used to convert particle momentum into measurable electric charges, depend on the AFE circuit used to process the incoming charges. Together the sensor and its instrumentation circuit are called astrophysical “sensor heads”.

To measure the particle flow energy level and to determine its direction, electrostatic deflectors, such as top-hat electrostatic analyzers are used [2]. The particles are thus accelerated after the energy selection by an additional electric field applied between the output of the analyzer and the particle sensor. In event counting applications, it is interesting to use MCP to detect it. In fact, by generating secondary electrons, such a MCP architecture can typically achieve an average gain of 10^6. These secondary electrons are then collected by 16 anodes distributed all around the MCP to obtain a 22.5° angle resolution.

Finally, the charge Q generated by one particle event, is processed by a readout circuit which converts it into a voltage. Note that this charge Q can either be negative (MCP based detector) or positive (inverse biased diode or avalanche

photodiode) depending on the particle detector type. As shown in [3], a typical AFE readout circuit consists of the following stages, a CPA, a PS. In our application for the detection, a discrimination stage is also required.

Nowadays, electronics used in space instrumentation is mainly discrete. Pre-qualified electronics for space environment can achieve the required specifications till now, but it greatly limits the evolution of detector performances. For example, to obtain better spatial and spectral resolutions, more and more channels are needed, thus increasing strongly consumption and size. In this case, electronics can become the system bottleneck. Instead of using discrete components, the development of an ASIC (application-specific integrated circuit) is a good alternative.

Over the last few years, ASIC technologies used in space embedded systems have evolved from radiation-hardened technologies to more conventional CMOS/BiCMOS ones for three main reasons: less costly, easier access and greater integration [4]-[7]. Since CMOS technologies are mature and intrinsically more immune to radiations, it becomes very interesting to design multichannel space instrumentation.

In severe spatial context, temperature is one of the main causes of electronic failures. Therefore, the circuit must be able to operate under large temperature variations (typically between -20°C and 80°C). Also, the planetary missions are constantly exposed to radiative environments. They consist mainly of charged particles such as protons and electrons. In low earth orbit missions, electronic devices must tolerate a minimum Total Ionizing Dose (TID) [8] of 20 krad for a 2 year mission [9]. To fulfill these conditions, the technology must be carefully chosen and some design techniques must be used to improve the circuit radiation tolerance.

Radiation effects on MOS devices are explained in [10]-[13]. Due to a thinner gate oxide thickness, modern CMOS transistors are naturally more radiation-hardened [10] than older technologies. Nevertheless, TID can still lead to NMOS current leakage [8]. Here, for an expected TID of at least 20 krad, the failure level scaling trend for digital CMOS process shows that a 0.35 µm technology is one of the most appropriate [10].

For our application, we used a standard 3.3 V 0.35 µm CMOS technology. The circuit design CPA+PS is described in [2].

The aim of this paper is thus to present the ASIC measurement results to validate the proposed instrumentation chain for space environment. It particularly shows that a conventional CMOS 0.35 µm technology can withstand TID higher than 360 krad even though only a few radiation-hardening design techniques have been employed.

In the next section, the MCP readout circuit is described. In Sections III, measurement results in vacuum chamber are presented. In Section IV, the circuit test results under temperature and radiations are shown.

MCP FRONT-END ARCHITECTURE

The circuit architecture is shown in Fig. 1. A more detailed description of the CPA+PS circuit stages can be found in [2].

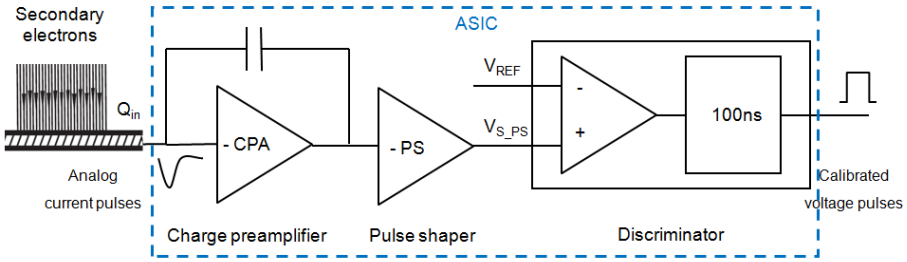

Fig. 1. Architecture of one channel of the event readout circuit.

The conversion gain G_c (charge to voltage) of the analog processing chain (CPA+PS) is set to 1.375 mV/fC in order to obtain a 1.65 V output voltage response for an incoming 1.2 pC charge.

First, the incoming negative charge is converted into a proportional positive voltage by a CPA. Next, this voltage is inversed and filtered by a PS. Both structures are designed to be very low noise and low power consumption [2]. The analog part has been optimized to be perfectly adapted to the MCP parameters and the targeted application, here the detection of charged particles. For example, efforts have been made to reduce noise and optimize the transconductance

of the input transistor. As shown in Fig. 2, an optimal size (W/L) of the PMOS input transistor to have the least possible noise can be found in simulation for a given shaping time and drain current.

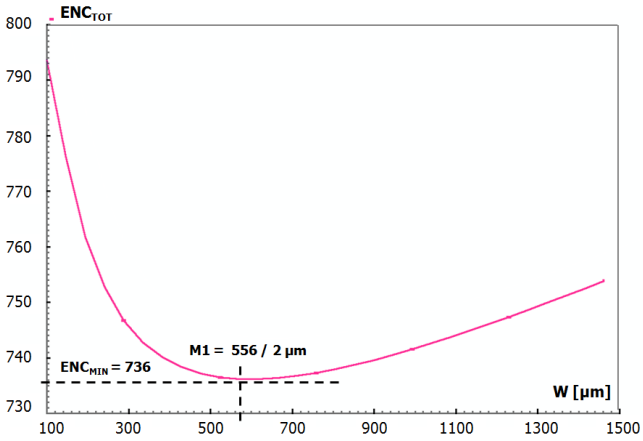

Fig. 2. PMOS input noise (ENC) optimization [2].

Here for a shaping time of 55 ns, $I_D = 320\,\mu A$ and an input capacitor of 5 pF, a large W/L PMOS input transistor is found (M1 : W_1/L_1 = 556/2 µm) to minimize noise.

Then, the PS output is processed by a discriminator (Fig. 1) in order to select only relevant events. A discriminator is a tunable level detector with a 1-bit analog-to-digital converter which provides a standard logic pulse of 100 ns width. It is made up of three parts: a comparator, a monostable circuit and a buffer. The first part compares the PS output voltage to the threshold voltage V_{REF}. This voltage V_{REF} which is used to define the minimum input amplitude to be detected (typically above the noise floor), can be set externally. The monostable circuit converts the comparator output voltage into a logical pulse of 100 ns width for system requirements.

The electrostatic analyzer angle resolution needs 16 channels to ensure the detection of all the MCP anodes. The 16 channel readout circuit has been integrated using a 0.35 µm CMOS technology. Fig. 3 shows the 5.67 mm² microchip photo. The ASIC is called CDIC16 for Charges Detection Integrated Circuit with 16 channels. The total power consumption is 2.15 mW/channel. To reduce crosstalk, the 16 channels are divided into 4 clusters of 4 channels each. In addition, each cluster has its own power supply. A test channel has also been integrated to probe the analog output voltage of the CPA and PS.

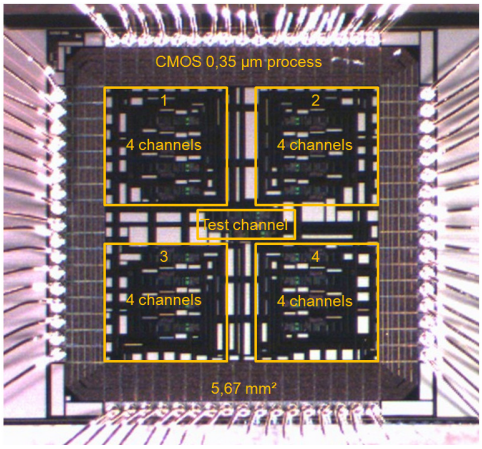

Fig. 3. Die photograph of the 16 channel readout circuit and a test channel.

TEST OF THE INSTRUMENTATION CHAIN

Vacuum chamber

In [2], measurement results were obtained by stimulating an input charge by applying a pulse voltage to a capacitor. Here, measurements of the full instrumentation chain have been carried out in a vacuum chamber in order to validate the circuit operation with a MCP and also to simulate space environment conditions. In a vacuum chamber, it is possible to directly generate incoming charges such as electrons by using an electron gun. These charges can then be directly amplified by a MCP which is finally connected to the ASIC test channel input.

The operation of the electron gun consists in extracting electrons from a conductive material into the vacuum and accelerating these electrons using an electrical field. This electron beam then illuminates the MCP which provides the amplification. Further, for test purposes, the MCP can be easily positioned in order to select a particular anode to which the test channel is connected. The charges generated by the MCP are thus collected by the test channel. Its PS output can be probed to measure the detected charge. The PS output signal is used to confirm the proper operation of the ASIC by plotting the MCP pulse gain distribution of the MCP at 2650 V measured with the ASIC (see Fig. 4).

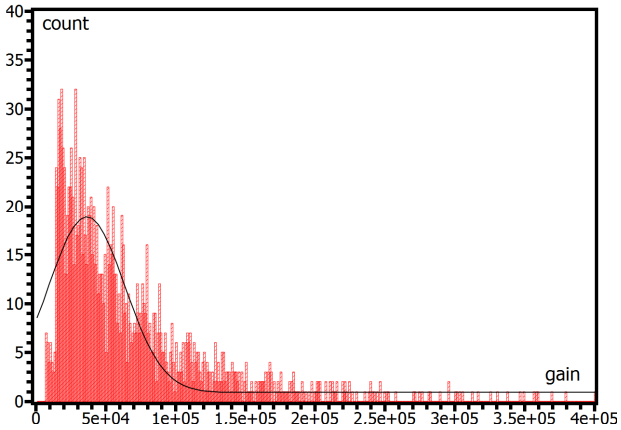

Fig. 4. Measured MCP pulse gain distribution at 2650 V due to charges of an MCP illuminated by an electron beam.

This test was performed, as a worst case, on an old MCP which implies that the MCP gain might be lower than previously mentioned (typically 10^6). Here, the MCP provides an average gain of 36.4 k for a MCP polarization voltage of 2650 V.

Crosstalk

Using 16 charge conversion channels on a same chip (Fig. 3) allows to significantly reduce the required detector size. However, their inherent proximity can induce capacitive coupling from one channel to another. Further, the conversion channels within a same cluster share the same supply voltage as well as the same substrate. Consequently, digital output triggers can generate some disruptions in the circuit. All these phenomena, also called crosstalk, might increase the minimum detectable charge.

When an incoming charge from the detector is correctly detected by a channel, thereby triggering its discriminator, unwanted signals might be injected into its surrounding channels through power supply lines and bulk substrate. If the comparator thresholds of these later channels were set too close to the noise floor, the generated parasitic signals could trigger their comparators and thus be incorrectly interpreted as an incoming charge. Crosstalk between channels can generate false events. As a consequence, in order to avoid false event detections due to crosstalk, a minimum threshold voltage must be found. To do so, for each cluster, experiments have been made to define the minimum threshold voltage for which crosstalk or noise could not trigger false events. Finally, the highest threshold voltage among the four clusters is chosen.

Three samples have been tested and the minimum detectable input charge without any ambiguity is 122 fC for electrons. These results show a 6% data loss for electron for typical 2300 V MCP polarization. This implies that the minimum threshold voltage is limited to that value: 762.5 ke^-.

VALIDATION OF THE CHAIN IN SPACE ENVIRONMENT

Extreme temperature performances

CDIC16 is placed in a thermal enclosure system. First, the CPA+PS output voltage versus the input positive charges (between 45 fC and 450 fC), has been simulated and measured for different values of temperature at 2.4 MHz (frequency near the AFE maximum count rate [2]).

Over the whole temperature range, the amplitude variation is linear with the input charge. However, the charge to voltage gain increases with temperature, which affects only the minimum detectable incoming charge. This variation can be explained by the fact that a poly-silicon resistance increases linearly as the temperature is raised. Further, in the PS, a MOS device is used as a resistor in the amplifier feedback loop [2]. Such a resistor is exponentially dependent on the temperature. These results are in accordance with simulations.

The dependence of the conversion gain at 2.4 MHz on the temperature corresponds to a variation of 1 $\mu V.fC^{-1}.K^{-1}$.

Radiation tolerance

TID is evaluated using gamma rays (γ). When a MOS transistor is exposed to these high-energy incident photons, electron-hole pairs are created in the gate oxide SiO_2. The generated carriers induce the buildup of charges which can lead to device degradations [13].

The irradiation testing facility

Cyclotron radiation tests have been performed in the Nuclear Physics Institute of UCL (Université Catholique de Louvain).

The circuits to be tested to radiation tolerance are placed in the irradiation facility to cumulate a radiation dose issued from the $^{60}C0$ at a rate of approximately 140 rad/hour. As shown in Fig. 5, three CDIC16s are irradiated at the same time: (1) $CDIC16_1$ and $CDIC16_2$ are turned on and theirs 16 inputs are electrically stimulated by charge pulses to simulate incoming input charges; (2) $CDIC16_3$ is grounded. Note that all CDIC16s are tested up to a dose of 103 krad by step of 5 krad. Then, $CDIC16_1$ had been irradiated up to 220 krad and $CDIC16_2$ up to 360 krad.

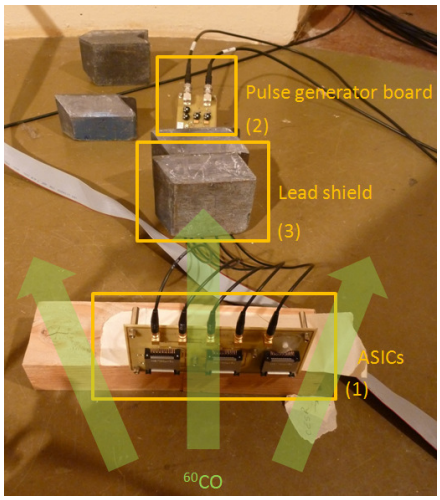

Fig. 5. Irradiated ASICs PCB with its power-supply and input stimuli PCB protected by a lead shield.

Measurements are made in-between irradiation steps of 5 krad to observe the effects of threshold voltage drifts and edge leakage current increases. One of the consequences of these drifts and leakage can be observed by measuring the power consumption of the ASIC as a function of TID. Functional tests of the 16 channels with the variable detection threshold are also performed. For the test chain, both CPA and PS analog stages are tested with an input charge pulse. Then, the characteristics of the comparator and monostable circuit alone are plotted. TID rate is about 3.4 krad/day.

Results

One of the most important test is to verify that all the channels are still operational after irradiation. With this aim, charges are injected at the inputs to confirm proper operation of CDIC16s. These tests showed that CDIC16 tolerates doses up to 360 krad without any relevant impact on the performance.

Another important test is the measurement of the power consumption. After irradiation, the $CDIC16_1$ and $CDIC16_2$ were annealed at 100°C during 168 hours and current consumptions of the 4 clusters of the 3 CDIC16s are shown in Fig. 6.

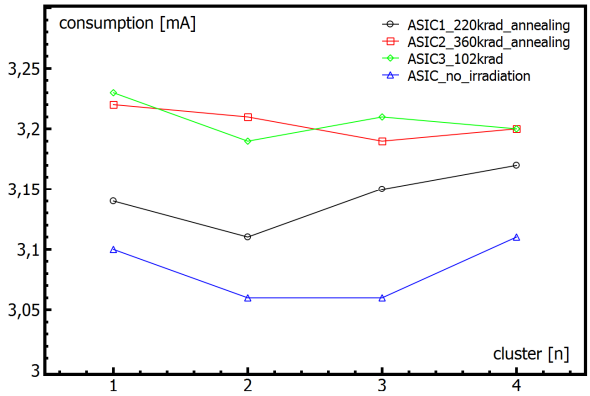

Fig. 6. Current consumption of the 4 clusters of 3 CDIC16s versus dose ranging from 0 to 360 krad.

In Fig. 6, the 4 clusters of a CDIC16 have almost the same power consumption variations. This shows that the dose received on a chip is the same. But it is interesting to note that there are still a few differences between the 3 CDIC16s according to their irradiation and annealing.

Before the irradiation, all the clusters of the 3 CDIC16s have a current consumption of about 3.07 mA per cluster. The third CDIC16 current consumption goes even up to 3.22 mA at 102 krad. Then, after a γ-rays irradiation of 220 krad for $CDIC16_1$ and 360 krad for $CDIC16_2$, the CDIC16s current consumption trend increases. The measurements on $CDIC16_1$ and $CDIC16_2$ were made after annealing and show a current consumption of 3.15 mA for $CDIC16_2$ and 3.22 mA for $CDIC16_3$ for one cluster. These results also show that after annealing, the power consumption of an irradiated circuit is partially recovered, which is consistent with some degree of interface state creation [8].

All the performed tests demonstrate that the proposed CDIC16 can tolerate radiation up to 360 krad at least.

CONCLUSION

This paper presented a CMOS instrumentation chain to be qualified for the space environment. In this paper, first, the test of the full instrumentation chain in a vacuum chamber has been presented to validate the CDIC16 operation with a MCP. Then, the crosstalk test has shown that the CDIC16 can detect negative charge over 122 fC free of any false detection. Next, a temperature test has been shown that the CDIC16 can withstand temperature ranging from -20°C to 80°C. Finally, gamma rays irradiation test has been carried out using ^{60}CO as radiative source to validate the CDIC16 operation with a TID of 360 krad. The CDIC16 and AMPTEK A111 component parameters have been summarized in Table 1. Compared to A111, the CDIC16 consumption and noise are reduced by a factor of 3 for the same count rate, which was the aim of this work. To conclude, it is shown that the CDIC16 can work in space environment with a MCP and is therefore qualified to make a specific space mission.

Table 1. Summary of CDIC16 Performances

Performances per channel	CDIC16	AMPTEK A111
Power supplies	3.3 V	4.7 V
Consumption	2.15 mW	6 mW
Noise ENC for C_{in}=5pF	954 e^-	3312 e^-
Detector max capacitor	0 – 25 pF	0 – 250 pF
Shaping time	55 ns	-
Count rate	2.6 MHz	2.5 MHz
Temperature accepted	- 20 °C à 80 °C	- 55 °C à 85 °C
Radiation tolerance	> 360 krad	> 100 krad
Crosstalk	90.9 fC (electron) 122 fC (hole)	-
Offset spread	7.6 mV	-

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REFERENCES

[1] M. West, D.S. Evans, R. von Steiger, Calibration of Particle Instruments in Space Physics, The International Space Science Institute Scientific Report, 2007.

[2] Bouyjou, F.; Bernal, O.; Tap-Beteille, H.; Sauvaud, J.-A.; , "A Low-Power CMOS Instrumentation Chain for Microchannel Plates in Astrophysics," *Sensors Journal, IEEE* , vol.11, no.4, pp.1040-1045, April 2011.

[3] H. Spieler, "Semiconductor detector systems", *Oxford University Press*, 2005.

[4] Yeom, J.Y.; Defendi, I.; Takahashi, H.; Zeitelhack, K.; Nakazawa, M.; Murayama, H., "A 12-Channel CMOS Preamplifier-Shaper-Discriminator ASIC for APD and Gas Counters," *Nuclear Science, IEEE Transactions on* , vol.53, no.4, pp.2204-2208, Aug. 2006.

[5] Noulis, T.; Siskos, S.; Sarrabayrouse, G., "Noise optimised charge-sensitive CMOS amplifier for capacitive radiation detectors," *Circuits, Devices & Systems, IET* , vol.2, no.3, pp.324-334, June 2008.

[6] Oo, K.T.Z.; Mandelli, E.; Moses, W.W., "A High-Speed Low-Noise 16-Channel CSA With Automatic Leakage Compensation In 0.35-µm CMOS Process for APD-Based PET Detectors," *Nuclear Science, IEEE Transactions on* , vol.54, no.3, pp.444-453, June 2007.

[7] Grybos, P.; Rodriguez, A.E.C.; Idzik, M.; Gaitan, J.L.; Prino, F.; Ramello, L.; Swientek, K.; Wiacek, P., "RX64DTH -a fully integrated 64-channel ASIC for a digital X-ray imaging system with energy window selection," *Nuclear Science, IEEE Transactions on* , vol.52, no.4, pp. 839-846, Aug. 2005.

[8] R. C. Lacoe, "Improving integrated circuit performance through the application of hardness-by-design methodology," IEEE Trans. Nucl. Sci., vol. 55, no. 4, pp. 1903–1925, Aug. 2008.

[9] Stassinopoulos, E.G.; Raymond, J.P.; , "The space radiation environment for electronics," *Proceedings of the IEEE* , vol.76, no.11, pp.1423-1442, Nov 1988

[10] Dodd, P.E.; Shaneyfelt, M.R.; Schwank, J.R.; Felix, J.A.; , "Current and Future Challenges in Radiation Effects on CMOS Electronics," *Nuclear Science, IEEE Transactions on* , vol.57, no.4, pp.1747-1763, Aug. 2010.

[11] Oldham, T.R.; McLean, F.B.; , "Total ionizing dose effects in MOS oxides and devices," *Nuclear Science, IEEE Transactions on* , vol.50, no.3, pp. 483- 499, June 2003.

[12] Hughes, H.L.; Benedetto, J.M.; , "Radiation effects and hardening of MOS technology: devices and circuits," *Nuclear Science, IEEE Transactions on* , vol.50, no.3, pp. 500- 521, June 2003.

[13] Schwank, J.R.; Shaneyfelt, M.R.; Fleetwood, D.M.; Felix, J.A.; Dodd, P.E.; Paillet, P.; Ferlet-Cavrois, V.; , "Radiation Effects in MOS Oxides," *Nuclear Science, IEEE Transactions on* , vol.55, no.4, pp.1833-1853, Aug. 2008.