Radiation Enhanced BSIM4 Model for UMC 90nm

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Introduction

Space is an unique place for electronics, due to the radiation interfering with their operation. Single Event Effects (SEEs) and Total Ionizing Dose (TID) are of major concern in CMOS designs for space. One of the issues faced is the limited number of tools available to design analog and mixed signal ASICs for the radiation environment. Radiation Hardened libraries already exist as well as TCAD simulators to simulate the radiation effects for a specific device. The problem lies in the lack of transparency the designer has, as to how radiation can affect his design at circuit level for a given technology used. The goal of this activity is to extend the standard SPICE compact models, to allow simulation of radiation effects parallel to the simulation of normal circuit behavior. To improve design efficiency the designer must have access to a number of radiation related variables. This work builds on work in the field by other researchers [1]. The goal of this work is to make the results on TCAD simulations be the ESA DESMICREX activity on umc 90nm [2] available on Cadence virtuoso, based on the latest developments in the field[3].

Theory

The two major effects studied were SET pulses and TID effects;

The SET is an effect that occurs when a proton or heavy ion collides with the device and specifically pn junction area inside the transistor.

a) A plasma track is created inside the semiconductor with electron-hole pairs.

b) The track creates a path of free carriers between p and n regions that can move to or from the positive n region, leading to a potential drop. This distorts potential gradients creating a field funnel.

c) Charge that is generated outside the funnel within its length diffuses to the junction.

Even though the SET phenomenon can be derived from first order equations modeling it with a semi empirical equation is more efficient. The charge injection into the device can be modeled by;

$$I = \frac{Q_c}{t_d - t_r}\left(e^{-t/td} - e^{-t/tr}\right) \qquad Q_c = \frac{\rho * LET * d}{3.6} * q$$

The above equation is referred to as the double exponential pulse. The technology and the device type determine the parameters td tr and d.

The TID sensitivity on the other hand can lead to threshold voltage shift and leakage currents. TID effects are mainly caused by trapped charges in oxide [6][7].

Leakage current due to corner parasitic transistors are modeled by;

$$I_{corner} = \begin{cases} \varepsilon\mu_{corner}\dfrac{W_{corner}}{L}*\left(V_{gs} - V_{th,corner} - \dfrac{V_{ds}}{2}\right)V_{ds}, V_{ds} < V_{gs} - V_{th,corner} \\ \varepsilon\mu_{corner}\dfrac{W_{corner}}{2L}*\left(V_{gs} - V_{th,corner}\right)^2, V_{ds} \geq V_{gs} - V_{th,corner} \end{cases}$$

$$V_{th,corner} = V_{fb} - \frac{Q_{trap}}{C_{ox}} + \frac{Q_B(2\phi_b)}{C_{ox}} + 2\phi_b$$

The technology and the device type determine parameters like Qb Cox Vfb while the trapped charge Qt is dependent on the radiation exposure.

Approach

There are two approaches for implementing radiation effects. One approach is the circuit level approach where you insert SPICE level circuit elements in order to simulate the effect [3]. Another approach is the compact model (CM) approach. With this approach you insert directly into a compact model of a device the radiation effects. BSIM4 [4] is an IGFET model developed by Berkeley and is one of the most widely used, and available CMs. We used a publicly available Verilog-A implementation of BSIM4 from Silvaco [5]. This generic implementation was configured for a UMC 90 nm low leakage version nMOS transistor.

The advantages of CM model approach are:

•Access to the equations and device parameters used in addition to the model parameters of the MOSFET.

•Inclusion of the current sources for better radiation modeling with respect to parasitics.

•Radiation behavior can be simulated without circuit modifications.

•Absence of foundry specific sensitive parameters such as doping profiles.

The disadvantage is:

•The speed of the Verilog-A model simulation is less than the Cadence implementation of BSIM4. This can be mitigated by choosing to replace the CMs of the sensitive transistors only.

Implementation

The SET double exponential pulse and TID leakage currents by parasitic transistors were implemented as presented in [6],[7],[8]. Some new parameters were also added, extracted from [2]. Radiation related input parameters are directly available to the user through device instance properties. The model has implementations for both source bulk and drain bulk pn junctions and it is possible to simulate 2 SETs together with TID leakage effects at the same time.
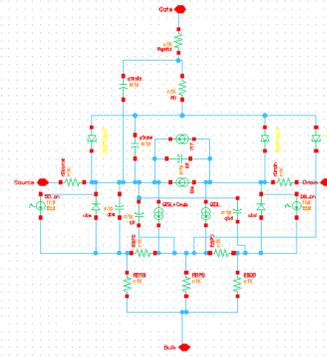
BSIM4 equivalent circuit with SET and TID effects
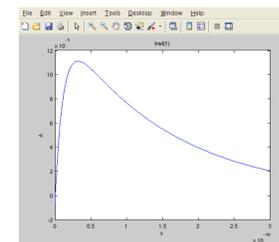

SET pulse simulation in Matalb
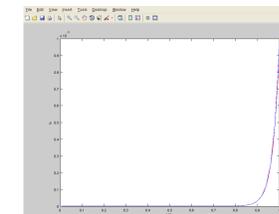
BSIM4 diode simulation in Matalb

In calculating the leakage currents the corner parasitic transistors have been assumed to have a greater impact than side forming transistors on STI layer. Accordingly only the corner leakage has been taken into account.

The position of the current sources simulating the effects, inside the equivalent circuit of BSIM4 and the Verilog-A internal nodes, is important. BSIM4 in its generic implementation allows a lot of freedom to the foundry using it, as to what kind of parasitics, noise models and internal phenomena need to be taken into account for a specific device. Depending on the implementation the model might use source and drain resistances or a resistor network for the substrate. Incorrect placement may lead to over or under estimation of the currents generated.

A debug mode was implemented to print internal parameters calculated in the model to verify the correct implementation of the radiation effects and its influence on the operation of the transistor. The output of the Verilog-A model has been compared to Cadence Model and to a dedicated BSIM4 Matlab model.

Results
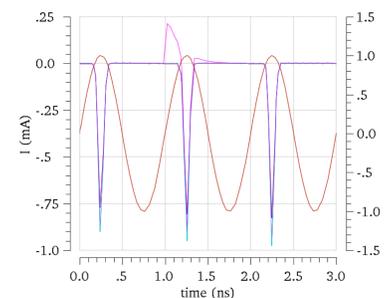
SET Pulse at 1ns with an LET of 30 Mev*cm^2/mg minimum sizing low leakage nMOS
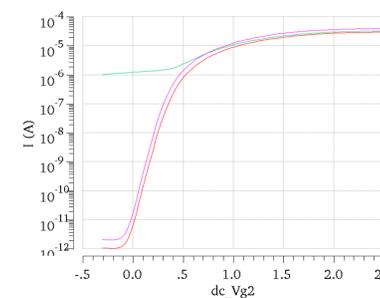
TID Leakage Currents Qt=100aC minimum sizing low leakage nMOS

Discussion

Effort was put into trying to constrain as many equation variables by the variables used in the model [9] and leaving the least degrees of freedom possible to the user.

The remaining parameters depend on technology and can vary widely e.g. the leakage current can vary over 2 orders of magnitude [10]. From the designer perspective the worst case is usually of the most importance. For the precise determination of the parameters TCAD simulations and/or Test Vehicle (TV) radiation measurements have to be performed.

For the SET td and tr parameters TCAD can be used to determine them, TVs have to be used to determine Qt for TID leakage and d for SETs.
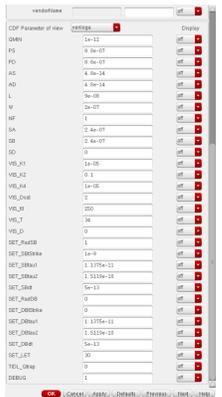
TCAD simulations have been undertaken with Cogenda[11] TCAD tool suite to extract the SET parameters. Information from different sources has been combined; device material measurements [2], device technology information and ITRS data. The 3-D doping profile reconstruction from 1-D measurement data and the device electrical characteristics is still in progress.

Rad Model Instance Properties

Conclusions

Radiation effects both TID and SET have been successfully implemented in the BSIM4 model. This allows simulation of the SET pulses as well as TID leakage effects. The SET, TID model parameters for the Low Leakage nMOS transistor have been determined. Further work on TCAD for SET pulse parameters as well as radiation tests on test vehicles is needed to increase the accuracy of these parameters. Additional work has to be conducted in order to determine dependence of the parameters on device type and geometry.

References

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