Design of a Radiation-Hardened Controller Area Network (CAN) Transceiver in .35µ Triple-well CMOS

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Introduction

In recent years there has been a drive to promote the use of the CAN bus for communications in space-borne avionics systems. In contrast to the MIL-1553 standard, the CAN bus is a 'democratic' message distribution system in that each node is able to receive each CAN message, i.e. all CAN nodes broadcast on the same bus lines. This reduces the number of I/O connectors required to implement the communications system. Additionally, MIL-1553 consumes much more power than CAN, a key performance advantage for space systems. Despite these advantages, there is no commercially available CAN transceiver which is hardened against the effects of the radiation.

To achieve radiation hardness, this design is undertaken using enclosed layout transistors from the Design Against Radiation Effects (DARE) library. Although the layout of these devices ensures a high level of immunity against total ionisation dose (TID) effects, the fact that the library uses a 180 nm bulk CMOS process (UMC) has important implications for the design of a CAN transceiver. In particular, several of the electrical requirements outlined in the 1 Mbit/s CAN ISO 11898-2 standard [1] imply a tolerance to high voltages. For example, the common-mode voltage of the bus ranges from a minimum of -2 V to a maximum of 7 V. Since the highest voltage transistor in the library is rated to 3.3 V, a number of design techniques must be employed to design a circuit which conforms to the physical layer standard.

CAN Description

The controller area network, pictured in Figure 1, is a 'democratic' message distribution system. All nodes on the network share the same two transmission wires which are terminated at each end of the bus by a 120 Ω resistor. Using these shared lines, each node on the network is able to receive each message broadcast on the bus. Likewise each node is able to access the bus to transmit a message. To avoid message collisions which would result from multiple nodes transmitting simultaneously, the bus undergoes an arbitration process at the start of each message whereby bus access is granted to the message with the highest priority.

Nodes are able to transmit messages on the bus by alternating between two states, see Figure 2. In the dominant state, the CANH and CANL pins enter a low impedance state and a differential voltage is seen between the two bus lines equal to

$$V_{diff} = V_{CANH} - V_{CANL}.$$

In the recessive state, the CANH and CANL pins maintain a high impedance state whereby Vdiff is approximately 0 V. This implies that a recessive state can be 'overwritten' by a dominant state, a key requirement for bus arbitration.

Since the CAN bus was originally conceived for automotive applications, the electrical requirements for the physical layer, as defined in ISO 11898-2, are stringent with regards to the conditions the transceiver should be able to operate in. A few of these in particular can cause problems when trying to implement a transceiver in 3.3 V bulk CMOS. For example, the common-mode range, V_{CM}, lies in the range $-2\text{ V} \le V_{CM} \le 7\text{ V}$, necessitating the need for protection devices to stop current flowing through the body to drain junction diode when the common-mode voltage lies outside the range of the power supplies.

Typically, this protection is achieved using diodes [2], see Figure 3. For this CMOS process, it was found that the forward voltage drop of the diodes was incompatible with the requirements for the differential output voltage. Therefore, a solution which is compliant with both requirements, as well as the remaining requirements in ISO 11898-2, without the use of protection diodes is required. For clarity a selection of the most relevant requirements for a low voltage transceiver are described.

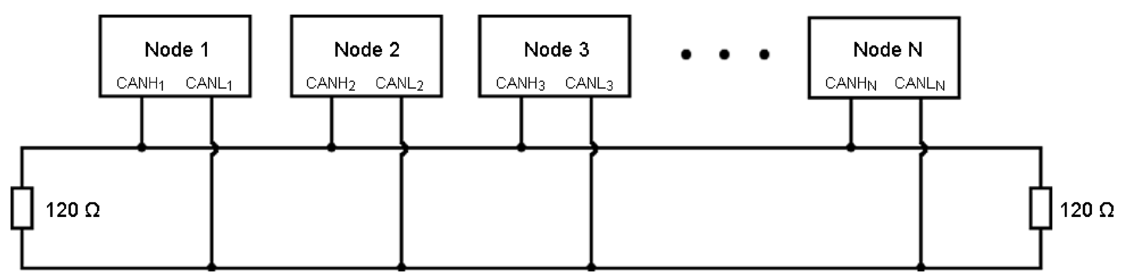

Figure 1. CAN BUS

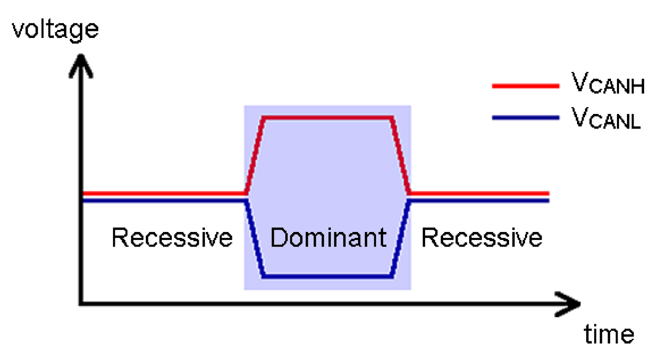

Figure 2. CAN States

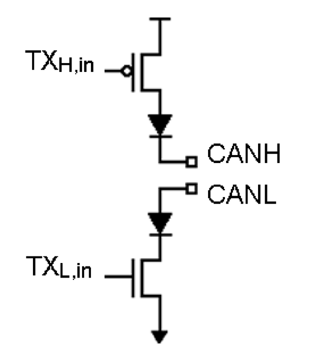

Figure 3. Typical CAN Transmitter

CAN ISO 11898-2 Requirements

Output Voltages

During the dominant state the differential voltage between the CANH and CANL of the transmitting node must comply with the voltage levels in table 1. The corresponding differential voltage levels for the recessive state are shown in table 2.

Parameter	Notation	Unit	Value		
			min	typ	max
Output bus voltage	V_{CANH}	V	2.75	3.5	4.5
	V_{CANL}	V	0.5	1.5	2.25
Differential output bus voltage	Vdiff	mV	1.5	2	3

Table 1. Output voltages during dominant state

Parameter	Notation	Unit	Value		
			min	typ	max
Output bus voltage	V_{CANH}	V	2	2.5	3
	V_{CANL}	V	2	2.5	3
Differential output bus voltage	Vdiff	mV	-500	0	50

Table 2. Output voltages during recessive state

Input Resistance

To maintain a low differential output voltage during the recessive state, the resistance seen looking into each bus node, Rin, must be compliant with the values given in Table 3 over the common mode range. Furthermore, the internal resistances seen looking into both CANH and CANL of a node must match to within 3 % relative to each other.

As well as an internal resistance looking into CANH and CANL of each bus node, there is also a resistance seen between these two pins, the differential internal resistance, Rdiff. For compliance with ISO 11898-2 the value of Rdiff must be compliant with the values in table 3.

Parameter	Notation	Unit	Value		
			min	typ	max
Internal resistance	R_{in}	kΩ	5		50
Differential internal resistance	R_{diff}	kΩ	10		100

Table 3. Internal resistances during recessive state

Common-Mode Range

To account for relative ground shifts between nodes as well as common-mode noise, a CAN transceiver must be designed to operate over a common mode voltage of -2 V to 7 V. When the bus is fully loaded, the voltages at the CAN node outputs must be compliant with the values in Tables 3 and 4, for the respective recessive and dominant states.

Parameter	Notation	Unit	Value		
			min	typ	max
Common mode bus voltage	V_{CANH}	V		2.5	7
	V_{CANL}	V	-2	2.5	
Differential bus voltage	V_{diff}	mV	-120	0	12

Table 3. Bus voltages during recessive state

Parameter	Notation	Unit	Value		
			min	typ	max
Common mode bus voltage	V_{CANH}	V		3.5	7
	V_{CANL}	V	-2	1.5	
Differential bus voltage	V_{diff}	mV	1.2	2	3

Table 4. Bus voltages during dominant state

Maximum Ratings

The CANH and CANL pins on each CAN node should be able to withstand a short-circuit to the voltages displayed in table 4. During this short circuit condition, operation of the circuit does not have to be guaranteed, only that the circuit should survive.

Nominal Battery Voltage (V)	Notation	Unit	Value	
			min	max
12	V_{CANH}	V	-3	16
	V_{CANL}	V	-3	16

Table 5. Maximum ratings of V_{CANH} and V_{CANL} of a CAN node

3.3 V CMOS CAN Transceiver

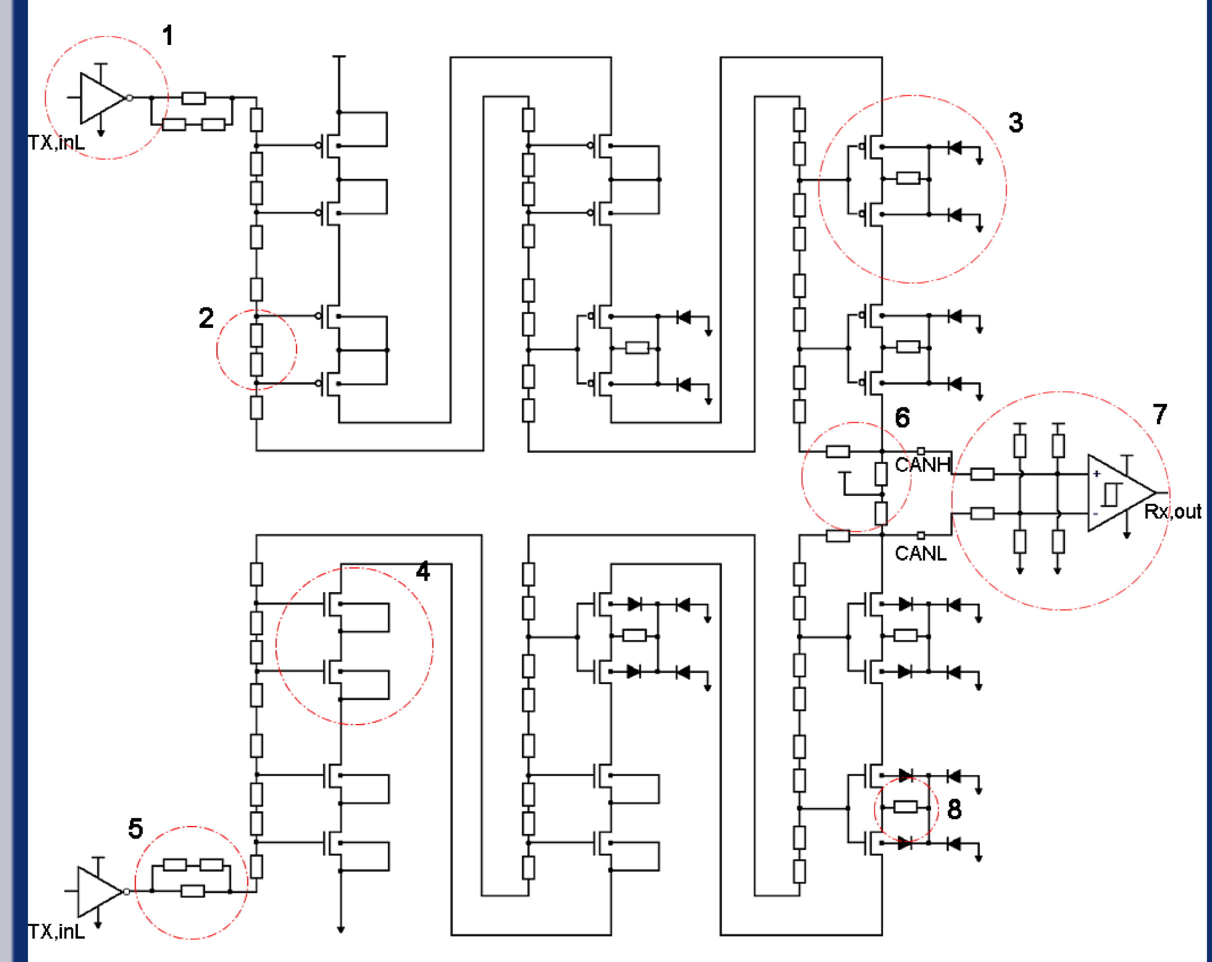

Figure 4. Low Voltage CMOS CAN Transceiver

Design Features

1. State Differentiation

The resistor strings which bias the gates of both the pmos and nmos driver strings are driven by the outputs of inverters which always maintain opposite polarities. This enables the differentiation of the two states of the CAN bus. In the dominant state, the pmos inverter output goes to ground and the nmos inverter goes to vdd, turning the transistors on. In the recessive state, the inverter outputs swap polarities and the transistors are off, maintaining a high impedance state.

2. Recessive Input Resistance

The resistors in the strings are sized such that the minimum internal resistance of the CAN specification can be met, and distributed between the gates of the transistors such that the gate to source voltage of each transistor ensures that it is off during the recessive state.

3. Reverse-current blocking

Traditionally, diodes would be connected in series with a driving transistor to prevent current flowing through the drain-body junction when the bus voltage drops below ground, or rises above vdd. In this process, the forward drops of the diodes were found to be incompatible with the minimum differential voltage during the dominant state, therefore a different approach was needed. By connecting the body of adjacent transistors to the connection between the source and drain, a series connection of a forward-biased diode and reverse-biased diode is formed. By connecting a string of these devices between the bus and the power supply, the reverse-current is limited to acceptable levels.

4. Input Resistance Matching I

Whilst connecting the body of adjacent pairs of transistors to the node which connects the source and drain ensures a forward biased diode and a reverse biased diode, using this configuration alone will not meet the specifications for Rin.This is due to a disparity between where the power supplies are in relation to the extremes of common-mode voltage. For example, in the nmos driver body-drain leakage will dominate internal resistance degradation for voltages from ground to -2 V, and I_{DS} leakage dominates the internal resistance from ground to 7 V. Since the degradation at 7 V is greater than at -2 V, additional transistors at the lower end can have their body connected to their source, reducing the extent of I_{DS} leakage.

5. Input Resistance Matching II

Variations in the threshold voltage of pmos and nmos transistors will not track, therefore an additional resistor is required to tune the voltages on each side of the driver such that the input resistance will match to within 3 % over the extent of the common-mode. This additional resistor is formed using the same unit resistor as the rest of the string, ensuring that it will track over PVT.

6. Recessive Common-Mode Shift

During the recessive state the common-mode voltage must lie between 2 and 3 volts. Since the resistance looking into both CANH and CANL must be matched to within 3 %, this shift is achieved by connecting CANH and CANL to the power supply via two resistors.

7. Receiver Resistive Divider

A resistive divider reduces the voltage at the input of the receiver to a level which is compatible with the oxide breakdown voltage of the transistors at the receiver input.

8. Substrate-current Leakage Mitigation

If the bus voltage is taken below ground and the CAN node is in the recessive state, the substrate to nwell diodes will become forward biased and begin to conduct. Resistors are used to limit the current such that the input resistance requirements can still be met for negative voltages. Care is taken to ensure that the wells can still be charged in a time scale which is compatible with the transient reqirements of the standard.

Results

The floating well structure achieves the required voltages to differentiate between the recessive and dominant states, see Figure 5. The requirements for output voltages when the bus is fully loaded, noted in Tables 3 and 4, can be simulated using a model [3] of the CAN bus which takes into account the common-mode voltage and the internal resistance of the remaining CAN nodes. At the extremes of common-mode voltage, the driver achieves the required voltages over PVT. Figures 7 and 8 illustrate matching of the internal resistance over the common-mode range.

When one of the bus lines is shorted to the maximum ratings the circuit will only survive for a satisfactory time period when in the high impedance recessive state. There is a nominal leakage current (~50 mA), and the resistor strings maintain the gate voltages below the oxide breakdown voltage. To ensure the driver enters the recessive state when the bus lines are shorted to the maximum ratings, additional over-current detection circuitry is added. When an over-current condition is detected in the dominant state, the driver will automatically revert to the recessive state.

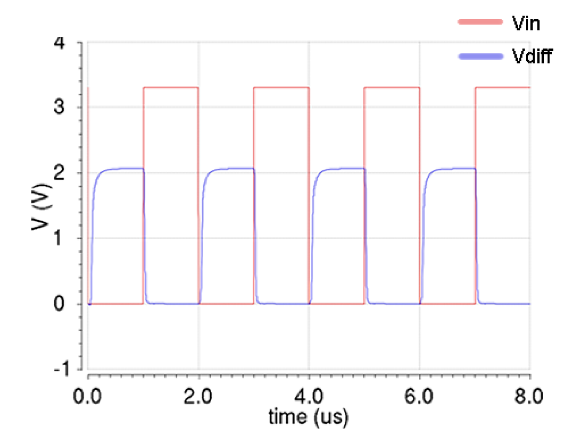

Figure 5. Differential output voltage

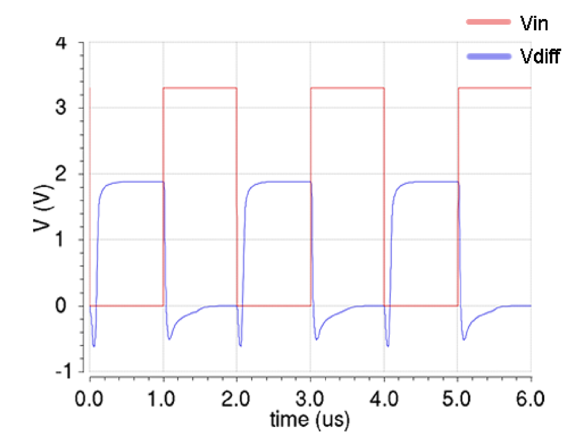

Figure 6. Output bus voltage with a fully loaded bus, V_{CM} = 7 V

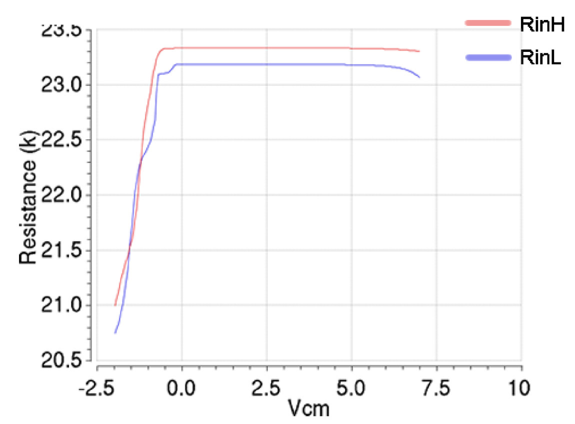

Figure 7. Input resistance for $V_{CANH} = V_{CANL}$

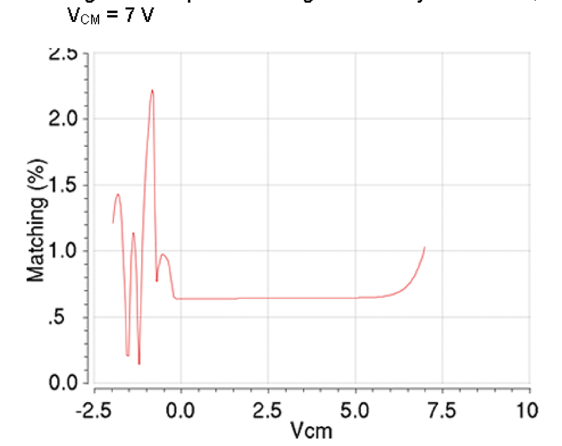

Figure 8. Input resistance matching for $V_{CANH} = V_{CANL}$

References

[1] ISO 11898-2, Road vehicles - Controller area network (CAN), Part2: High-speed medium access unit, International Organization for Standardization, 2003

[2] TJA1040 High speed CAN transceiver [Datasheet], Phillips Semiconductors, October 2003

[3] SN65HVD230 3.3 V CAN Transceivers [Datasheet], Texas Instruments, January 2009