Caen Aurelia Space

Caen Aurelia Space Reorganization

- Merger between CAEN Aerospace and Aurelia Microelettronica Space Activities on December 2009.
- Transfer from CAEN Network to Angelo Investments on May 2010.
- Angelo Investments Roadmap:
  - Resources:
    - Reinforce the Viareggio/Pisa Premises
    - Establish new Premises in Bari
    - Strong synergies between Angelo INV Companies in Aerospace field.
  - Facilities:
    - New Building in Bari for Angelo INV Companies -> 14000 m^2
    - Qualification of production line for space activities
    - 2 Class 100 and 2 Class 100000 Clean Rooms
    - Anechoic Chamber (under construction)
    - Mechanical Test Facility (under construction)
- All commitments and undertakings will be maintained

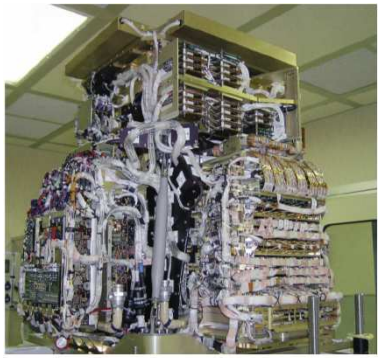
A new name for the Company is expected to become effective in October 2010, all Customers and Suppliers will be formally informed by letter.

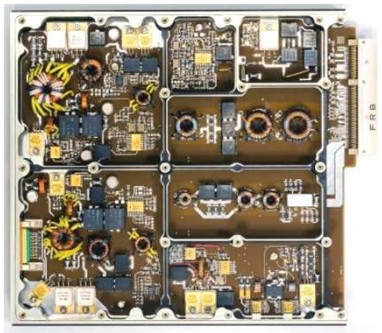
Caen Aurelia Space

Caen Aurelia Space Current Activities

Angelo Investments

Space to Innovation & Micro-Art of Technology





Design, Manufacturing, Assembly and Test of space-oriented electronics:

Power supply electronics

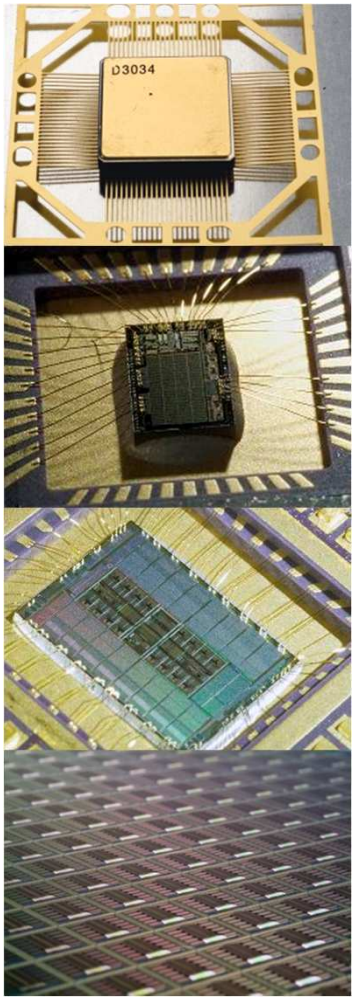
- DC/DC Converters
- Power Distribution and Conditioning Units
- Low and High Voltage Power Supply Systems
- HV Power Supply Systems for Electrical Propulsion

Cooler Drive Electronics for Cryocoolers

Front-end Electronics

Payload Data Handling/ Processing Units

SpW/CAN/1553 Multi-bus Boards



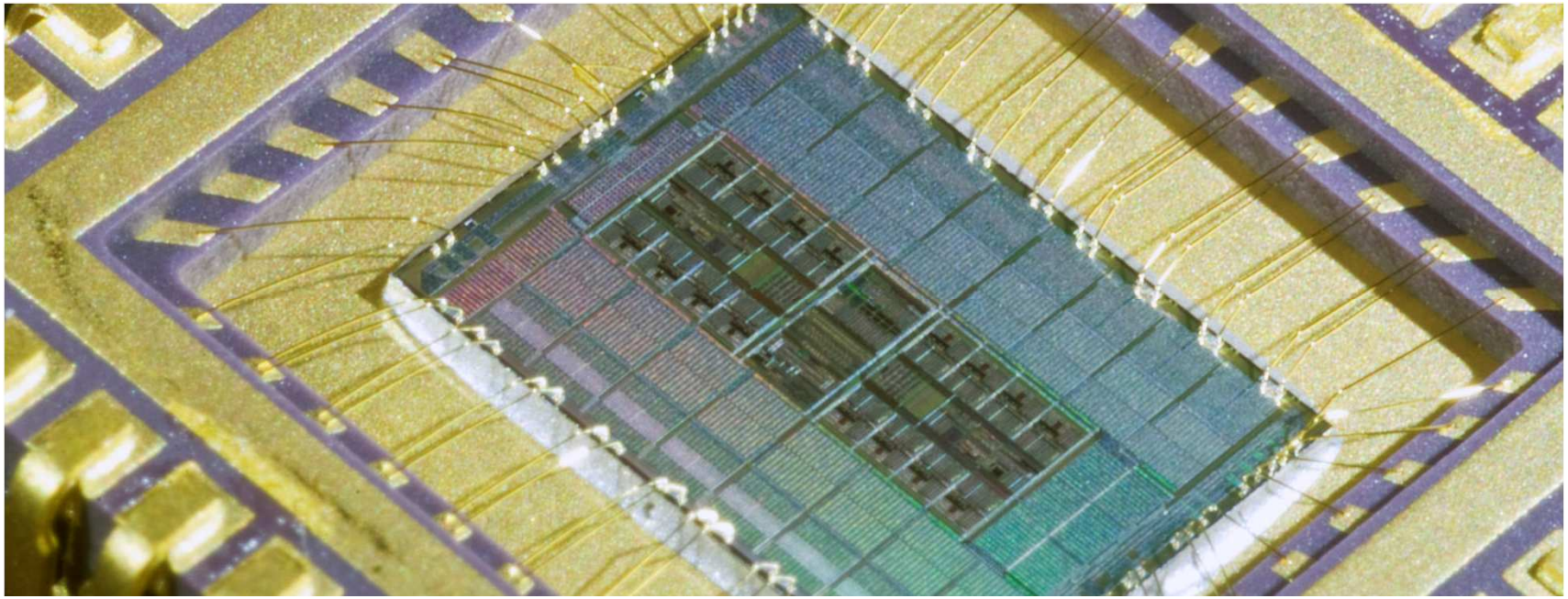
Design and Production of rad-tolerant microelectronic devices:

Custom ASICs

- CANbus controller and transceiver
- MIL-STD-1553 transceiver
- SEL protection
- Front-end and ADC

Complex FPGA Fitting

- SpaceWire Bridges
- LEON uC
- CANopen Controller
- Cryptography systems
- DSP



Mixed-Signal ASIC for High Power Commands Management

Noordwijk, The Netherlands
September 7th, 2010

Bigongiari F., Chicca S., Nurra V., Tuccio G.
CAEN AURELIA SPACE

Esposti M.L., Mattavelli M.
THALES ALENIA SPACE ITALIA

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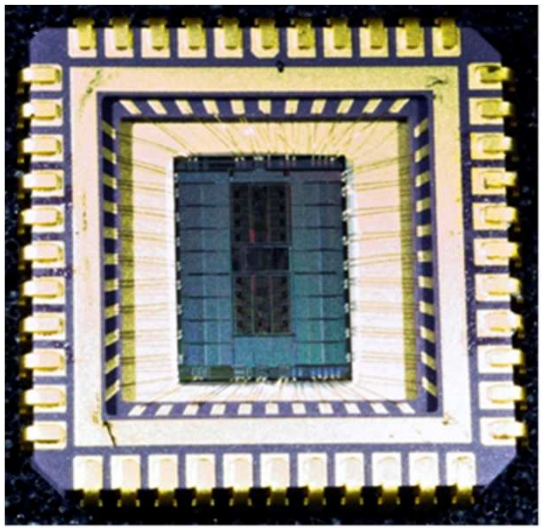
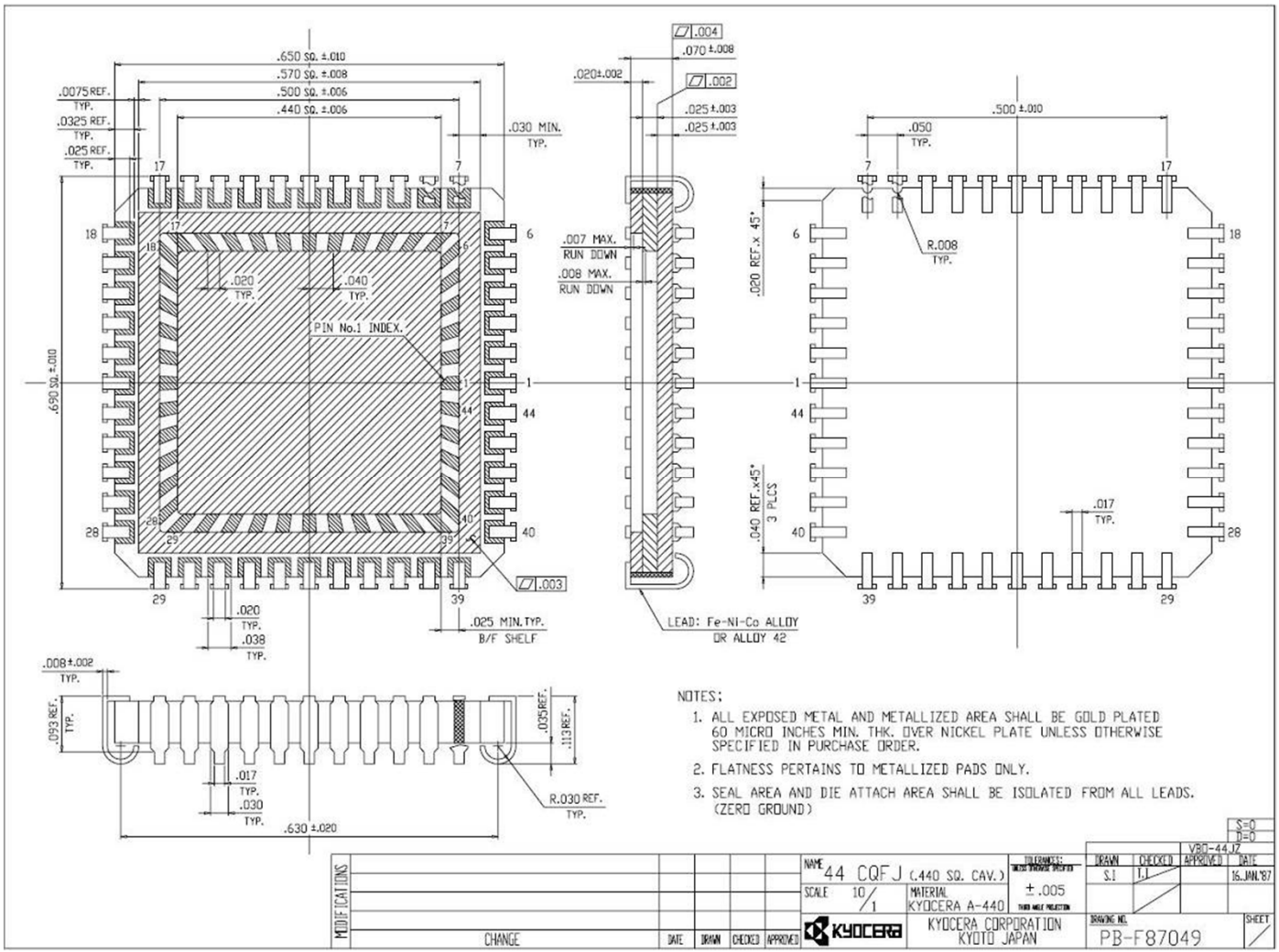
16HPCMD ASIC



- CAEN AURELIA SPACE is subcontractor of THALES ALENIA SPACE ITALIA
- Primary application within platform and payload control of Thales Alenia Space Data Handling equipments
- First delivery of 80 FM for SENTINEL-1 Mission

in charge of generating "High Power ON/OFF" discrete Commands, widely used on board spacecrafts, to switch equipments to ON or OFF status, and to select specific operating modes

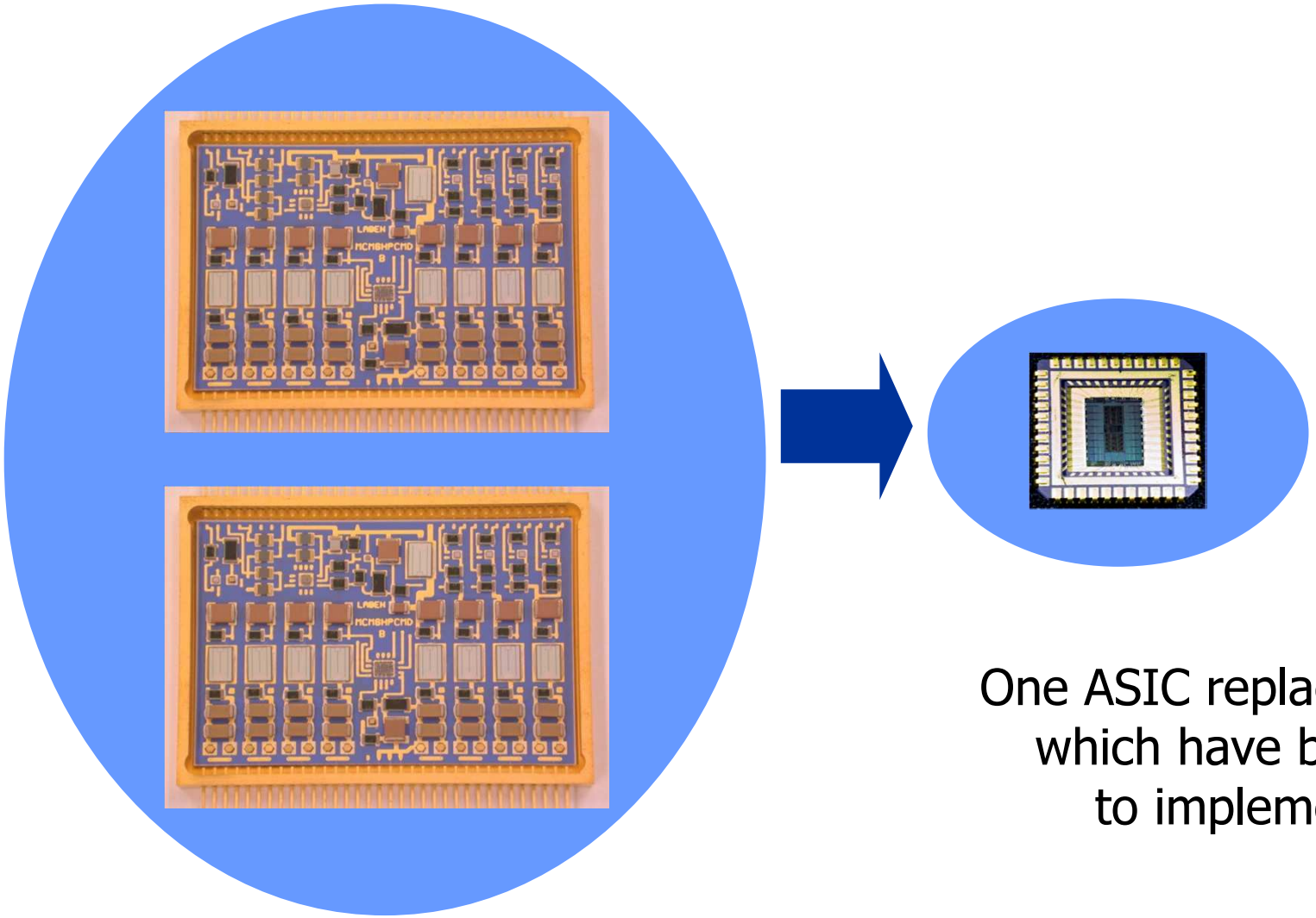
TECHNOLOGY & PACKAGE



XFAB 0.6um BiCMOS SOI-HV technology

JLCC 44 (KYOCERA PB-F87049 with anti-bleeding)

Miniaturization



One ASIC replaces two Hybrids
which have been used so far
to implement the function

High Power Commands (1)

Definition from ESCC-E50-14A:

"The high power pulse (HPC) command interfaces are intended for load driving interfaces and, for example, can be used to switch relays or similar loads.

The high current capabilities of these interfaces lead to their protection against short circuiting and against failure in a high current mode.

The high power pulse command consists of a single signal, HPC_OUT(H), generated by the core element. This is connected by a single ended circuit to the input at the peripheral element.

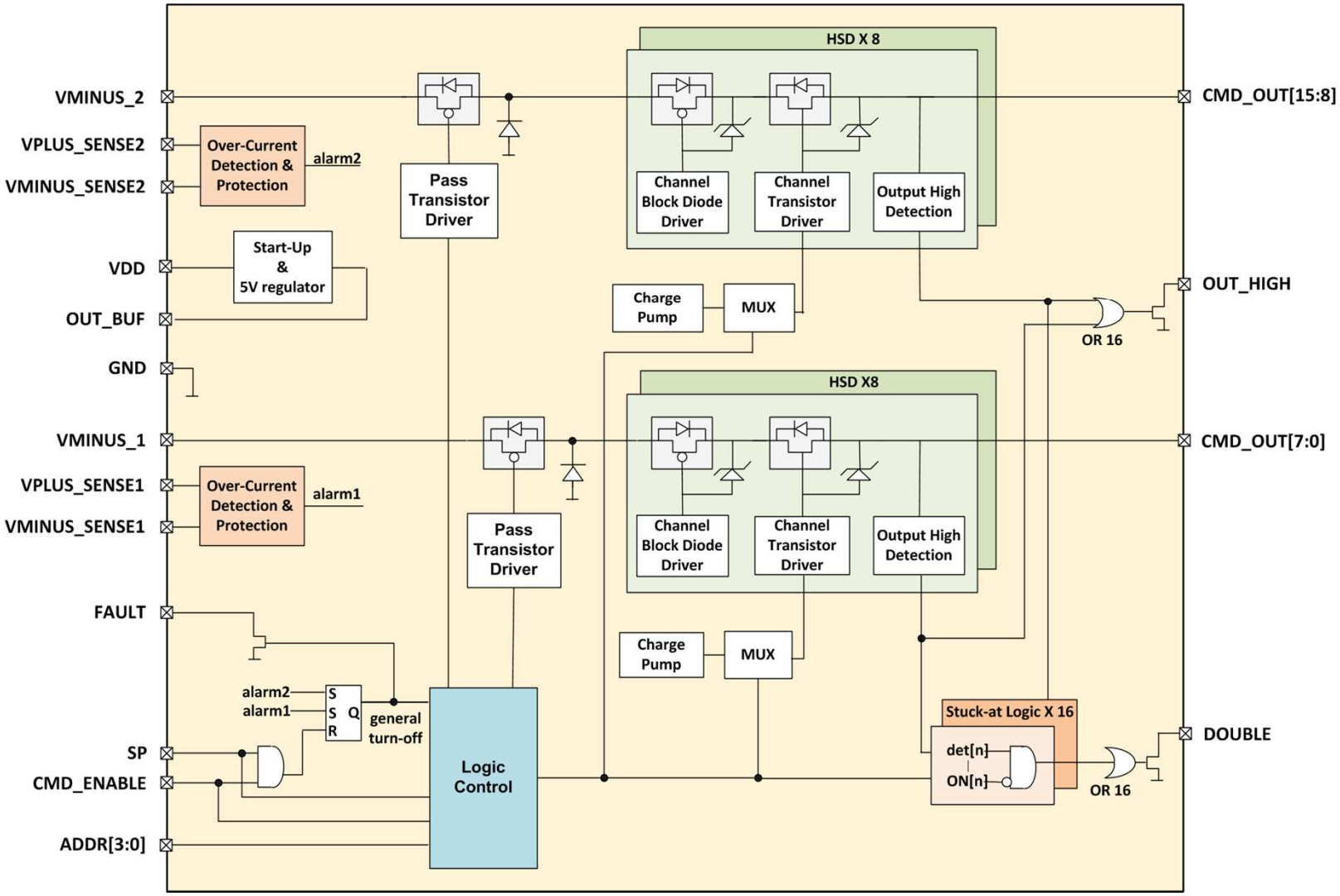
The interface is entirely controlled from the core element."

High Power Commands (2)

16HPCMD ASIC consists in 16 high side driver (HSD) channels able to drive low voltage (LV), high current (HC) and high voltage (HV) inductive or resistive loads connected between the power output pins and external ground

	LV - HPC	HV - HPC	HC - HPC
Active state output voltage	**12 V to 16 V**	**22 V to 29 V**	**22 V to 29 V**
Active current drive capability	**180 mA**	**180 mA**	**600 mA**
Pulse width	**4 ms to 1024 ms (system design selectable depending on receiver characteristics)**		
Output voltage rise and fall times	**50 µs to 2 ms (when connected to a resistive load of 100 Ω)**		

BLOCK DIAGRAM



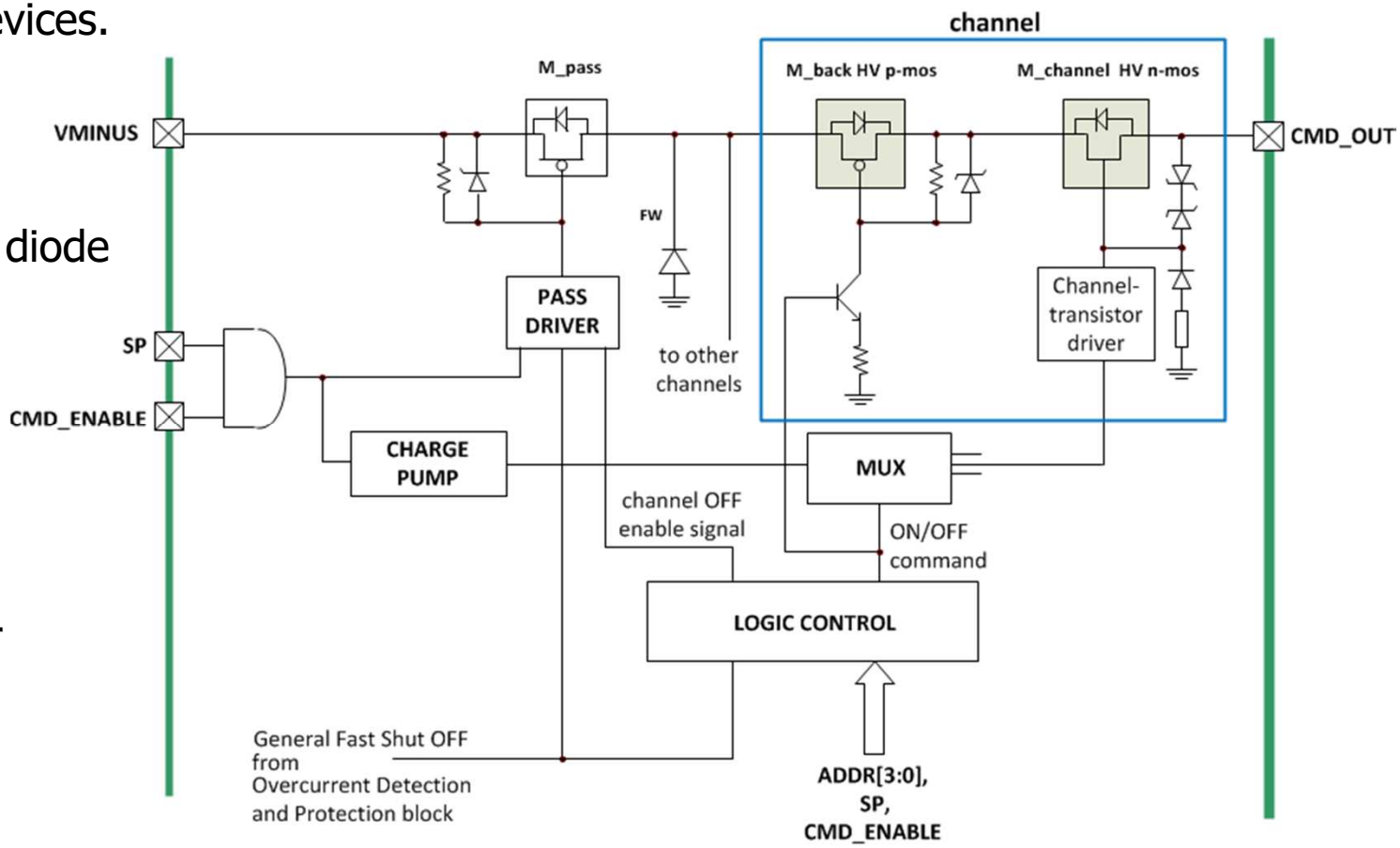
Building Blocks

- 2 command issuing sections independently powered by one input power line, each one composed by 8 channel outputs.
- 2 current sense controls to limit the maximum current that can flow through the ASIC on the load
- Over Voltage Protection circuitry
- Output High Detection circuitry
- Double Command Detection circuitry
- 4 digital input ADDR[3:0] to address 1 out of 16 outputs.
- 2 control signals for ASIC selection (SP, CMD_ENABLE)
- 3 digital output signals to monitor the ASIC status (FAULT, OUT_HIGH and DOUBLE)

Command Issuing Section

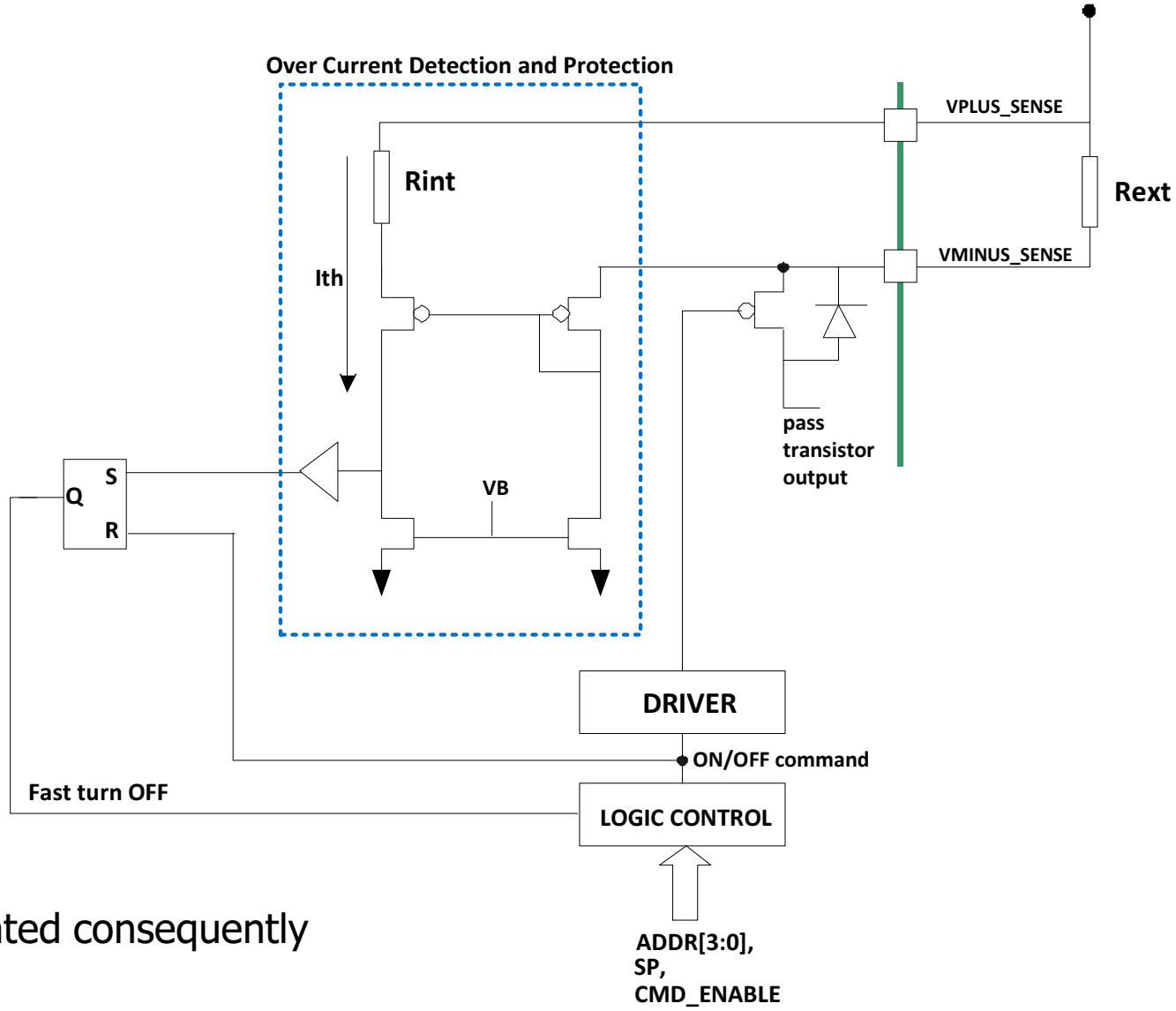
The channel structure with **3 pass transistors connected in cascade** has been chosen in order to have **high reliability** against single failure on the pass transistors, and allows a **wired-OR** connection among different devices.

- Pass transistor
- Under-ground-free-wheeling diode
- Charge pump
- Shift level / MUX
- Single channel:
  - ✓ Active blocking diode
  - ✓ Channel-output power transistor
- Combinational logic



Sensing & Warnings Section (1)

The ***Over Current Detection & Protection*** block is in charge of generating a **general shut OFF** as a logic signal to the Control Logic to force a fast turn OFF of the pass transistor and the presently addressed channel (disregarding the ON external command on the digital IF) upon the pass transistor current overcomes a certain internally generated threshold.

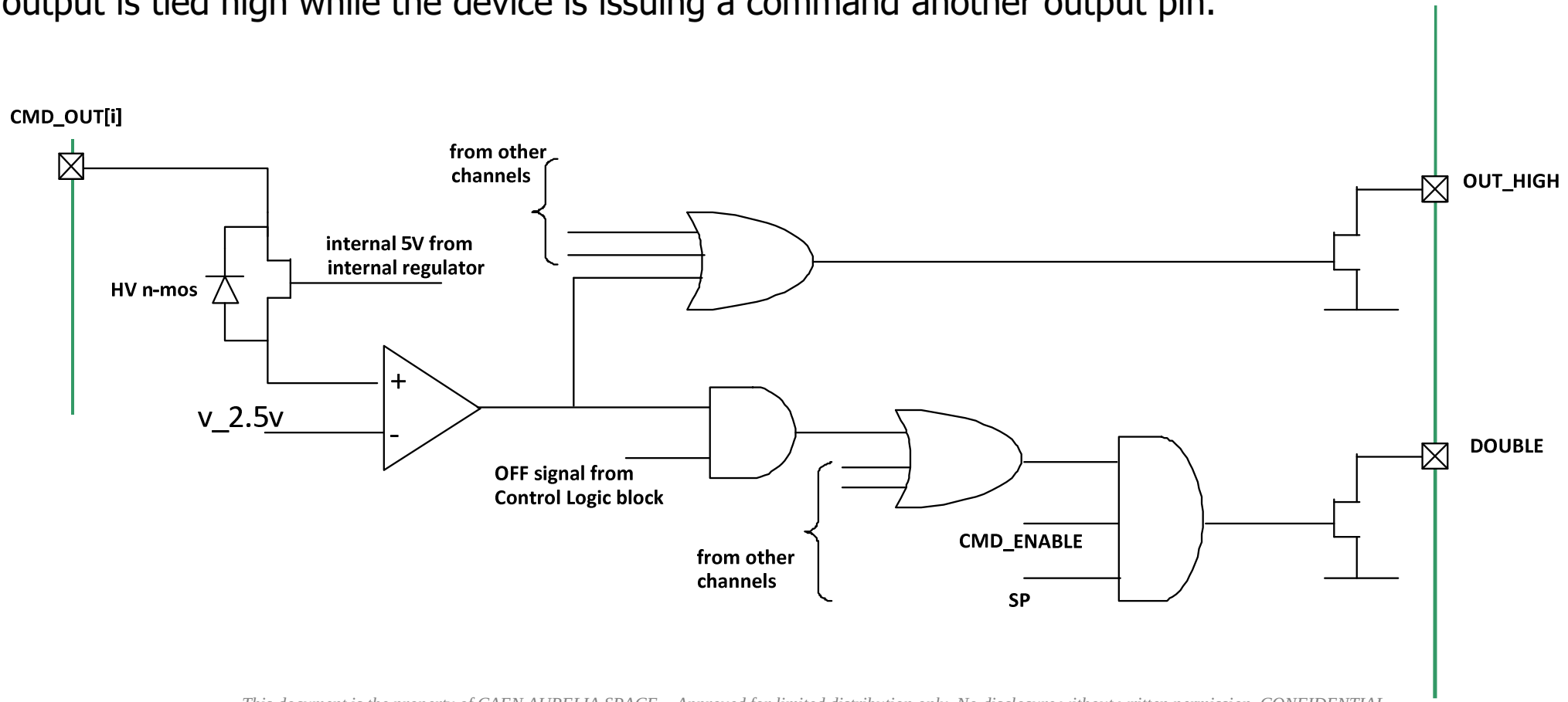


A status signal **FAULT** is generated consequently

Sensing & Warnings Section (2)

Inside each channel, an ***Output High Detection*** circuitry provides a logic signal when the output voltage overcomes a certain internal threshold. **OUT_HIGH** is active if a command has been issued.

The ***Double Command Detection*** aims to warn on a dedicated pin **DOUBLE** that a not addressed output is tied high while the device is issuing a command another output pin.



Service Section

The **charge pump** block is a 3-stage standard charge pump working at 250KHz frequency.

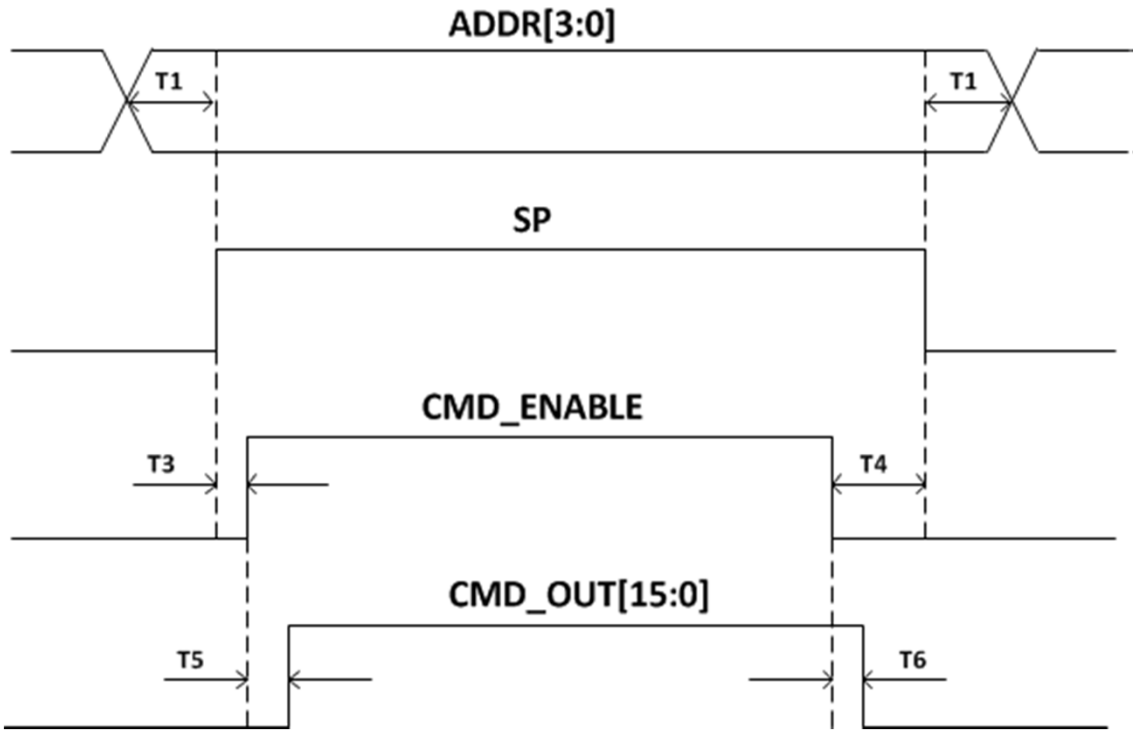
It is activated upon the CMD_ENABLE and SP signals go active, only if the address input signals ADDR[3:0] are codifying one of the 8 channels served by the charge pump itself.

The **5V internal regulator** provides supply for the logic section and for low-voltage analogue blocks.

A **buffered internal bandgap**, supplied by the low-voltage 5V VDD external Power Supply, is provided on OUT_BUF output pin. In order to adjust the rising/falling edges on sixteen CMD_OUT outputs, an external resistance is connected between OUT_BUF and GND pins.

Digital Interface

The parallel digital interface composed by the channel-address logic (ADDR[3:0]), the command enable (CMD_ENABLE) and the sample (SP) signals, guarantees that only one channel out of 16 channels at a time is activated.



The ASIC is issuing a command only when CMD_ENABLE and SP input signals are both active high: it is not issuing a command when CMD_ENABLE or SP signal is low.

Radiation Hardening By Design

Since the technology selected is used for automotive applications, special techniques have been adopted in order to increase the radiation hardness.

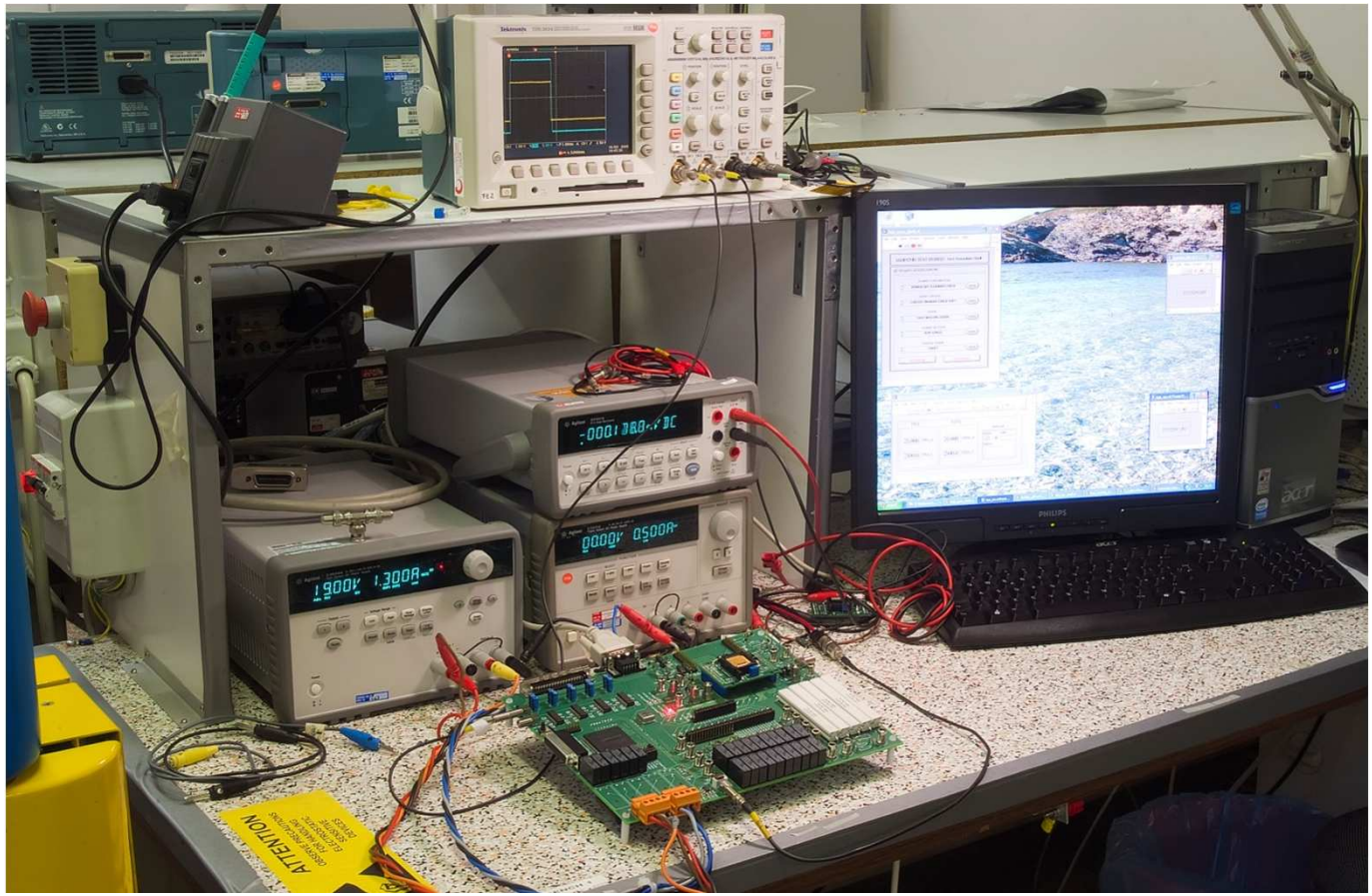
Being an SOI process the immunity against **SEL** effect is good, but particular attention has been taken in order to totally eliminate the parasitic NPN transistor between power supply and ground that is intrinsically formed when a PMOS transistor is built inside a P-well region.

To increase the hardness to **SEU**, a TMR module has been added for each flip-flop, whereas the hardness to **SET** has been mitigated using adequate threshold for the comparators.

The **TID** effects have been mitigated by design (i.e. increasing the comparator threshold) and layout techniques.

Electrical Test

A dedicated test setup has been developed in Labview™ environment.

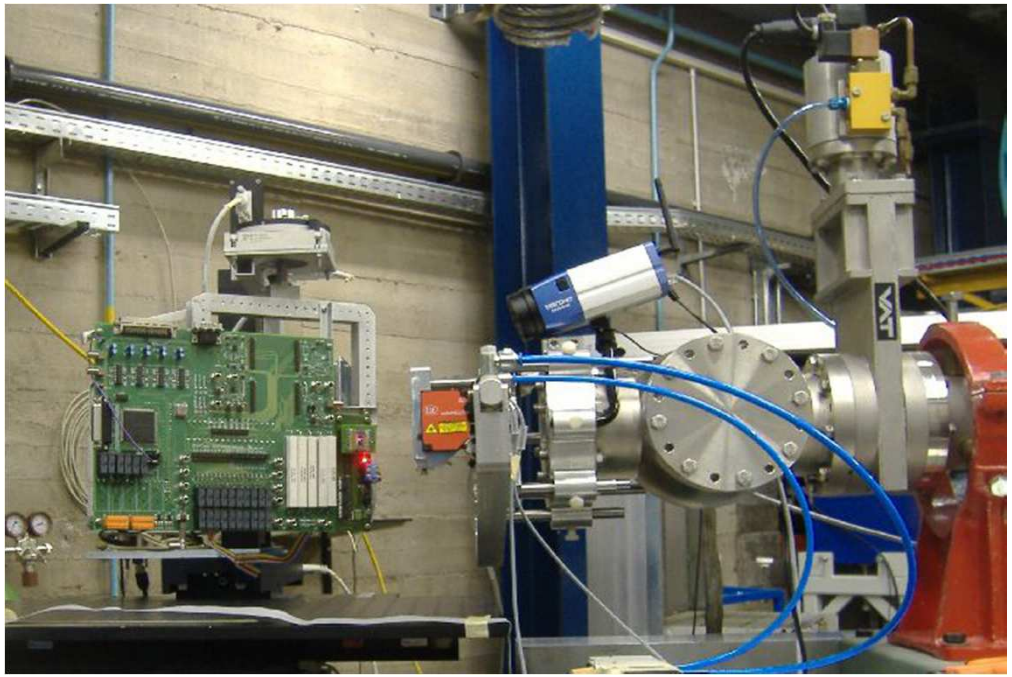


The ASIC has been tested at room, +125 C and -40 C and in the entire power line voltage and output load range.

The results of electrical tests confirmed the correctness of ASIC behaviour.

Radiation Test

The ASIC has been tested under radiation to evaluate its performance.



SEE tests with heavy ion have been performed up to 70 Mev, confirming immunity to Latch-up. Some transients have been observed, having however very low probability to occur (one command over 10 billions could be in principle affected in a typical GEO environment).

The **TID** tests with CO^{60} have been performed in both biased and unbiased modes. Biased devices shows full performances up to about 15 kRad, while unbiased samples can tolerate more than 50 Krad.

Screening and Qualification

A screening and qualification campaign to obtain the flight models for Sentinel-1 is on-going and should be concluded on the end of next November.

Considering that the technology selected is not a qualified process, in order to have a first selection of the good parts, a wafer probe test and a preliminary electrical test at the three temperatures (25°C, 125°C, -40°C) are performed respectively on wafers between manufacturing and packaging and on packaged parts between assembly and screening.

The first lot has already been screened with excellent results in term of parameters drift and total of defective parts.
(*only 2 defective parts over 90 components*)

FM Packaging

- Body & Lids Inspection
- Die Visual Inspection
- Die Attach & Wire Bonding
- Bond Strenght
- Die Shear
- Internal Visual Inspection
- Hermetic Sealing
- Serialization
- External Visual Inspection

ASIC packaging has been performed in accordance with the standard flow from ESCC Generic Specification No. 9000.

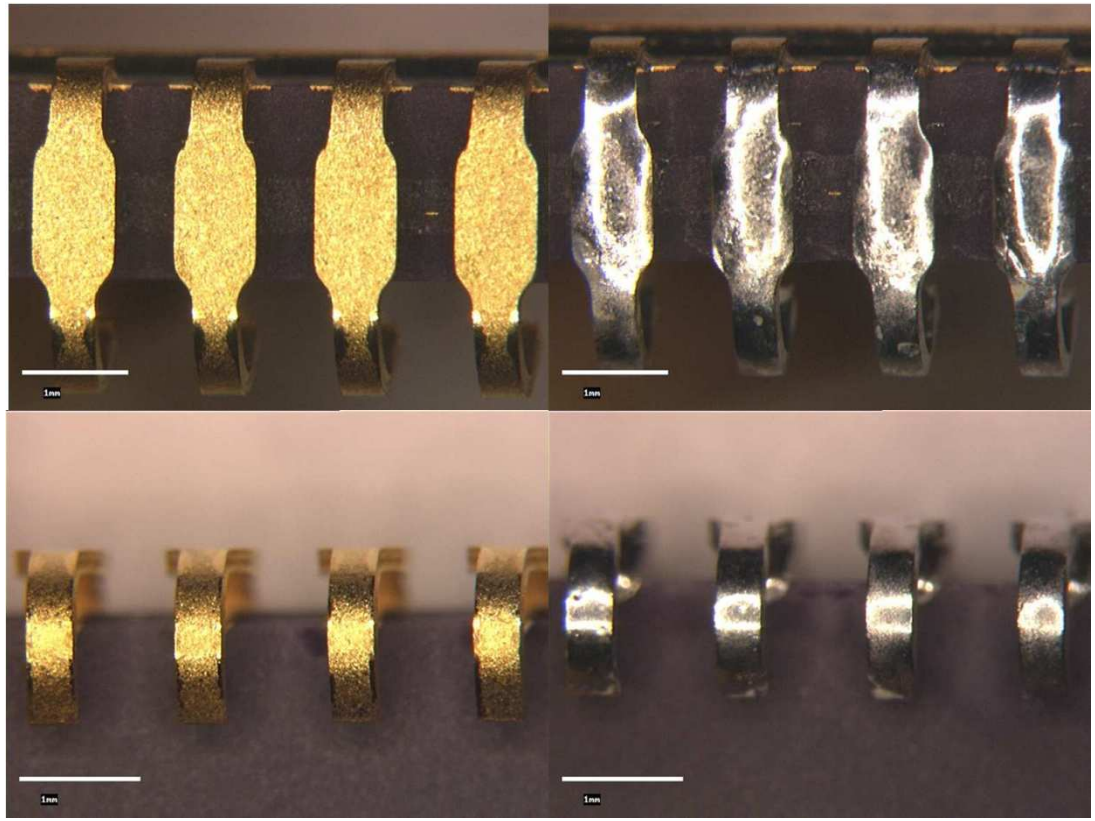
All parts have been marked with manufacturer and product name, date code and serial number.

An RGA analysis has been additionally performed, immediately after packaging.

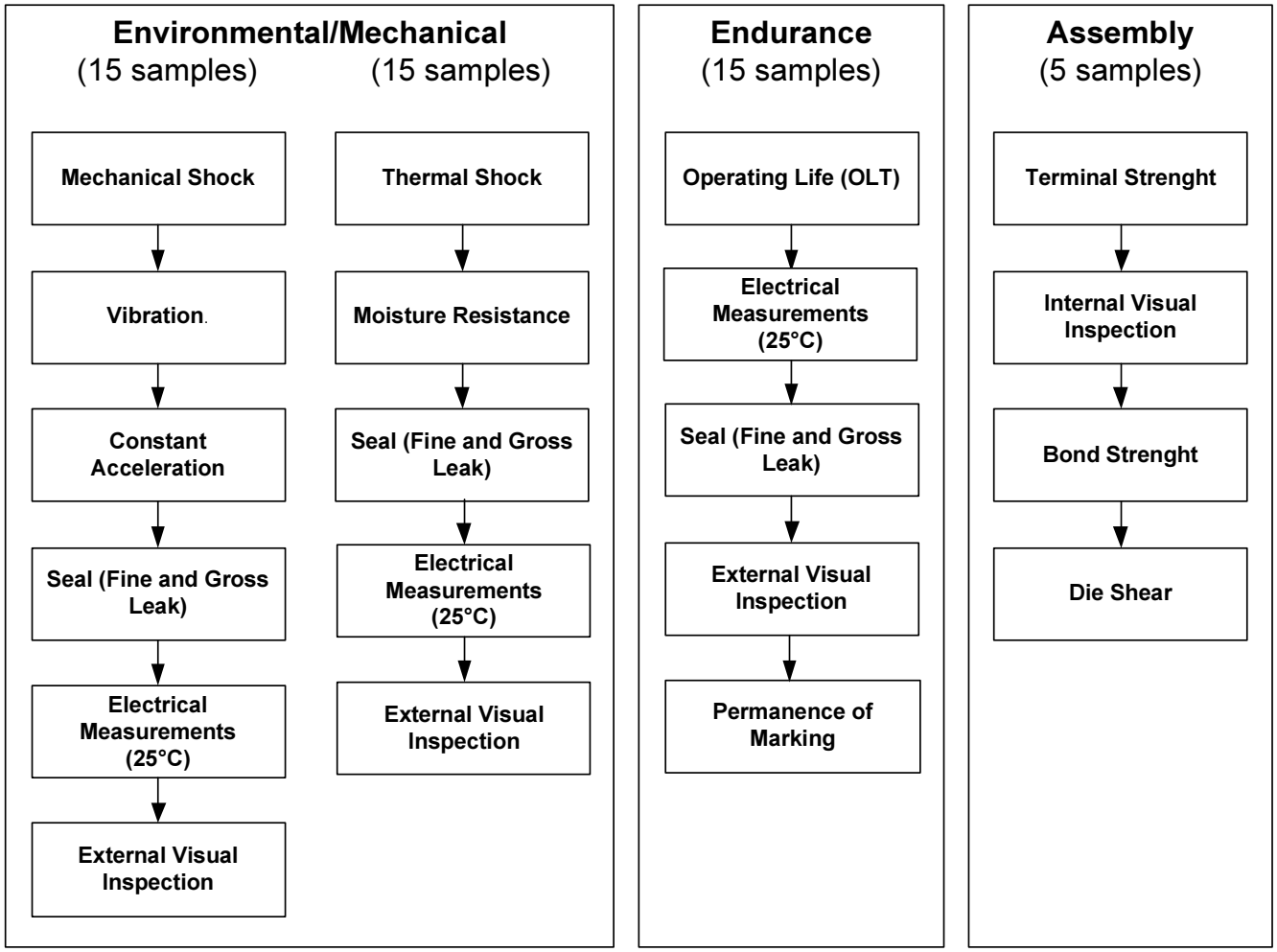
FM Screening

- High Temperature Stabilisation Bake
- Temperature Cycling
- Particle Impact Noise Detection (PIND)
- Electrical Measurements
- Power Burn-in
- Electrical Measurements
- Parameter Drift Values
- High and low temperature El. Measurements
- Check for lot failure
- Seal Effectiveness (Fine and Gross Leak)
- External Visual Inspection
- Solderability

The screening has been performed in accordance with the standard flow from ESCC Generic Specification No. 9000



FM Qualification



Qualification is on-going in accordance with the standard flow from ESCC Generic Specification No. 9000

Operating Life Test is performed in the following conditions:

2000h @ +125°C

CONCLUSION

- A mixed-signal ASIC for High Power Commands Management has been presented
- The ASIC will be primarily used within platform and payload control of Thales Alenia Space Data Handling equipments with first application in Sentinel-1 mission.
- The channel structure with 3 pass transistors connected in cascade allows having a robust component against failure on a single pass transistor, and using the device in wired-OR connection.
- The results of radiation test confirms adequacy of the ASIC to be used in most of space missions (Earth GEO and LEO, Mars, etc..).
- The ASIC is actually under screening and qualification phase.

THANK YOU
FOR YOUR ATTENTION!

www.caenaurelia.com

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