STARX32: A Complete On-Chip X-Ray Spectroscopy Readout System with Imaging Capability

Presented by P. Bastia on behalf of the STARX32 team

ThalesAlenia Space
A Thales / Finmeccanica Company

Politecnico di Milano

University of Pavia

Template reference : 100181670S-EN

THALES

ORIGIN OF THE PROJECT

In the last decade the Detector technology became mature for realization of large 2D X-ray detector array in GaAs, CdZnTe and similar materials

To use these arrays in a space instrument a Read Out Integrated Circuit is mandatory, this ROIC should be low-power, low-noise, hi-speed, highly integrated … and in general subjected to all limitation of space environment.

No device with these characteristics existed around 2002 when ESA started a dedicated technological program "Large Format Detector Readout"

A Industry-University team formed in Italy to search a solution to this technological challenge

TEAM ORGANIZATION

OVERALL PROJECT MANAGEMENT

ThalesAlenia Space

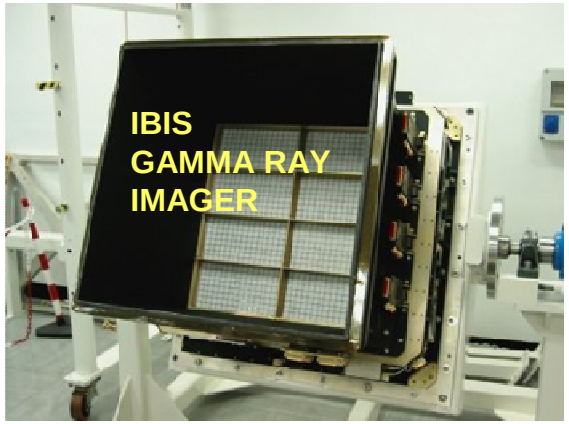
FRONT-END SECTION DESIGN

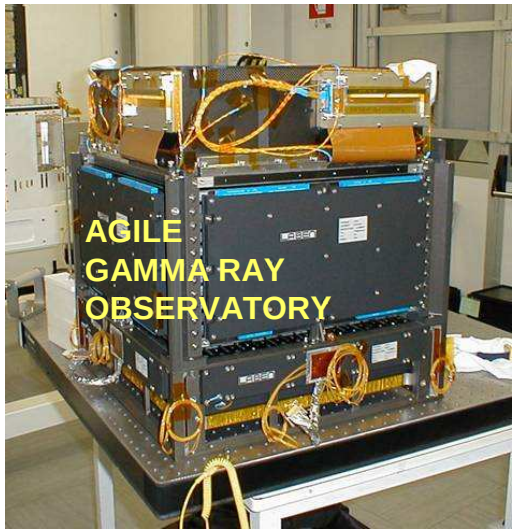
ADC & READOUT LOGIC DESIGN

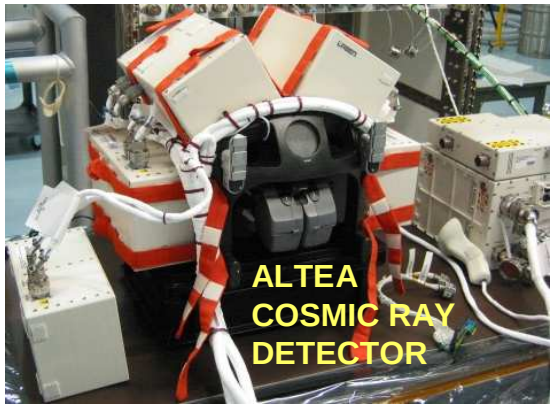
TEST EQUIPMENT DESIGN & MFG

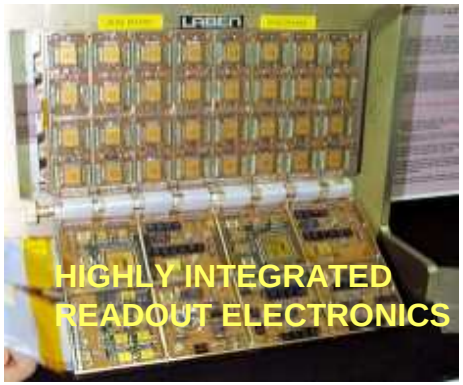
ThalesAlenia Space

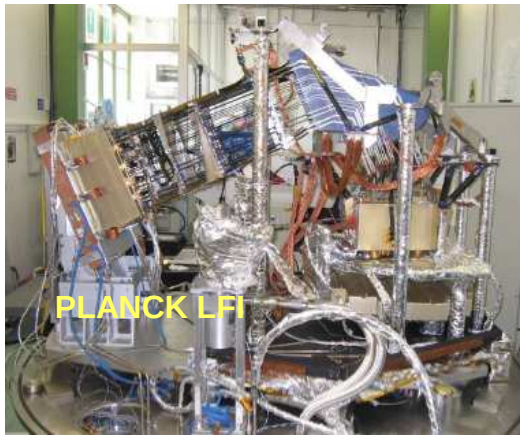
More than 30 year experience in development of space instruments for x-rays, gamma-rays, cosmic-rays, and scientific payload in general.











THALES

UNIVERSITY TEAMS

Politecnico di Milano, Department of Electronics Engineering and Information Science

- particular skills in designing ultra low noise front end for X-ray detectors (more than 100 papers on the subject)

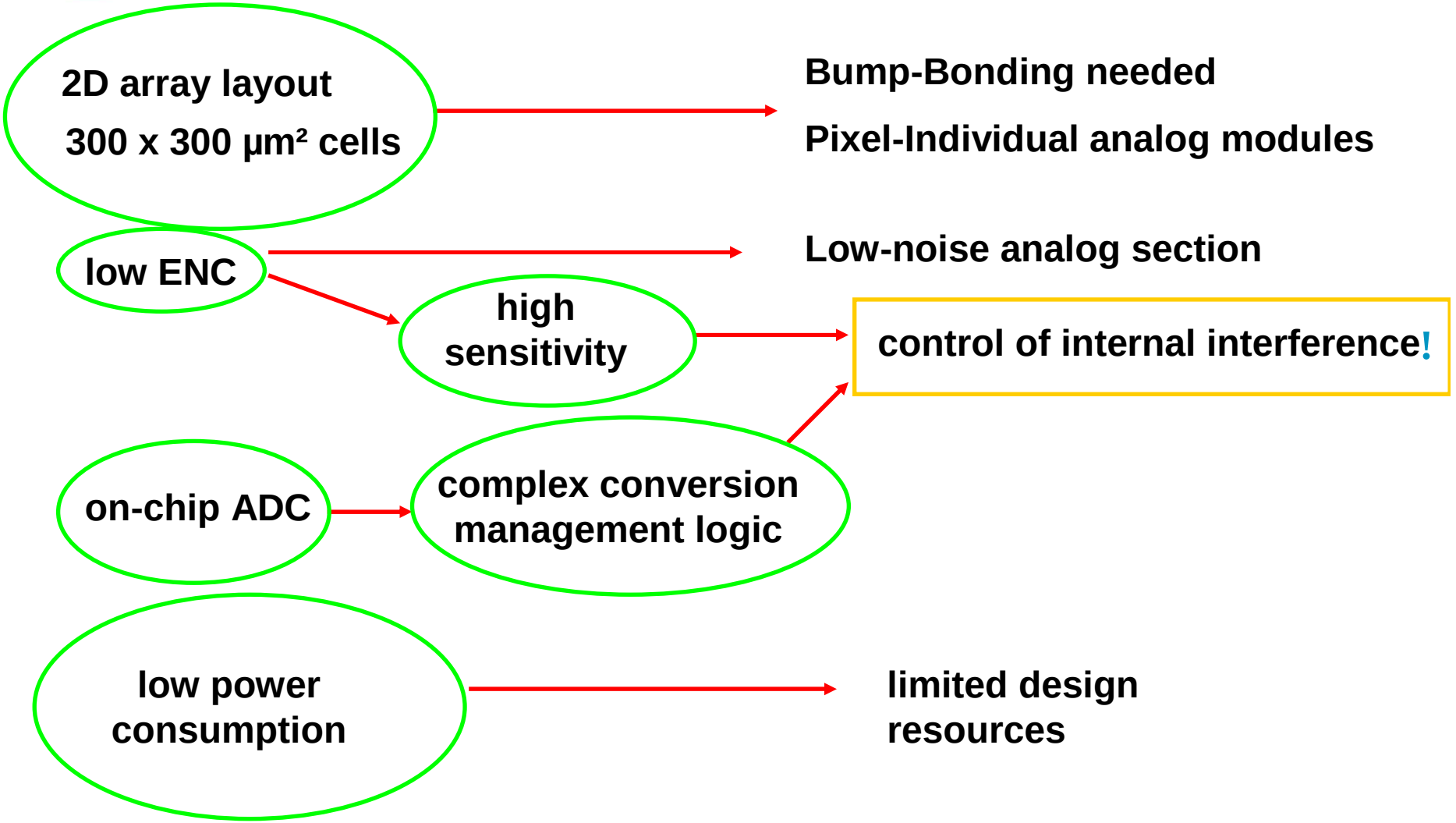
University of Pavia, Integrated Microsystem Laboratory

- member EUROPRACTICE
- large experience in mixed-signal ASIC development

REQUIREMENTS REVIEW

A SET OF CHALLENGING REQUIREMENTS

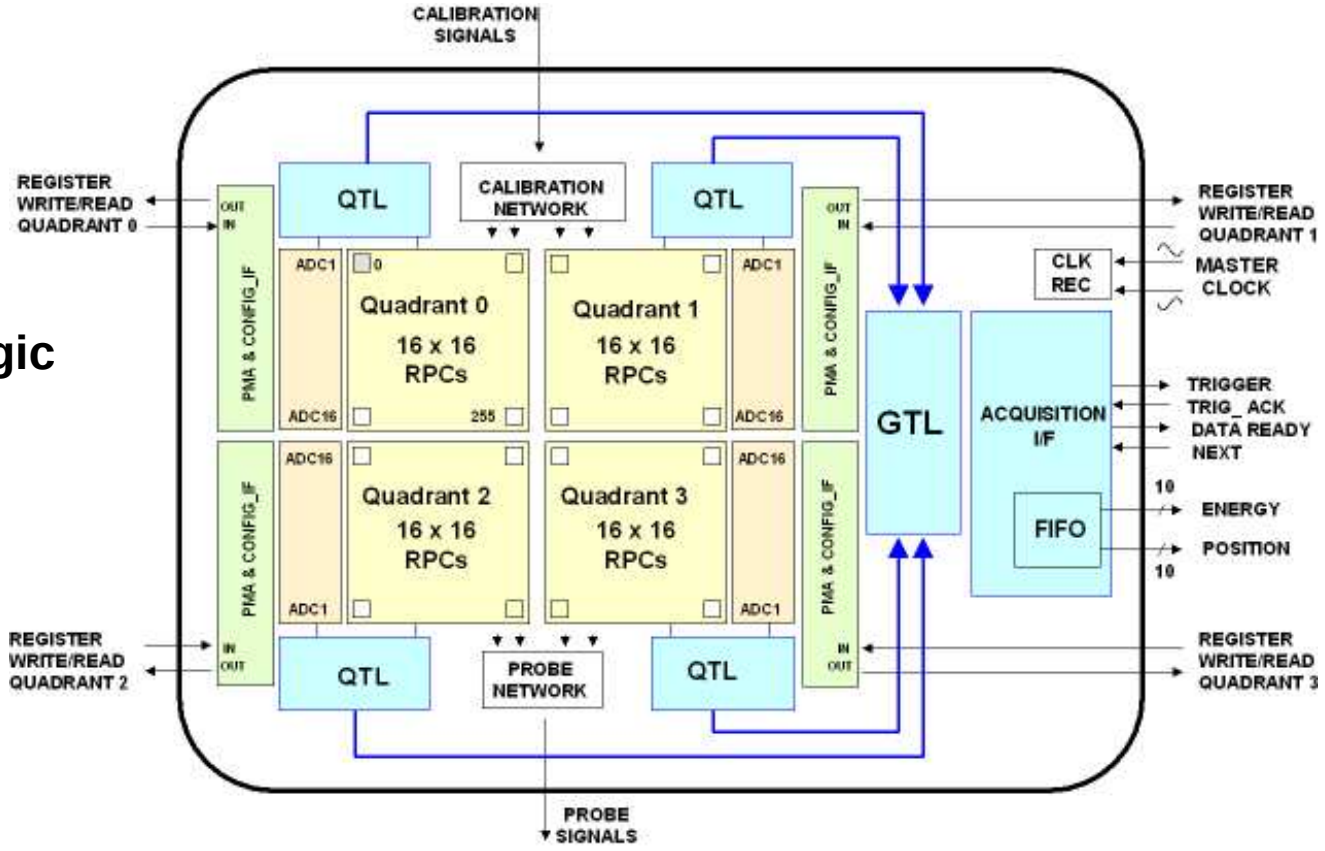
Parameter	Value	Remarks
Number of channels	32 x 32	1024:1 mux-ing required
Layout	Square array of channels (300µm pitch)	bump-bonding required between detector and ASIC
Input charge range	120 – 12000 electrons	0.5 – 50 keV in GaAs
ENC	< 30 electrons r.m.s.	with Cdet < 400fF and Idet < 2 pA detector connected
Shaping peak time	1-10µs selectable	
ADC	on-chip ≥ 9 bit resolution	system-on-a-chip including all readout logic and ADC
Event rate	> 10 kcps/channel	~10^6 cps total rate capability
Power consumption	≈ 500 µW/channel	



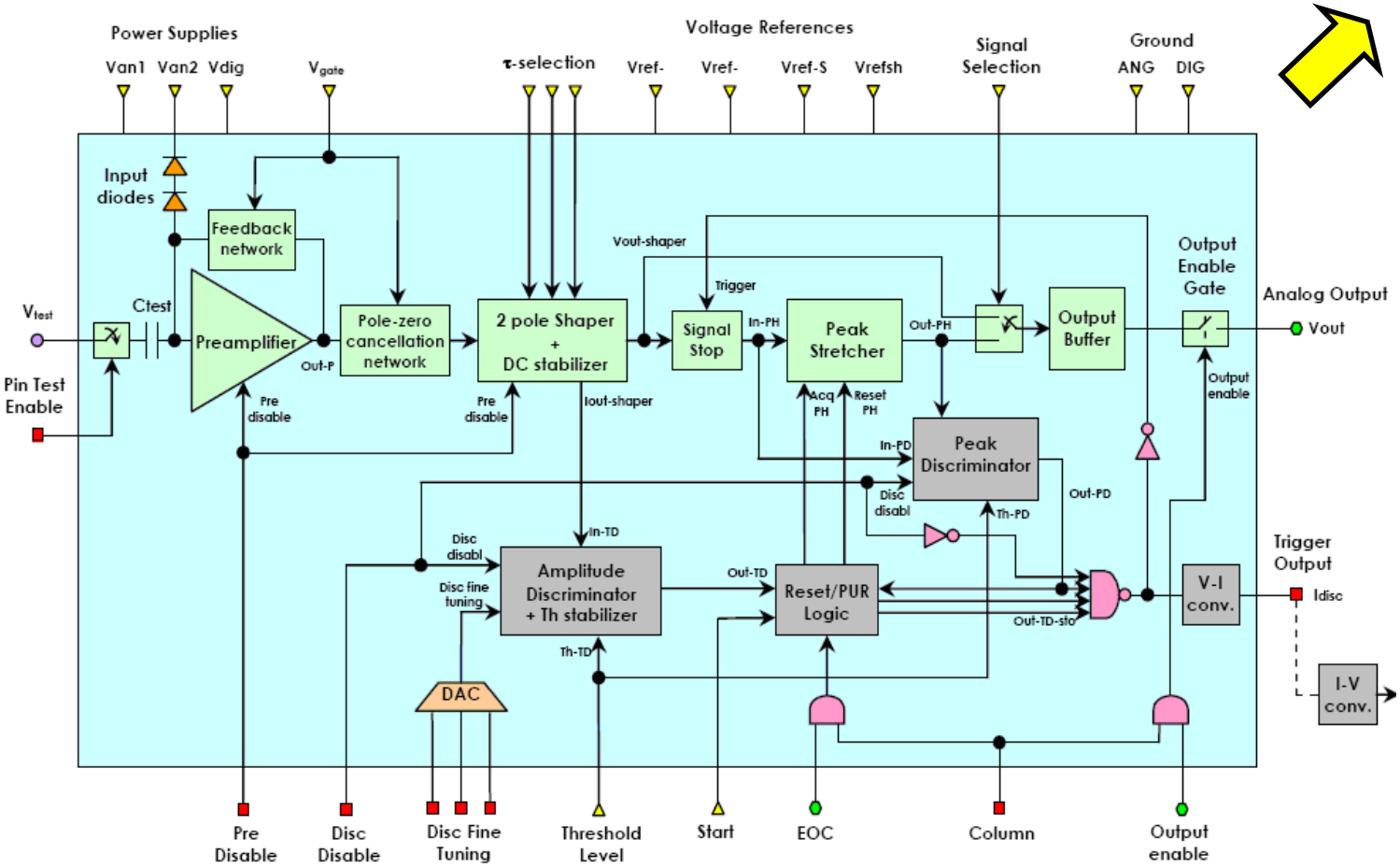
ARCHITECTURAL DESIGN

OVERALL BLOCK DIAGRAM

- Four quadrant
- 256RPCs/quadrant
- 16 ADCs/quadrant
- Quadrant Trigger Logic
- Global Trigger Logic
- Acquisition I/F
- Configuration I/F
- Calibration Network
- Probe Network



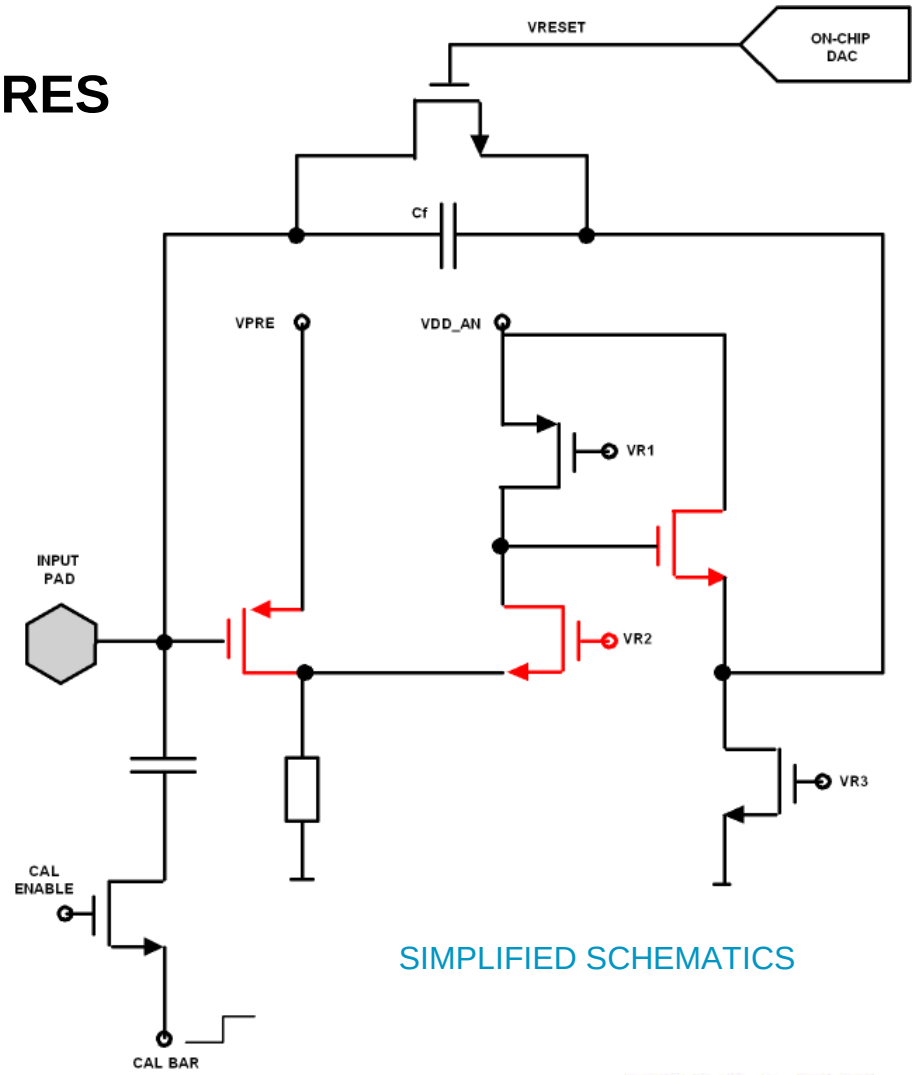
READOUT PIXEL CELL



CHARGE PREAMPLIFIER FEATURES

- Dedicated preamplifiers supply line
- P-MOS input stage & cascode
- Continuous reset with subthreshold transistor
- On/Off features
- Calibration input

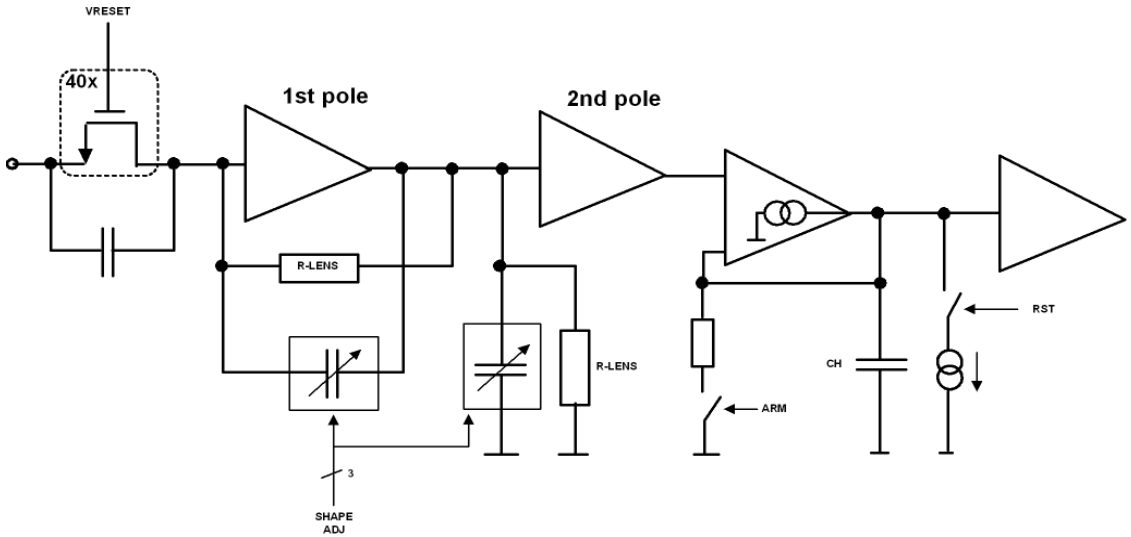
- 100µm x 100µm occupation
- 120 µW power dissipation



SIMPLIFIED SCHEMATICS

PZC, SHAPER AND STRETCHER

- **Reset circuit non linearity compensation**
- **Current-mode shaper**
- **DC cancellation**
- **Adjustable peak time 1,2,4,5,6,7,9,10 µs**
- **Equalization gain w.r.t. shaping time**



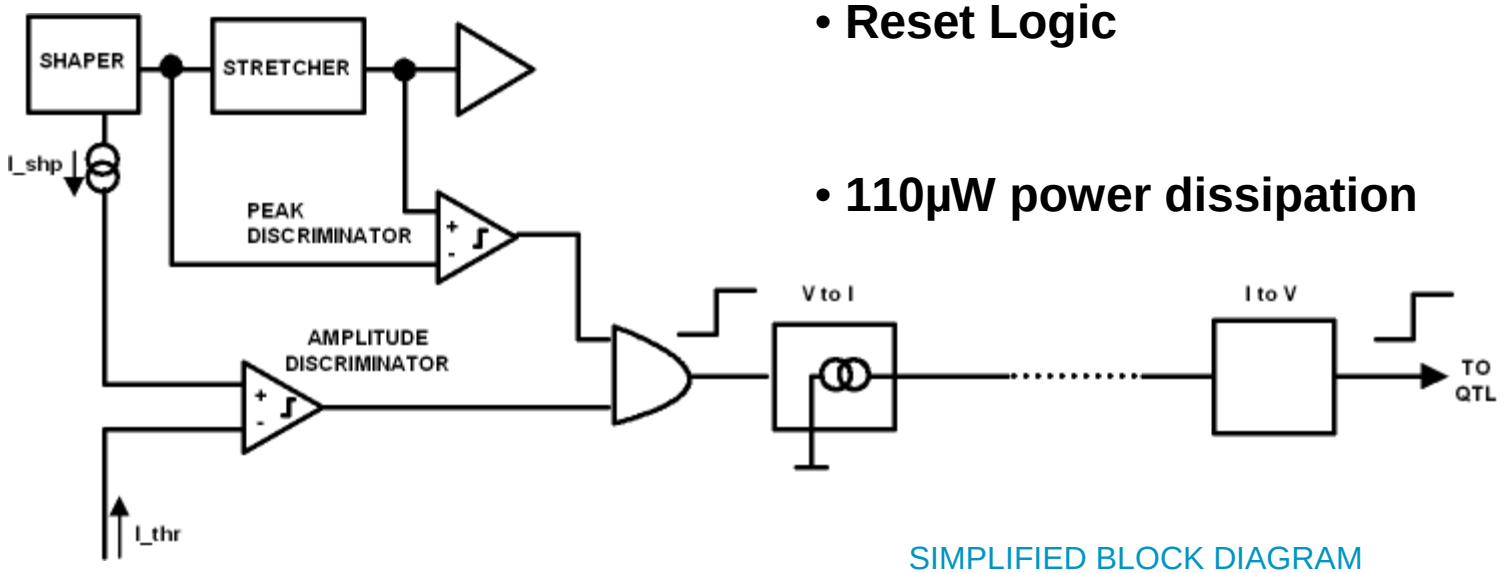
SIMPLIFIED BLOCK DIAGRAM

- **250 µW power dissipation**

RPC TRIGGER CIRCUITRY

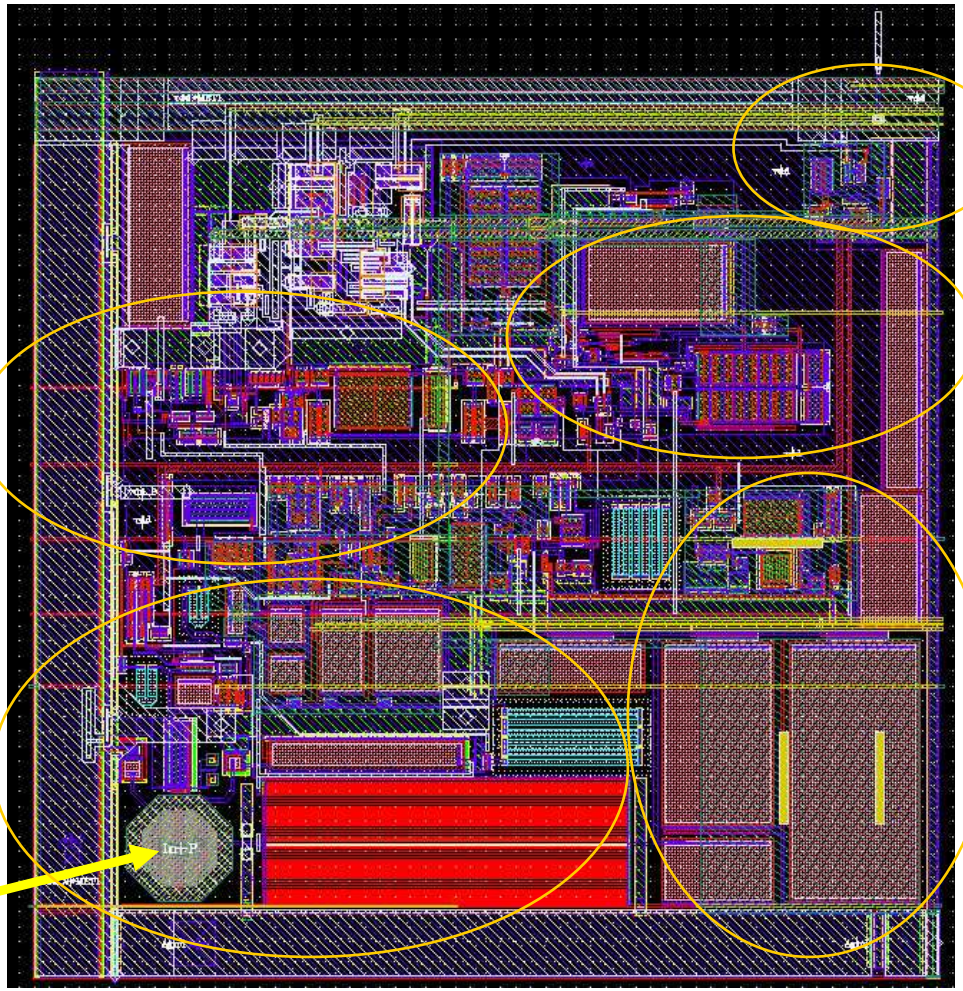
- **Amplitude discriminator**
- **Fine THR tuning**
- **Peak discriminator**
- **Current-mode trigger to periphery**
- **Reset Logic**

- **110µW power dissipation**



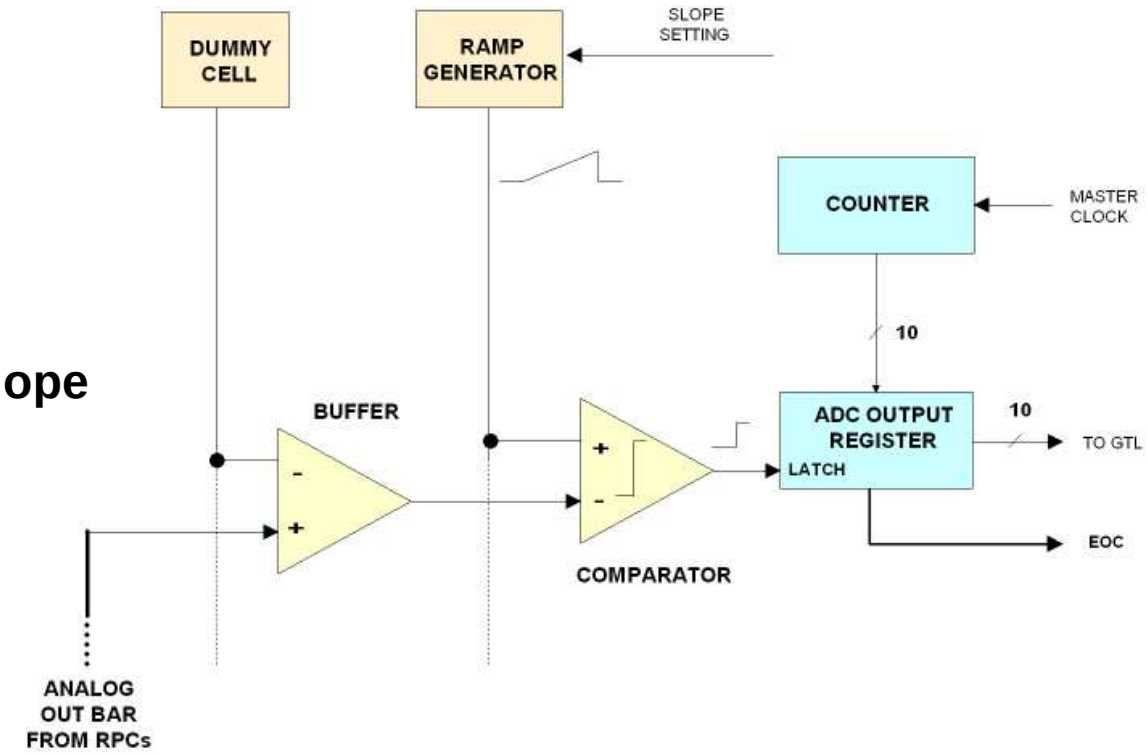
SIMPLIFIED BLOCK DIAGRAM

RPC LAYOUT



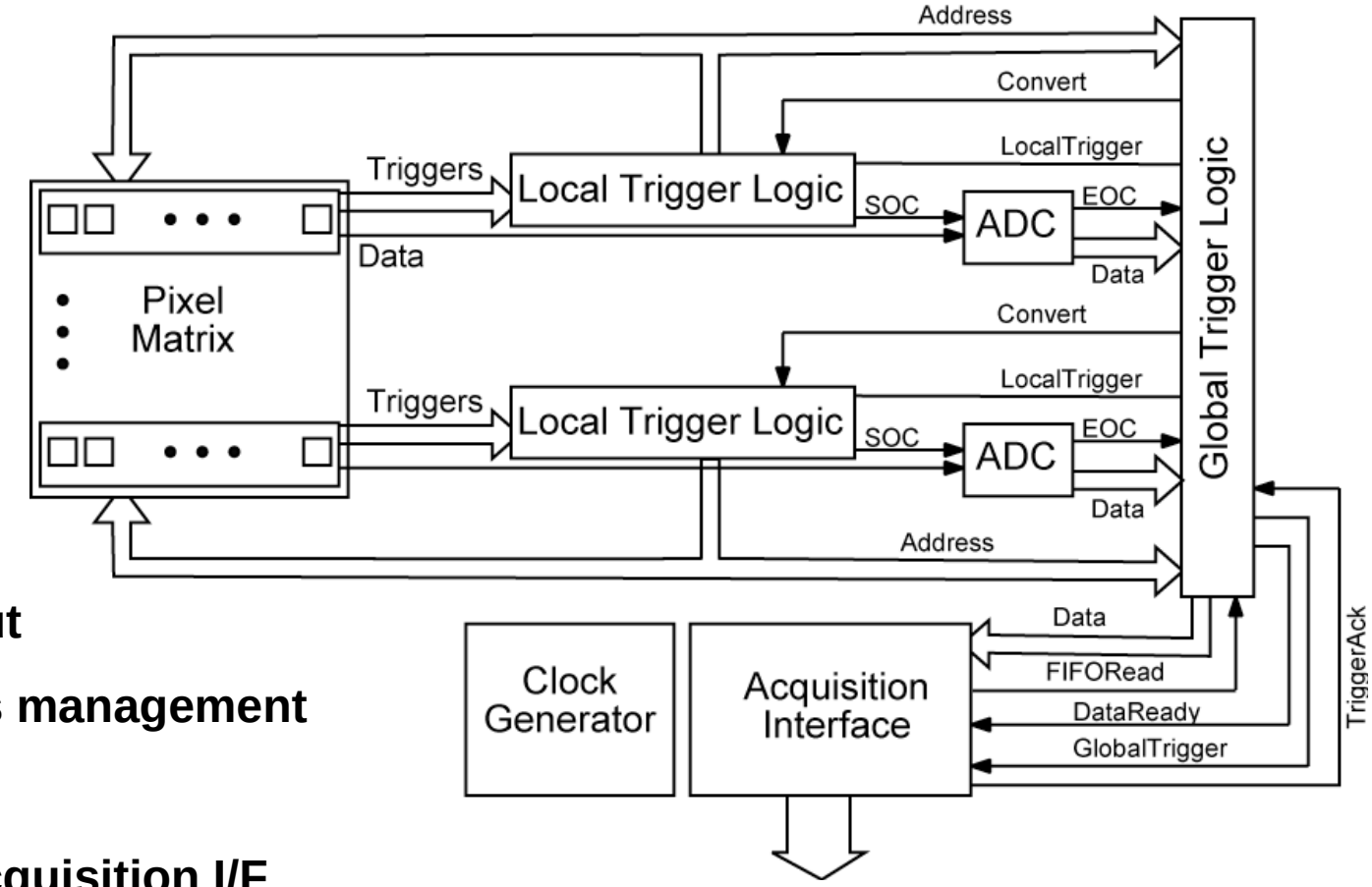
ADCs

- 16 RPC/ADC
- Wilkinson, 10 bit
- sine/differential clock
- on-chip adjustable ramp slope



- < 2 mW power dissipation

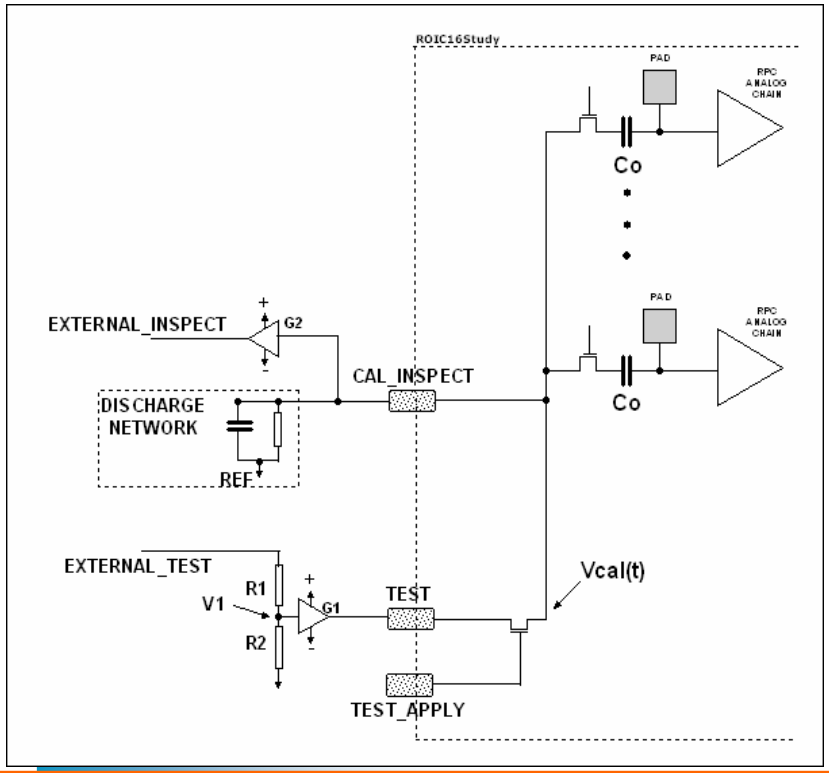
QTU/GTU



- **Sparse Readout**
- **Multiple events management**
- **Global FIFO**
- **Fast parallel acquisition I/F**

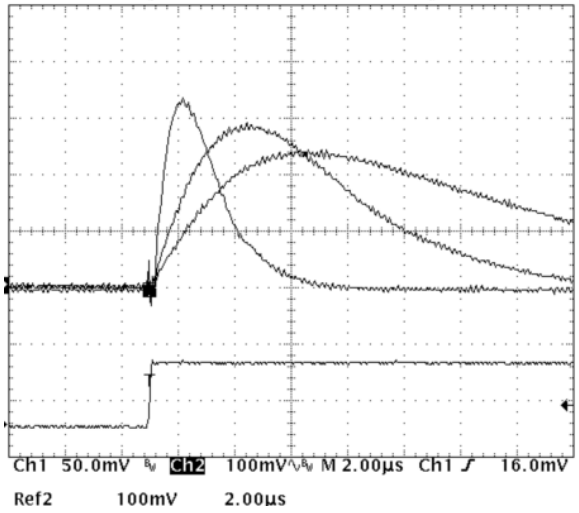
CALIBRATION NETWORK

- three independent nets
- internal or external pulsing



PROBE NETWORK

- interesting nodes inspection



ON BOARD DACS

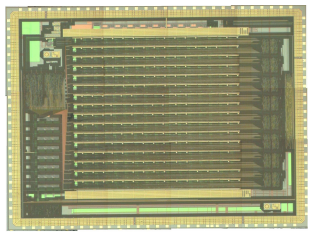
- Threshold and preamplifier reset adjustable by telecommand

PROTOTYPES

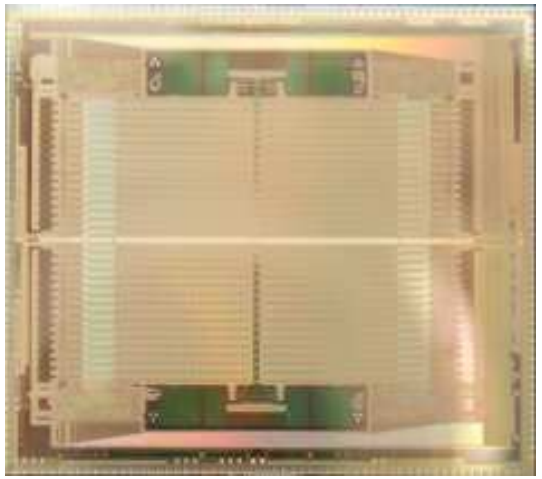
Selected Technology: AMS C35 0.35µm CMOS

Four foundry runs:

- 16x16 study prototype #1 (MPW)
- 16x16 study prototype #2 (MPW)



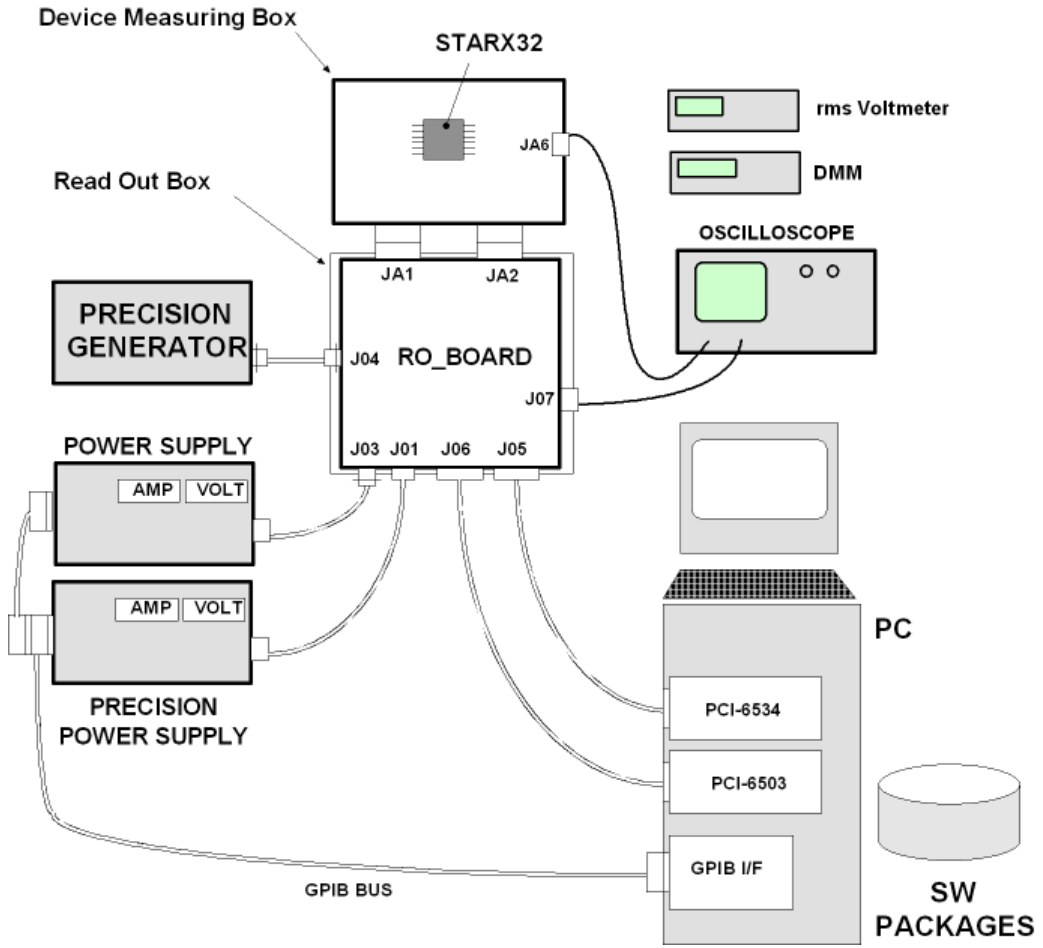
- 32x32 prototype (STARX32 v.1) (dedicated run)
- 32x32 “final” (STARX32 v.2) (dedicated run)



TESTING

DEDICATED TEST SYSTEM

- Device mounted on carrier hybrid
- Shielded box with local biasing
- ReadOut box (FPGA)
- Fast digital I/O card for data
- Standard I/O card for configuration
- PC-controlled
- Control and Analysis SW

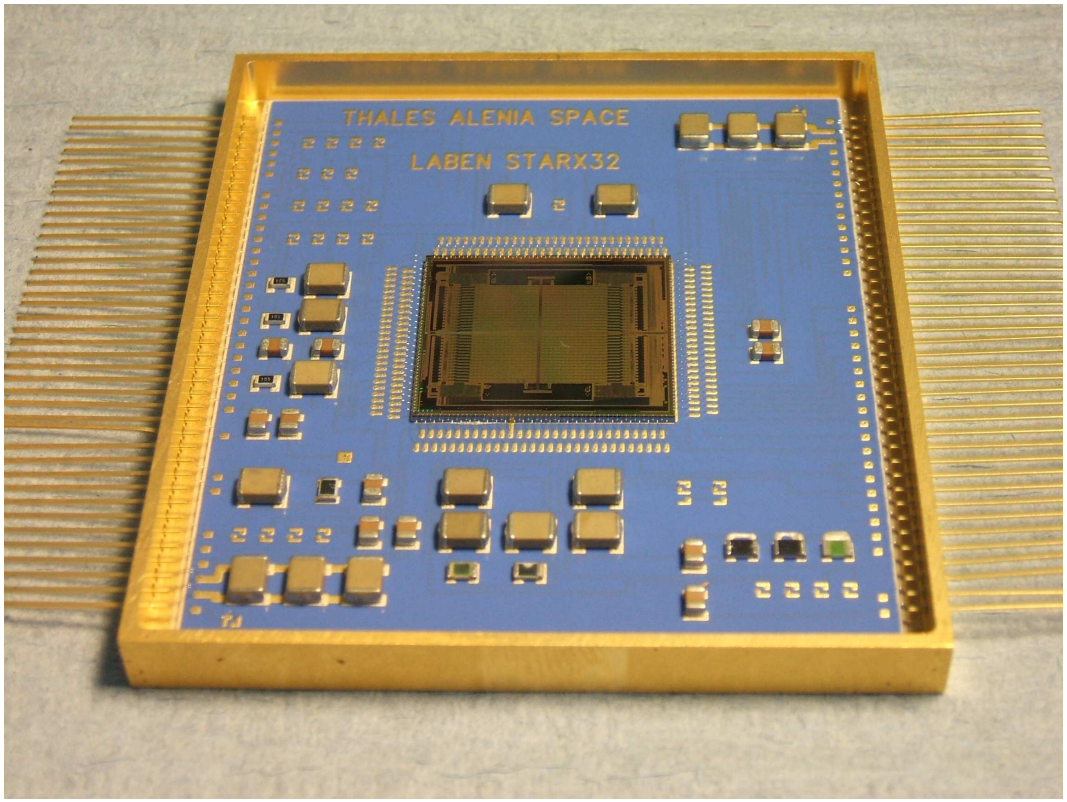


CARRIER HYBRID

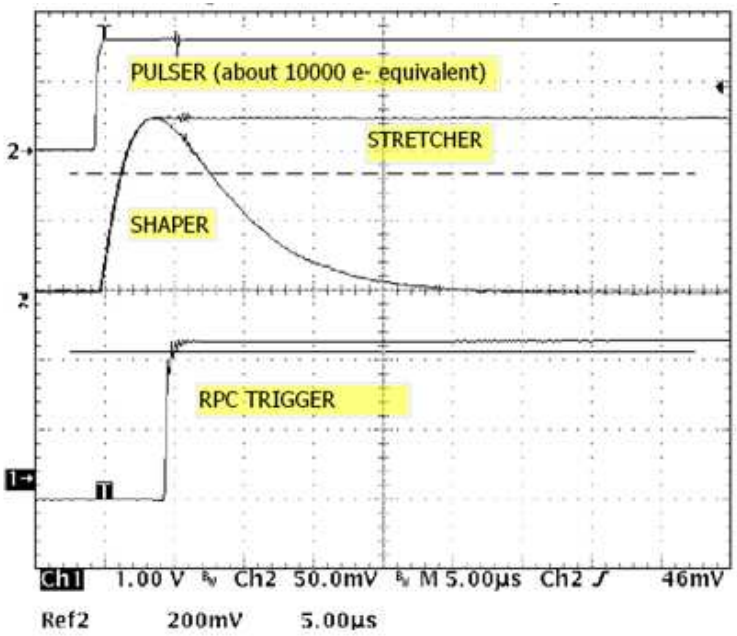
provides a light-tight and protected environment for the device under test

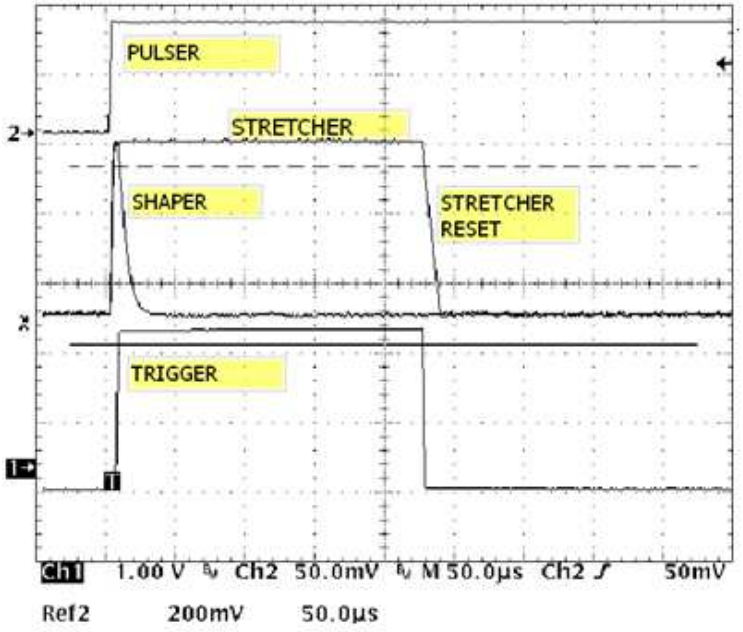
allows easy mating/demating with the test equipment

Hosts some ancillary passives for filtering/bias purposes

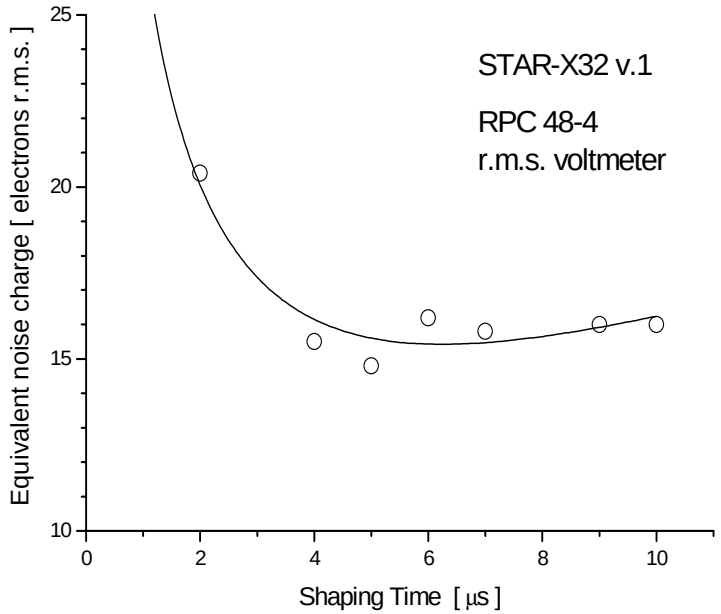


TYPICAL RPC SIGNALS





ENC MEASUREMENTS (room-T, no-detector)

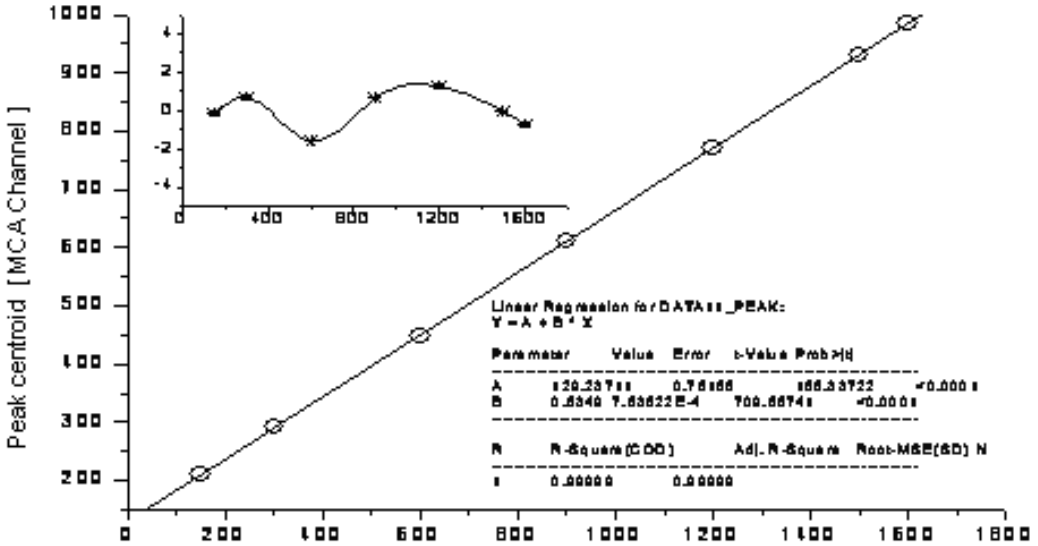


Minimum ENC:

~ 16 electrons rms at 6µs peak time

END-TO-END LINEARITY

(include on-board ADC)



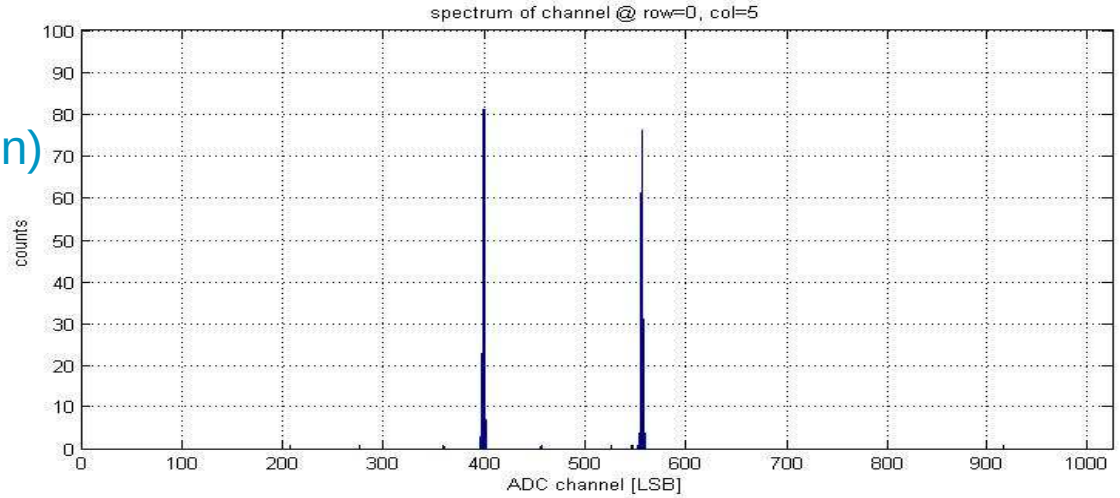
Stimulus via calibration network

Range ~1000 to 10000 electrons

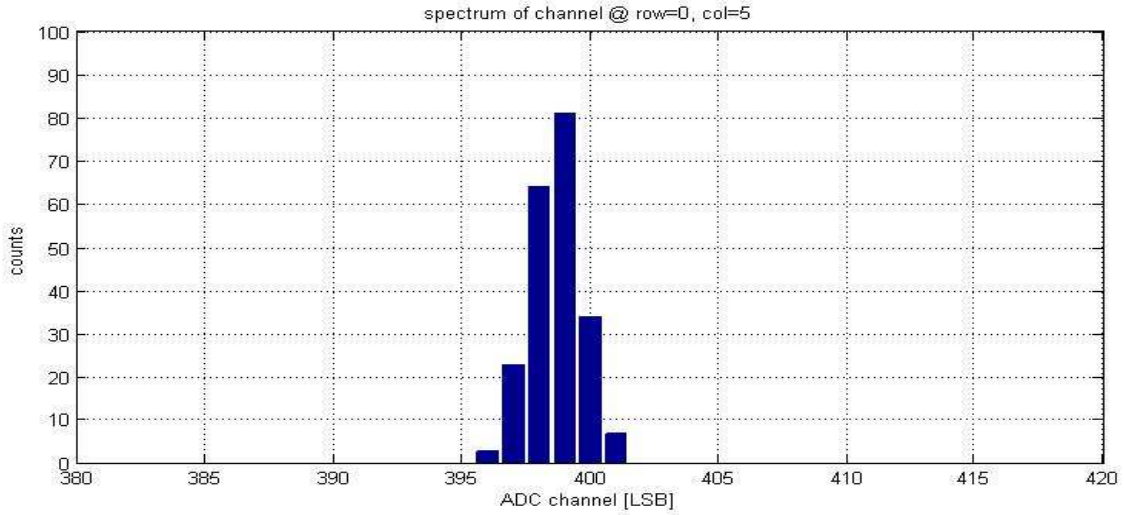
INL < 0.25 %

END-TO-END spectrum

(stimulus by on board calibration)

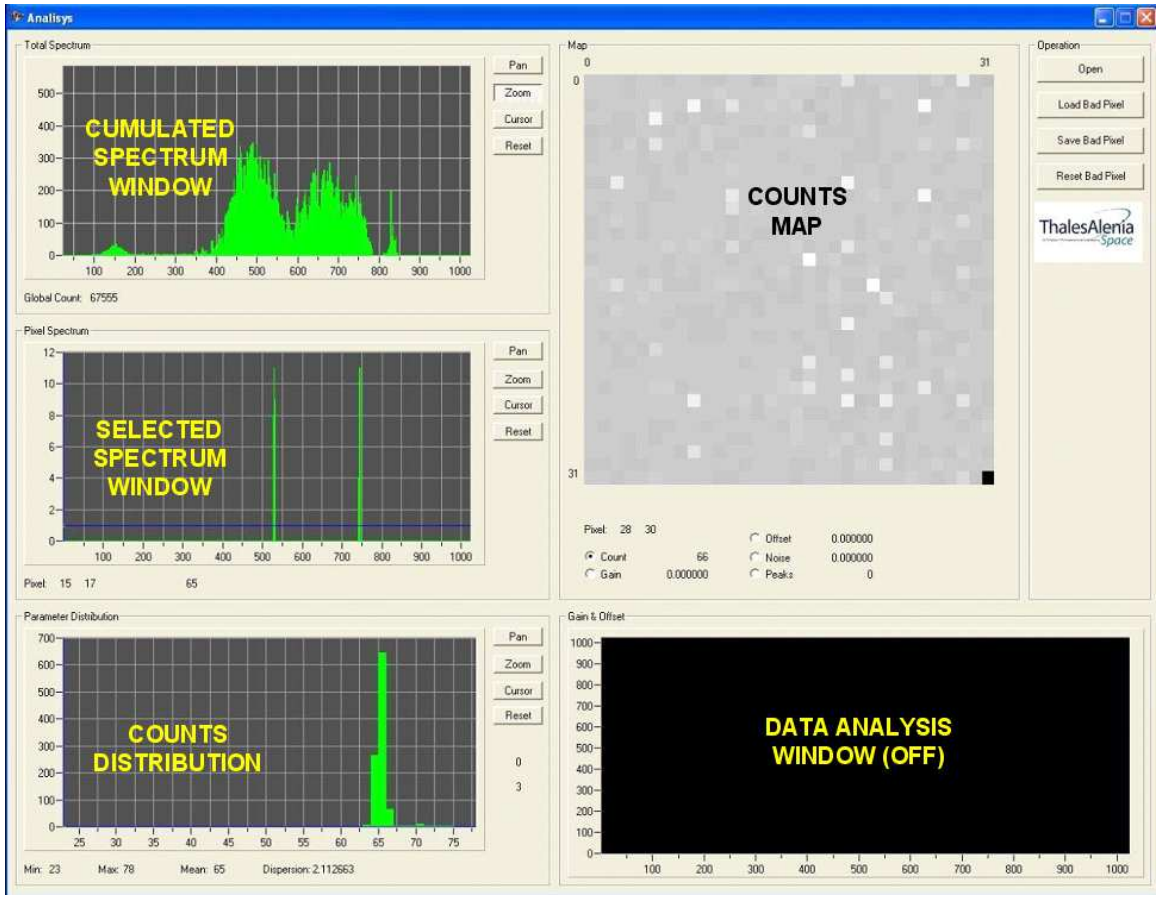


Line details

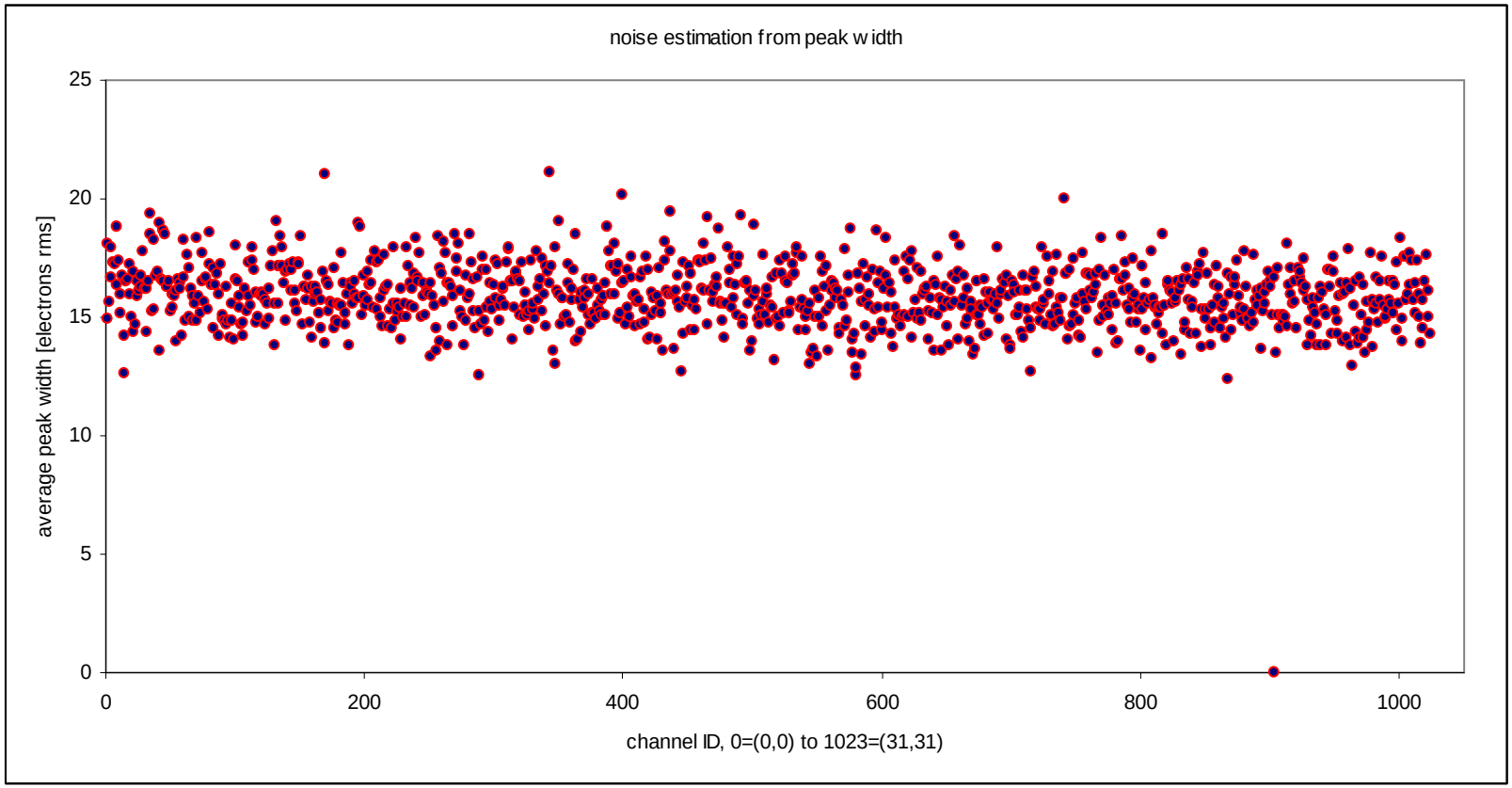


QUICK-LOOK ANALYSIS

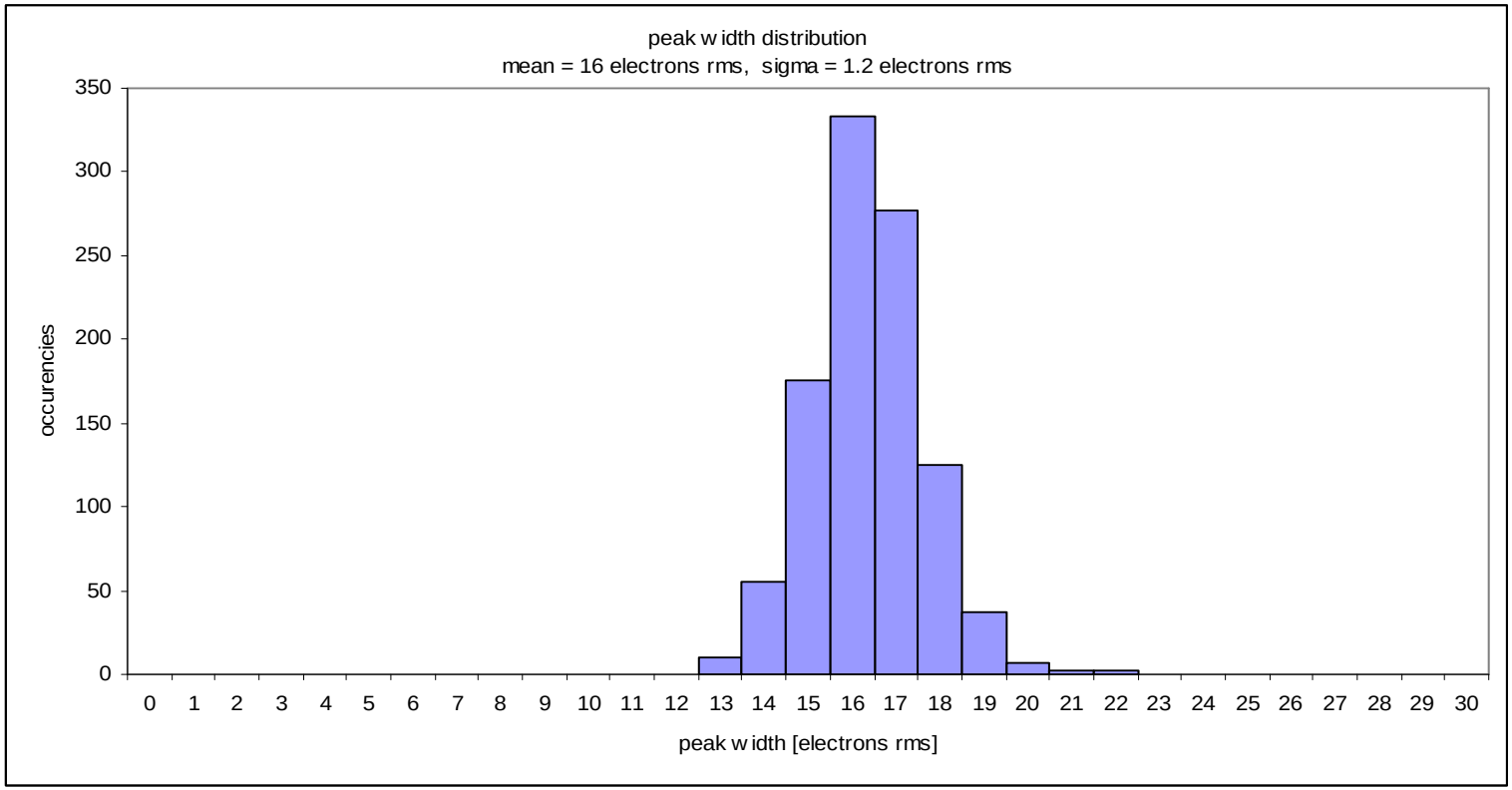
- **all RPCs found working**
- **thin individual spectra lines**
- **gain/offset spread …**



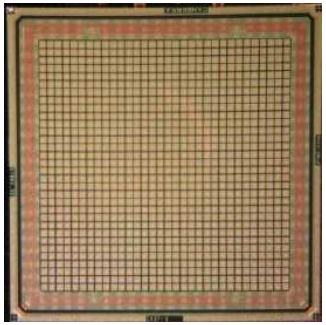
PEAK WIDTH



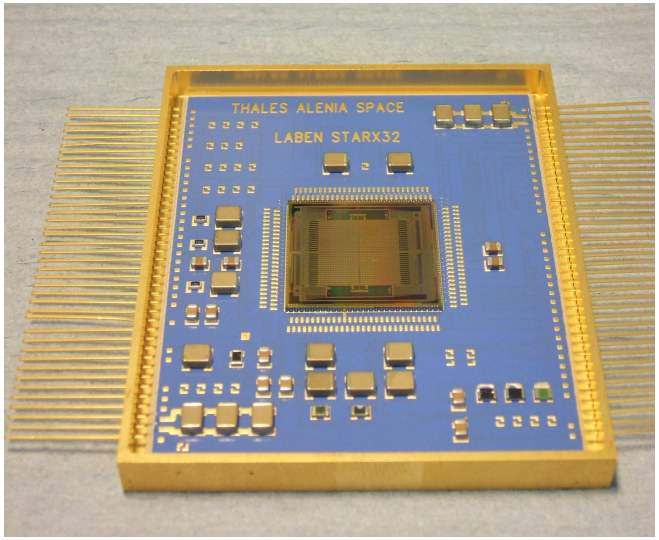
PEAK WIDTH



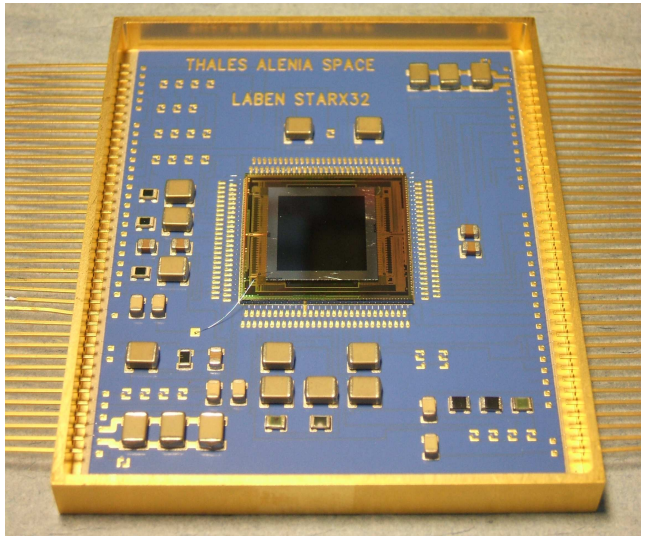
TEST WITH DETECTOR



- Custom-made 32x32 pixels p-n Silicon detector procured for test in realistic condition
- Bump-Bonded on some samples of STARX-32, one sample put on carrier hybrid



without detector



with detector

FINDINGS

- **bump-bonding process functionally OK (just 1 out of 1024 missing bond found)**
- **process possibly critical w.r.t. pixels performance:**

reverse currents much higher than expected

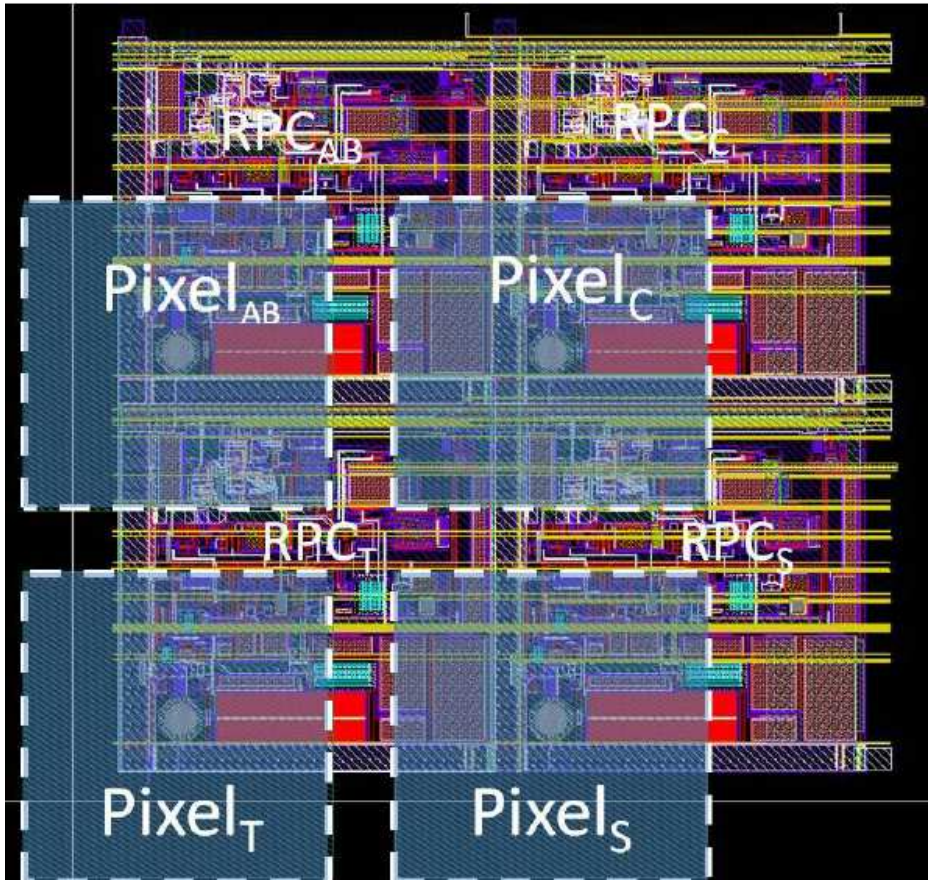
up to > 50 nA/cm^2,

is this due to bump-bonding process ?

FINDINGS

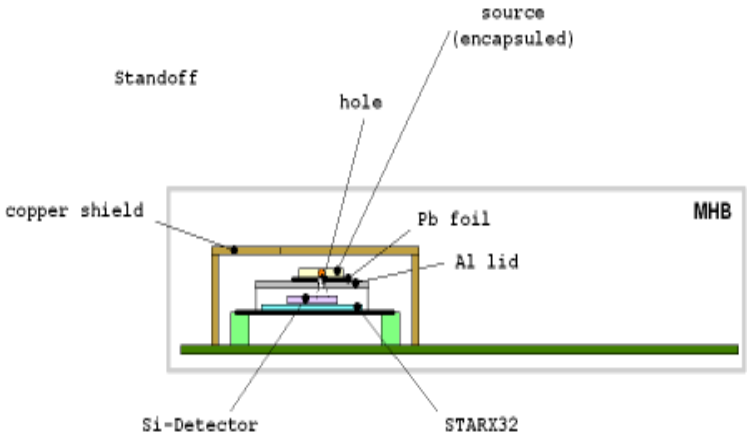
- **inter-pixel cross-talk**

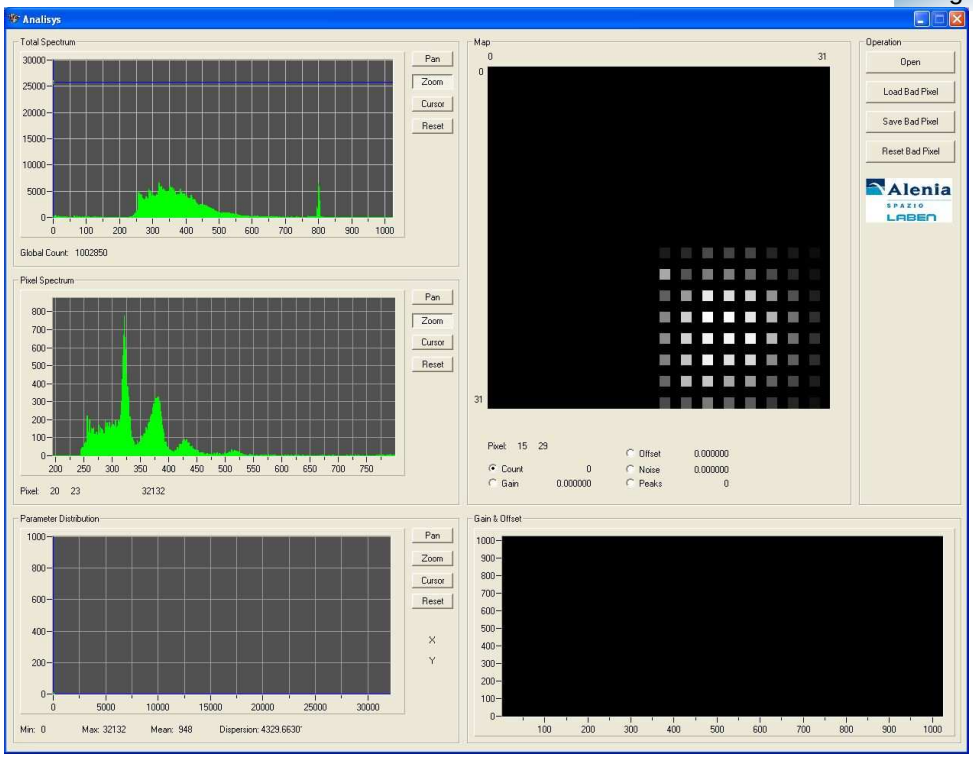
some signals from an active RPC can AC-couple to nearby RPCs via detector

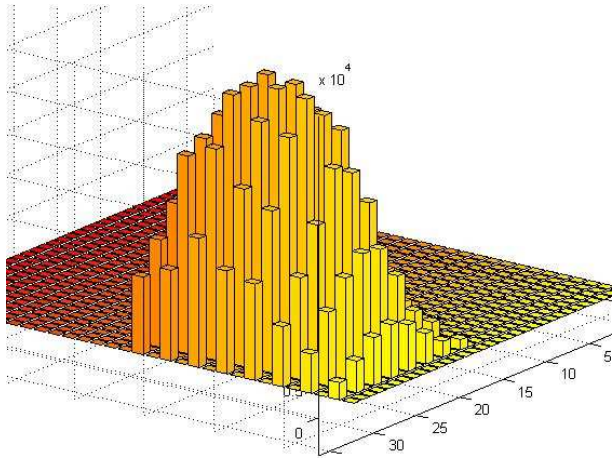


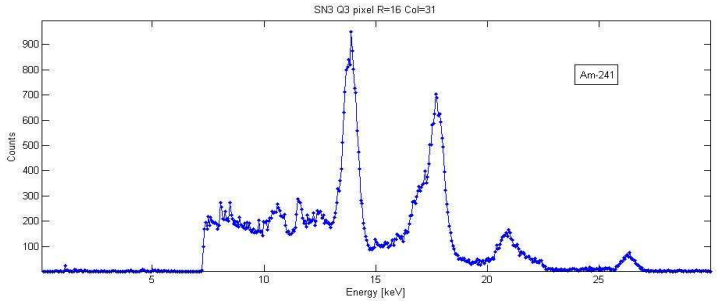
Additional shielding (metal) above disturbing nodes implemented in final prototype.

effectiveness to be tested soon









TID TEST

In view of possible application on spaceborne instruments

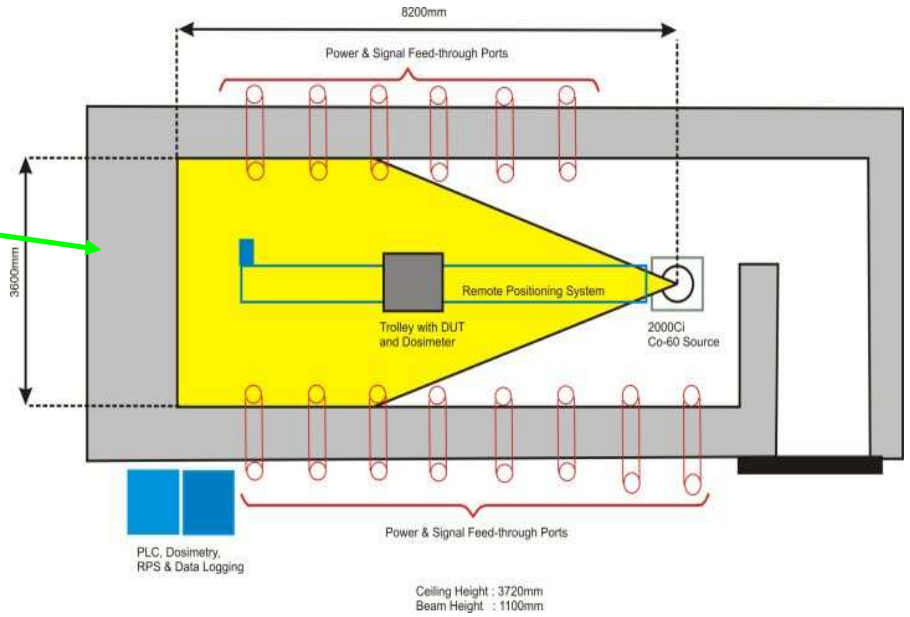
…

Radiation Test have been performed at
ESTEC Co-60 Facility

Total Dose = up to 59 krad

Intermediate steps every 8 krad

Total Irradiation Time = 3 Days

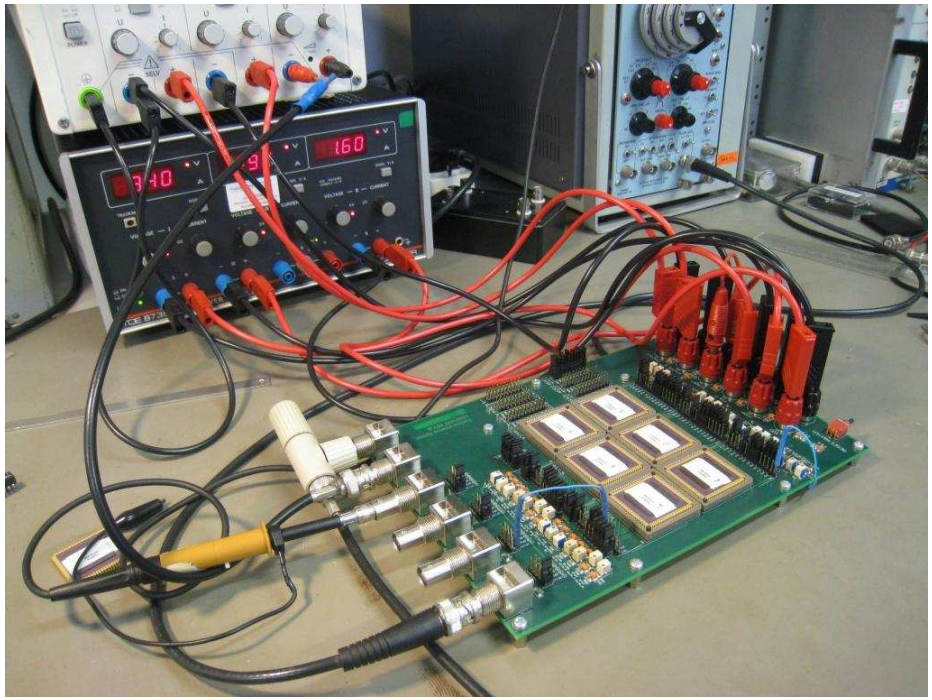


TEST BOARD

A dedicated Test Board has been designed and manufactured.

The board has been used both for biasing during irradiation and for measurements.

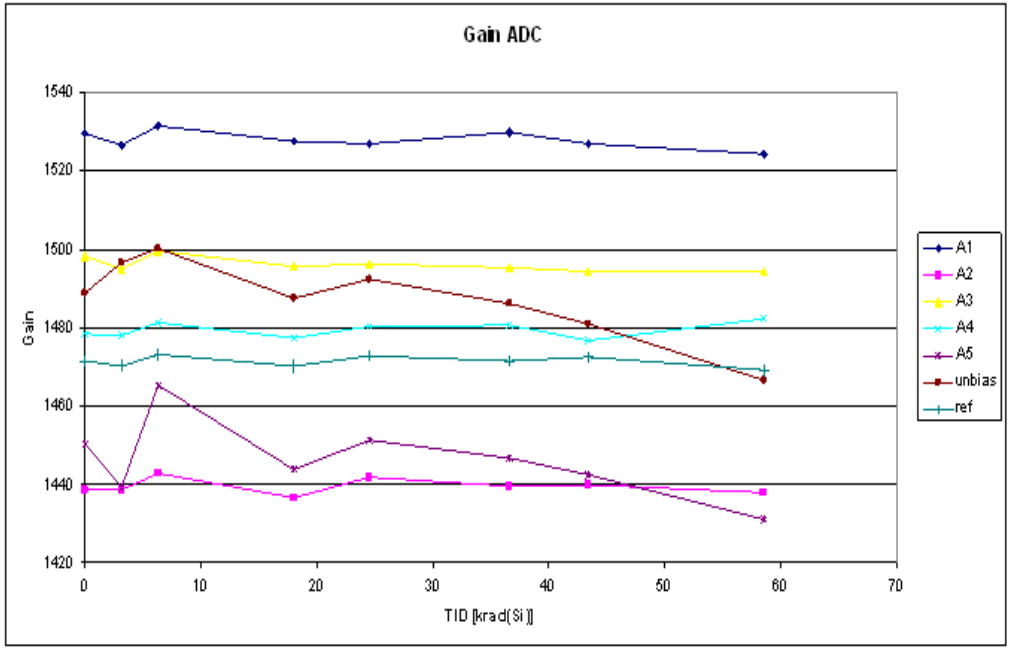
The board is able to host up to 6 chips together and to stimulate and test up to 5 chip at the same time.



TID TEST RESULTS

- most of RPC parameters do not show significant variations up to 60 krad
- one RPC bias show constant negative trend ~1% at 60 krad (tolerable)

- only marginal drifts on ADCs
- two samples needed re-adjust of the rest voltage above 40 krad



The test results suggest that the AMS 0.35 µm CMOS technology used in the LFDR prototype is rad tolerant at least to 60 krad.

SUMMARY & CONCLUSIONS

SUMMARY & CONCLUSIONS

- We presented the latest development for the STARX32 project
- The overall performances are very good, e.g. ENC and power dissipation, moreover radiation tolerance (TID) has been proven up to > 50 krad
- As expected for such a challenging design task we are improving the design through successive prototypes and extended test campaigns
- Control of internal interference is of paramount importance and the major reason for the need of multiple prototypes
- Bump-Bonded detector requires carefull “top” shielding of the front end cell
- The 4-th prototype (STARX32 v.2) has been manufactured in May 2010 and is presently under test, results so far are encouraging, we are looking forward to bump-bond a sample with a detector for complete end-to-end test