The NemeriX G3 chipset: a radiation hardened front end for GNSS receivers aimed at space application

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Outline

• G3 Chipset Requirements
• Microelectronic Technology Selection
• Architecture of the 2 ASICs
• First Space Application using the ASICs
Nemerix’s G3 chipset

- The chipset consists of 2 ASICs:
  - NJ1007R: RF receiver front end
  - NJ1017R: AD DA interface

- Requirements
  - Multifrequency receiver GPS/Galileo/GLONASS
  - High RF performances more important than integration level or cost effectiveness
  - Radiation tolerant design for space borne applications

- Technology selection criteria:
  - Shall have good RF performance.
  - Shall be available also in small quantities.
  - Shall be either radiation tolerant or allow radiation tolerant circuits to be designed.
The G3 chipset

• Main Reason for a Chipset:
  – Prevent interference between AD converters and sensitive RF circuitry.

• NJ1007R:
  – Pure analog RF ASIC
  – S35, SiGe process

• NJ1017R:
  – Massive digital ASIC.
  – C35 process would be fine. S35 was selected in order to produce NJ1007 and NJ1017 on the same wafer. Main advantages:
    • Reduced costs
    • Easier qualification process
System configuration

NemerIX's RF front end

RF downconverter ASIC

GNSS (an. I/Q)

f2

data

clock

AD & DA ASIC

OSC

GNSS

f6

data

clock

Base Band Processor

NemerIX's RF front end

BB processor
G3 chipset common parameters

<table>
<thead>
<tr>
<th>Power Supply in active mode</th>
<th>Supply Voltage</th>
<th>AVDD</th>
<th>2.2 ... 3.6</th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>DVDD</td>
<td>1.6 to AVDD+0.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| NJ1007R supply current @ 3.6V | AVDD | 13.8 | mA |
| DVDD | 110 (*) | μA |

| NJ1017R Supply current @ 3.6V | AVDD | 2 | mA |
| DVDD | <1 (*) | mA |

<table>
<thead>
<tr>
<th>Radiation Tolerance</th>
<th>Total Dose</th>
<th>120</th>
<th>krad(Si)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heavy Ions</td>
<td>84</td>
<td>MeV/mg/cm²</td>
<td></td>
</tr>
</tbody>
</table>

(*) Excluding load
Package solution: 36-CBGA

CERAMIC
KYOCERA A473

SOLDER LID
42 ALLOY / Solder KC-003

NJ10xxR

5x0.8=4
0.8
0.4

0.85±0.1
0.72±0.07

0.45 ±0.05

0.3

5.6±0.05
4.7±0.08

6±0.15
Process selection

• General:
  – Thin layers (wells, diffusions, oxides). Thick N-well may improve latch-up.
  – Retrograded well or buried layer and epi improve latch-up resistance.
  – SOI has no mechanism to generate a latch-up.
  – Deep trenches improve latch-up somewhat.

• BJT:
  – Thin base and emitter more robust than thick base (less $\beta$ degradation).
  – Poly emitter (thinner) more robust than a diffused one.

• MOS:
  – Thin gate oxide better than thick oxide (less charge trapping, less device degradation).
  – Shorter channel transistors (stronger) give improved SEE resistance.

  **Process: AMS S35, 0.35µm SiGe HBT**
Microsection of the S35 process (NJ1007R)

- Polymide
- Passivation
- Thick Metal 4
- Oxide + Vias
- Metal 3
- Oxide + Vias
- Metal 2
- Oxide + Vias
- Metal 1
- Oxide + Vias
- Substrate
NJ1007R – RF receiver front end

- Integrated LNA
- External filters
- I/Q outputs
- Die size: 1.2 x 1.0 mm
- Signal Bandwidth < 24MHz
**NJ1007R characteristics**

<table>
<thead>
<tr>
<th>Component</th>
<th>Parameter</th>
<th>LNA</th>
<th>RF Down-converter</th>
<th>IF Strip</th>
<th>RF-VCO IF-VCO</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Gain</td>
<td>19 dB</td>
<td></td>
<td>70 dB</td>
<td>800 MHz/V</td>
</tr>
<tr>
<td></td>
<td>Noise figure</td>
<td>1.6 dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>IP3</td>
<td>-10 dBm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 dB compression point</td>
<td>-22 dBm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Conversion gain</td>
<td>25 dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SSB noise figure</td>
<td>9 dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>IP3</td>
<td>-10 dBm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 dB compression point</td>
<td>-18 dBm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>AGC amplifier gain</td>
<td>1.6 dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Gain control range</td>
<td>70 dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RF SSB phase noise</td>
<td>-83 dBc/Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SSB noise figure</td>
<td>-57 dBc/Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>IF VCO sensitivity</td>
<td>250 MHz/V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RF SSB phase noise</td>
<td>-50 dBc/Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RF SSB phase noise</td>
<td>-85 dBc/Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>IIF SSB noise</td>
<td>-50 dBc/Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>PLL spurs</td>
<td>&lt;35 dBc</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
NJ1017R – AD DA Interface ASIC

- 2 ADCs (for I/Q outputs of NJ1007R)
  - 3-bit
  - Sampling frequency < 50MHz
- 8-bit DAC (for AGC)
- SPI like interface to the base band processor
- PLL (for sampling clock)
### NJ1017R characteristics

<table>
<thead>
<tr>
<th>Component</th>
<th>Specification</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-bit ADC</td>
<td>DNL</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>INL</td>
<td>0.5</td>
</tr>
<tr>
<td>Max sampling freq.</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Input Voltage range</td>
<td></td>
<td>700 mVpp</td>
</tr>
<tr>
<td>SFDR</td>
<td></td>
<td>25 dB</td>
</tr>
<tr>
<td>AGC 8-bit DAC</td>
<td>DNL</td>
<td>3 LSB</td>
</tr>
<tr>
<td></td>
<td>INL</td>
<td>3 LSB</td>
</tr>
<tr>
<td>Output Voltage range</td>
<td></td>
<td>0 ... 2.1 V</td>
</tr>
<tr>
<td>VCO, PLL</td>
<td>Frequency Range</td>
<td>25 ... 100 MHz</td>
</tr>
<tr>
<td></td>
<td>RF SSB phase noise</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1MHz</td>
<td>-90 dB</td>
</tr>
<tr>
<td></td>
<td>10kHz</td>
<td>-60 dB</td>
</tr>
<tr>
<td></td>
<td>100Hz</td>
<td>-65 dB</td>
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</tbody>
</table>
NJ1007R chip layout
NJ1007R chip on CBGA substrate
Close view of bonded NJ1007R
Overview of G3 chip set Lot Validation

• Project started in 2007

• Lot Validation based on ESCC9000 including
  – Wafer Manufacturing
  – Wafer Lot Acceptance including Total Ionizing (TID) Dose testing
  – Packaging of Evaluation Lot
  – Evaluation Test
  – Packaging of Flight Lot
  – Screening of Flight Lot
  – Lot validation of Flight Lot

• Completion expected early 2009
G3 chip set First Application

- GPS based Precise Orbit Determination (POD) Receiver for ESA-SWARM Mission

- Down-converts and digitizes the GPS L1 and L2 signals by means of Nj1007R and NJ1017R, RF- and mixed-signal ASICs

- AGGA-2 chips and a LEON processor form the heart of the digital signal processing
G3 chip set First Application
G3 chip set First Application
G3 chip set First Application

• Interfaces
  – UART (RS-422) TC/TM interface
  – MIL-STD-1553B TC/TM interface extension

• Electronic Box
  – Box Size: 322x240x104 mm³
  – Weight: < 3.5 kg including antenna
  – Power Consumption: < 10W

• Antenna
  – Patch Excited Cup Antenna with improved multipath suppression from Saab Space
Conclusions

- G3 Chipset consists of RF Front-End and AD Converter
- Chipset is Radiation Tolerant (120 krad(Si); 84 MeV/mg/cm$^2$)
- G3 ASICs are Being Qualified to ESCC9000
- First Application for SWARM Mission (under construction)

Thank you for your attention