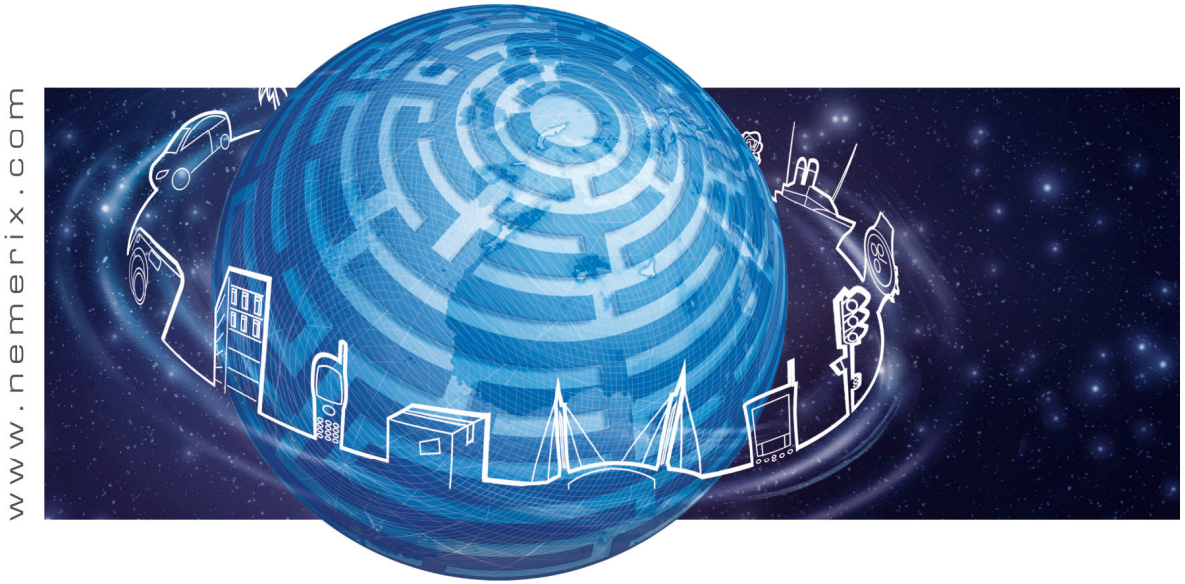
Austrian Aerospace

NEMERIX
WORLD'S LOWEST POWER GPS SOLUTIONS

The NemeriX G3 chipset : a radiation hardened front end for GNSS receivers aimed at space application



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Hannes Schwammschneider; Austrian Aerospace

Outline

- G3 Chipset Requirements
- Microelectronic Technology Selection
- Architecture of the 2 ASICs
- First Space Application using the ASICs

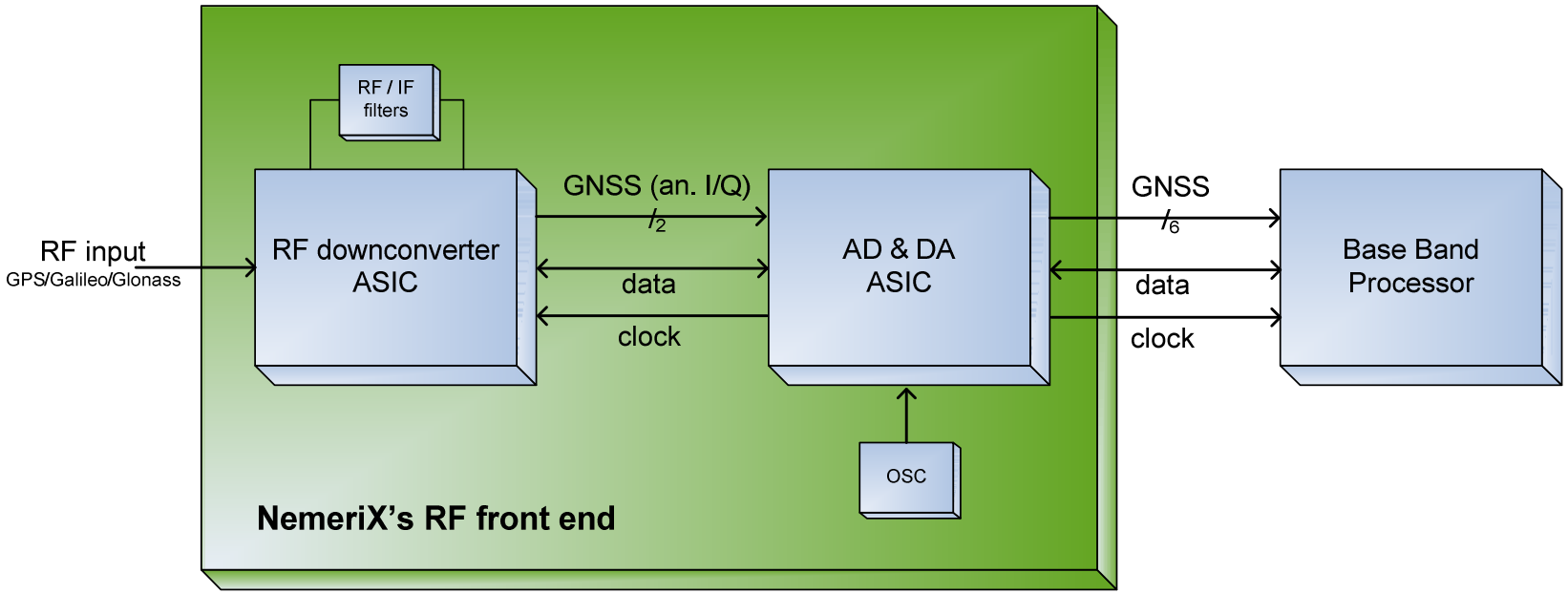
NemeriX's G3 chipset

- The chipset consists of 2 ASICs:
  - NJ1007R: RF receiver front end
  - NJ1017R: AD DA interface
- Requirements
  - Multifrequency receiver GPS/Galileo/GLONASS
  - High RF performances more important than integration level or cost effectiveness
  - Radiation tolerant design for space borne applications
- Technology selection criteria:
  - Shall have good RF performance.
  - Shall be available also in small quantities.
  - Shall be either radiation tolerant or allow radiation tolerant circuits to be designed.

The G3 chipset

- Main Reason for a Chipset:
  - Prevent interference between AD converters and sensitive RF circuitry.
- NJ1007R:
  - Pure analog RF ASIC
  - S35, SiGe process
- NJ1017R:
  - Massive digital ASIC.
  - C35 process would be fine. S35 was selected in order to produce NJ1007 and NJ1017 on the same wafer. Main advantages:
    - Reduced costs
    - Easier qualification process

System configuration



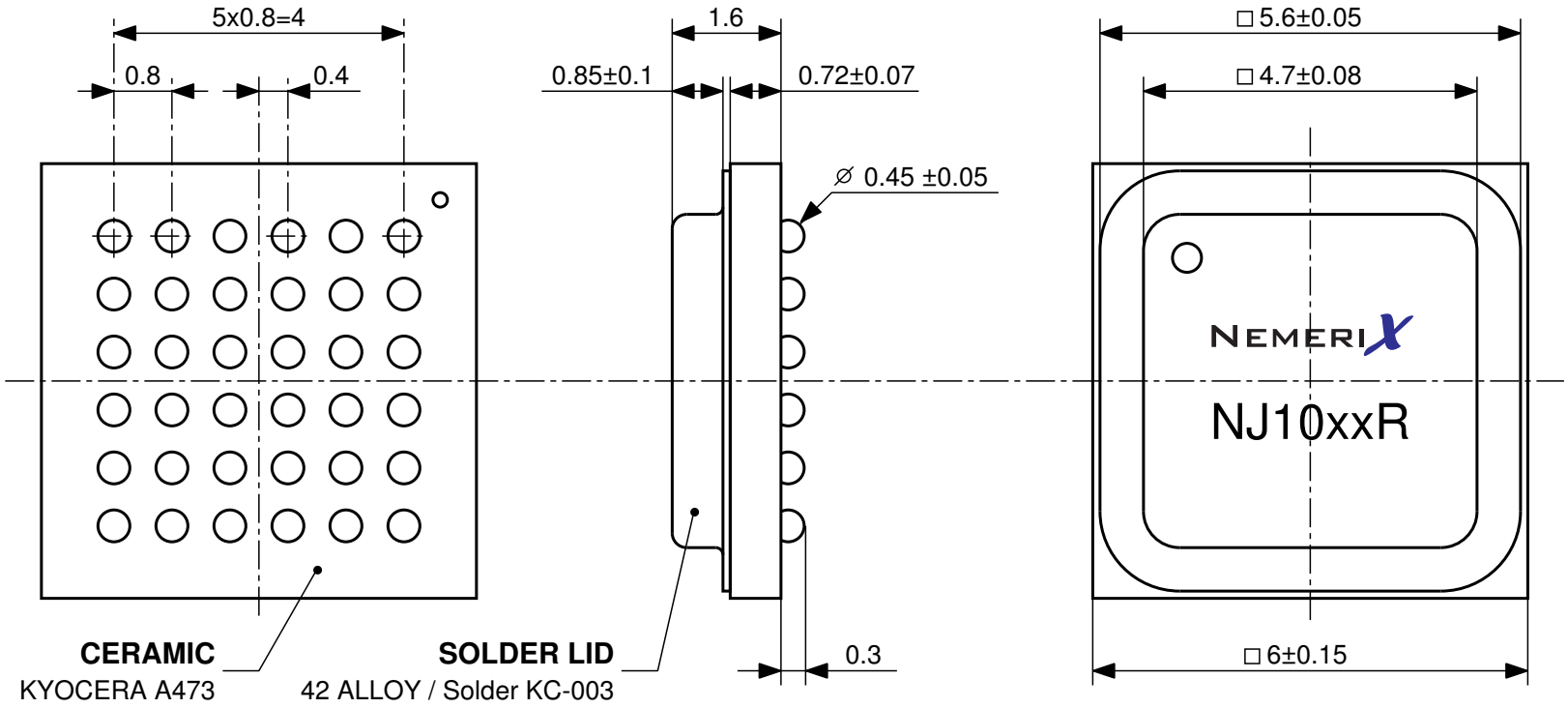
NemeriX's RF front end BB processor

G3 chipset common parameters

Power Supply in active mode	**Supply voltage**	AVDD	2.2 … 3.6	V
		DVDD	1.6 to AVDD+0.2	V
	NJ1007R supply current @ 3.6V	AVDD	13.8	mA
		DVDD	110 (*)	µA
	NJ1017R Supply current @ 3.6V	AVDD	2	mA
		DVDD	<1 (*)	mA
Radiation Tolerance	**Total Dose**		120	krad(Si)
	Heavy Ions		84	MeV/mg/cm^2

(*) Excluding load

Package solution: 36-CBGA

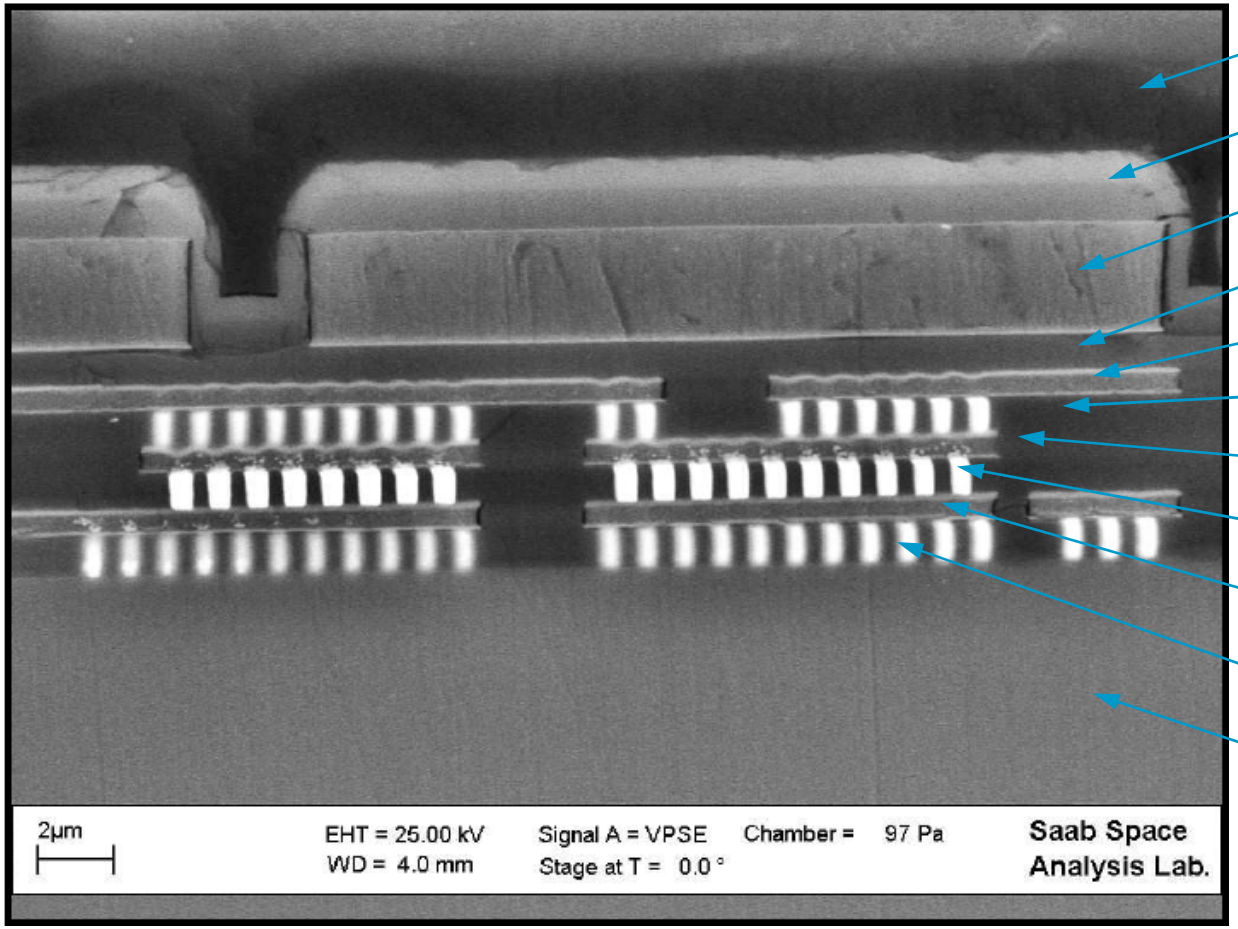


Process selection

- General:
  - Thin layers (wells, diffusions, oxides). Thick N-well may improve latch-up.
  - Retrograded well or buried layer and epi improve latch-up resistance.
  - SOI has no mechanism to generate a latch-up.
  - Deep trenches improve latch-up somewhat.
- BJT:
  - Thin base and emitter more robust than thick base (less β degradation).
  - Poly emitter (thinner) more robust than a diffused one.
- MOS:
  - Thin gate oxide better than thick oxide (less charge trapping, less device degradation).
  - Shorter channel transistors (stronger) give improved SEE resistance.

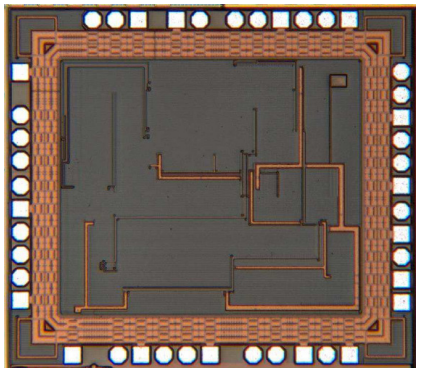
Process: AMS S35, 0.35µm SiGe HBT

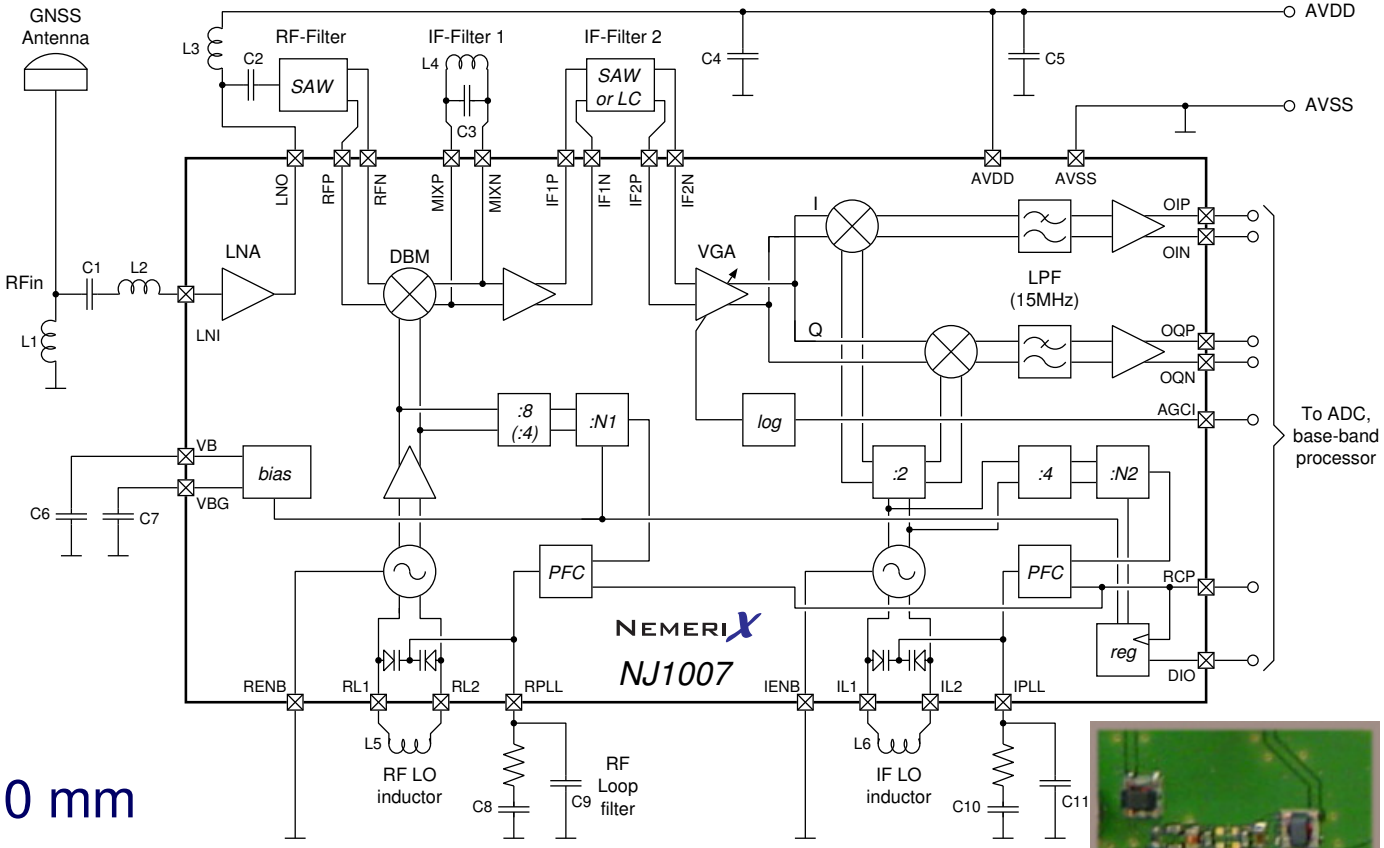
Microsection of the S35 process (NJ1007R)



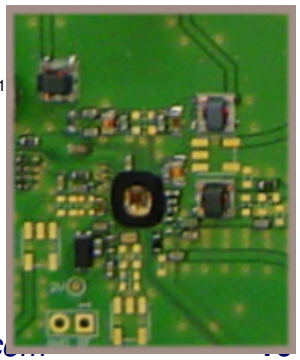
Polymide
Passivation
Thick Metal 4
Oxide + Vias
Metal 3
Oxide + Vias
Metal 2
Oxide + Vias
Metal 1
Oxide + Vias
Substrate

NJ1007R – RF receiver front end





- Integrated LNA
- External filters
- I/Q outputs
- Die size: 1.2 x 1.0 mm
- Signal Bandwidth < 24MHz

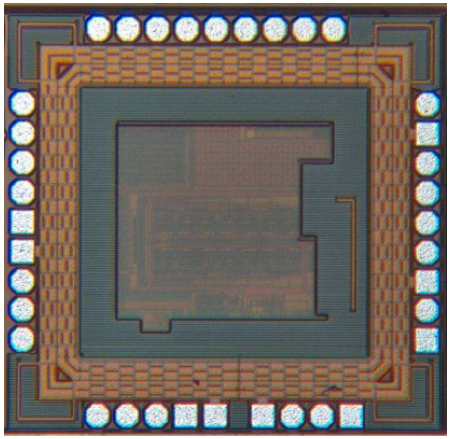


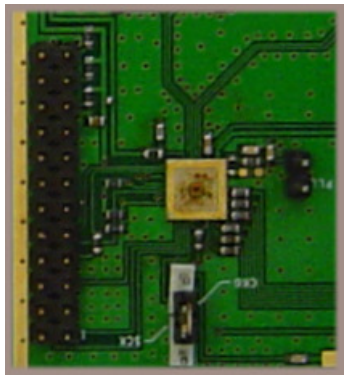
NJ1007R characteristics

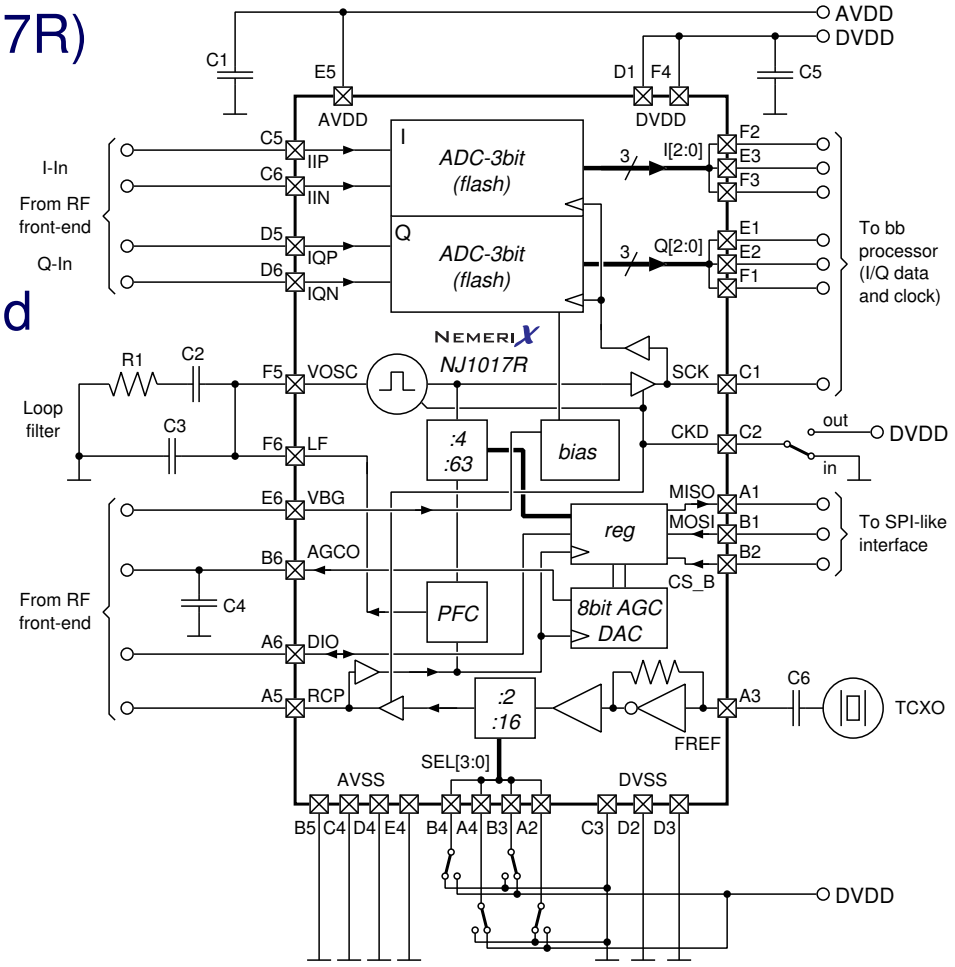
NJ1007 (G3RF)	**LNA**	Gain		19	dB
		Noise figure		1.6	dB
		IP3		-10	dBm
		1 dB compression point		-22	dBm
	RF Down-converter	Conversion gain		25	dB
		SSB noise figure		9	dB
		IP3		-10	dBm
		1dB compression point		-18	dBm
	IF Strip	AGC amplifier gain		70	dB
		Gain control range		60	dB
	RF-VCO IF-VCO	RF VCO sensitivity		800	MHz/V
		RF SSB phase noise	100kHz 1kHz 10Hz	-83 -57 -50	dBc/Hz dBc/Hz dBc/Hz
		IF VCO sensitivity		250	MHz/V
		IF SSB phase noise	100kHz 1kHz 10Hz	-85 -78 -65	dBc/Hz dBc/Hz dBc/Hz
		PLL spurs		<35	dBc

NJ1017R – AD DA Interface ASIC

- 2 ADCs (for I/Q outputs of NJ1007R)
  - 3-bit
  - Sampling frequency < 50MHz
- 8-bit DAC (for AGC)
- SPI like interface to the base band processor
- PLL (for sampling clock)



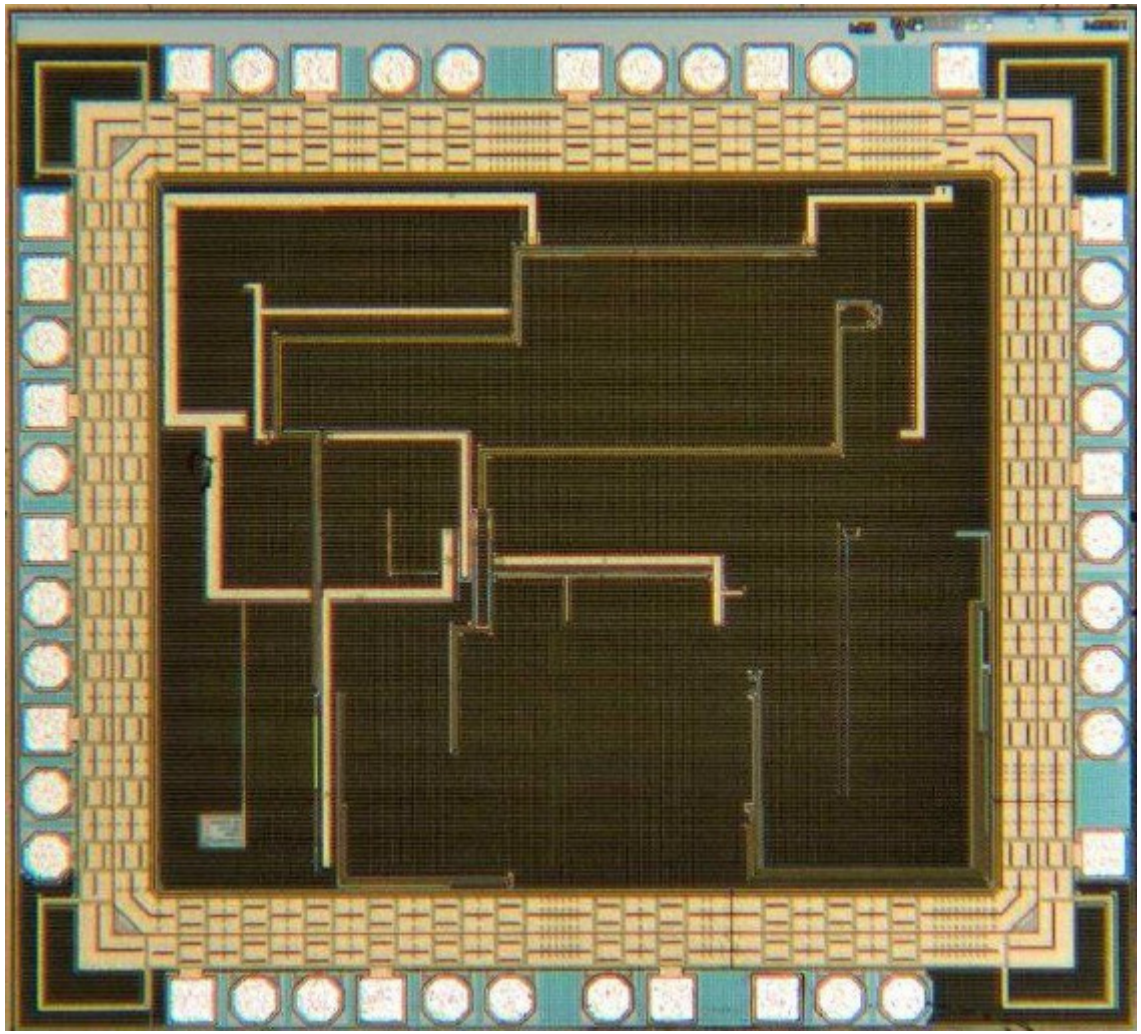




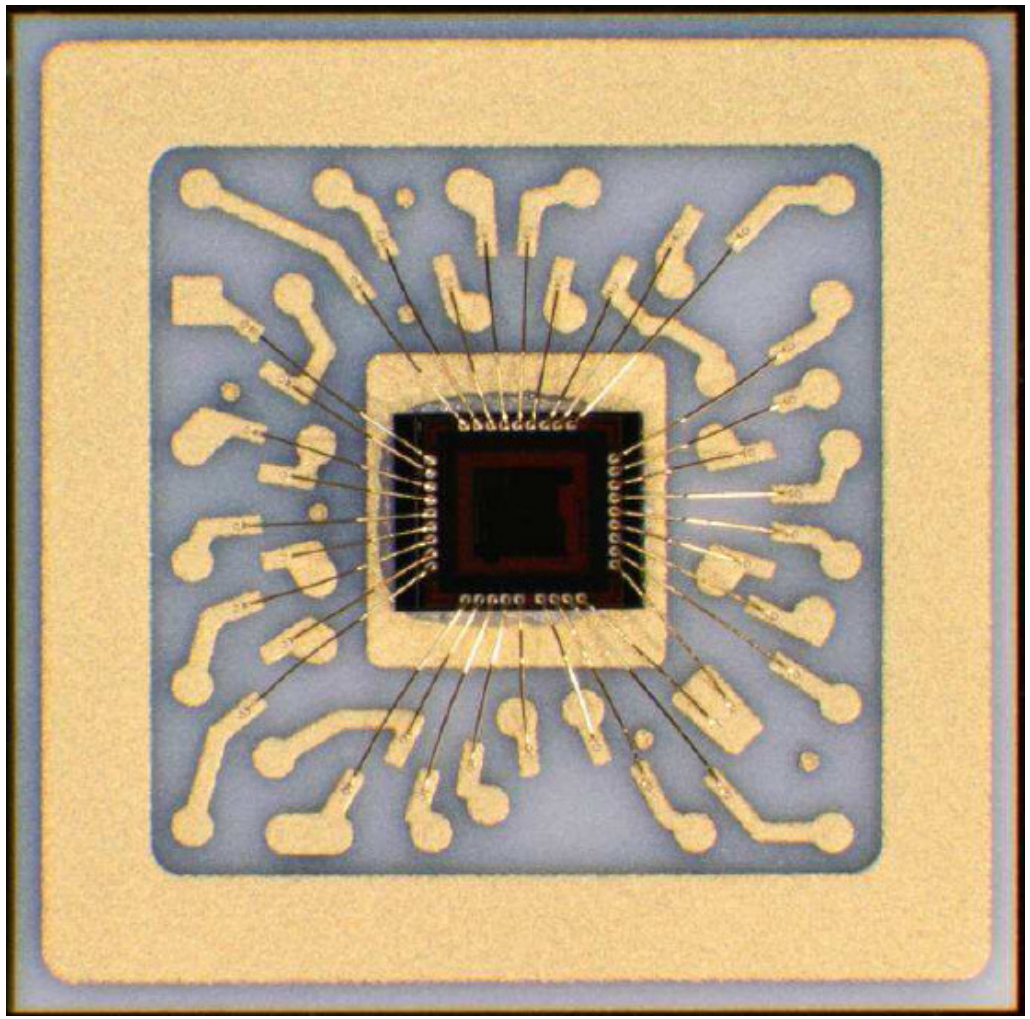
NJ1017R characteristics

NJ1017 (G3AD)	**3-bit ADC**	DNL		0.5	LSB
		INL		0.5	LSB
		Max sampling freq.		<50	MHz
		Input Voltage range		700	mVpp
		SFDR		25	dB
	AGC 8-bit DAC	DNL		3	LSB
		INL		3	LSB
		Output Voltage range		0 ... 2.1	V
	VCO, PLL	Frequency Range		25 … 100	MHz
		RF SSB phase noise	1MHz 10kHz 100Hz	-90 -60 -65	dB dB dB

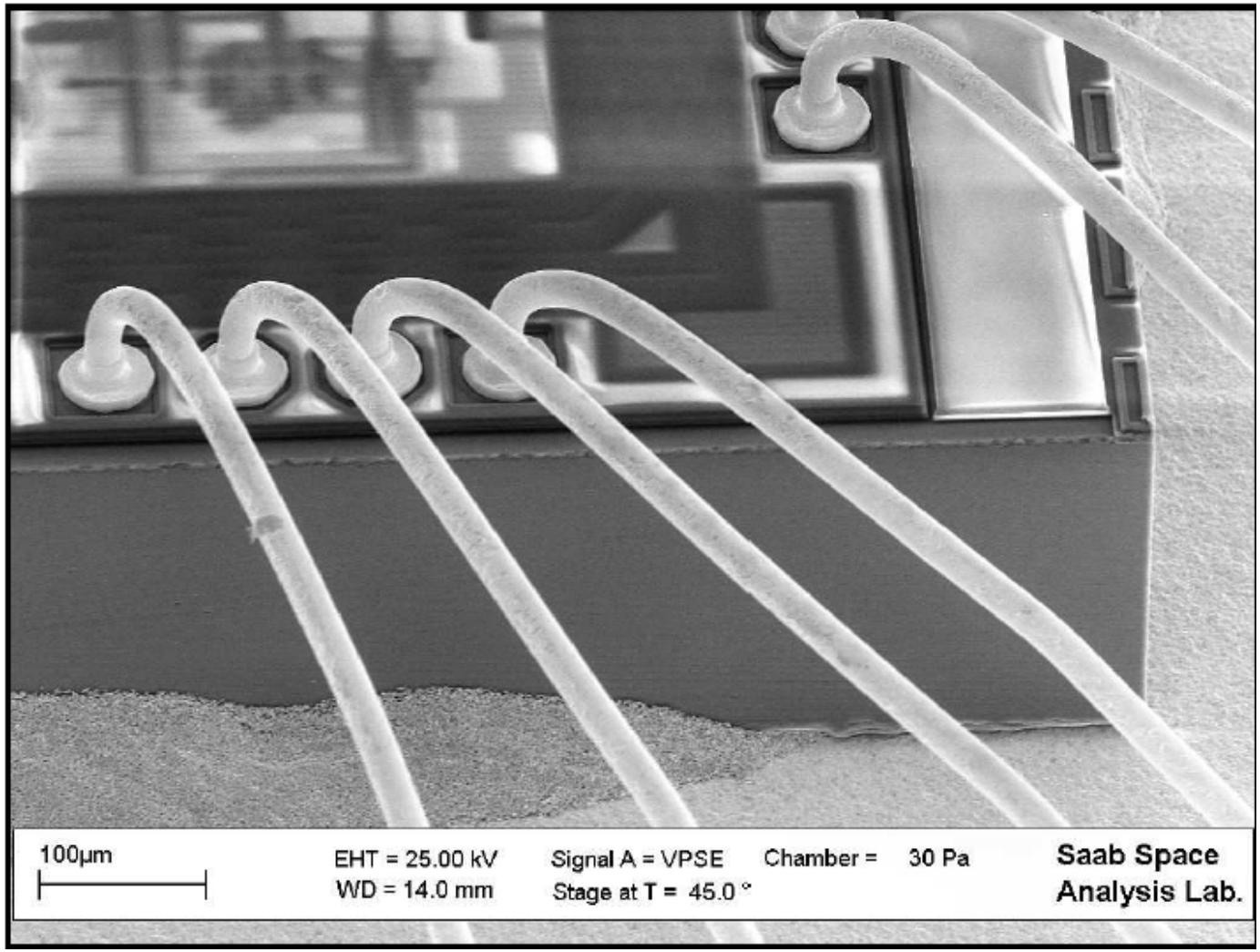
NJ1007R chip layout



NJ1007R chip on CBGA substrate



Close view of bonded NJ1007R



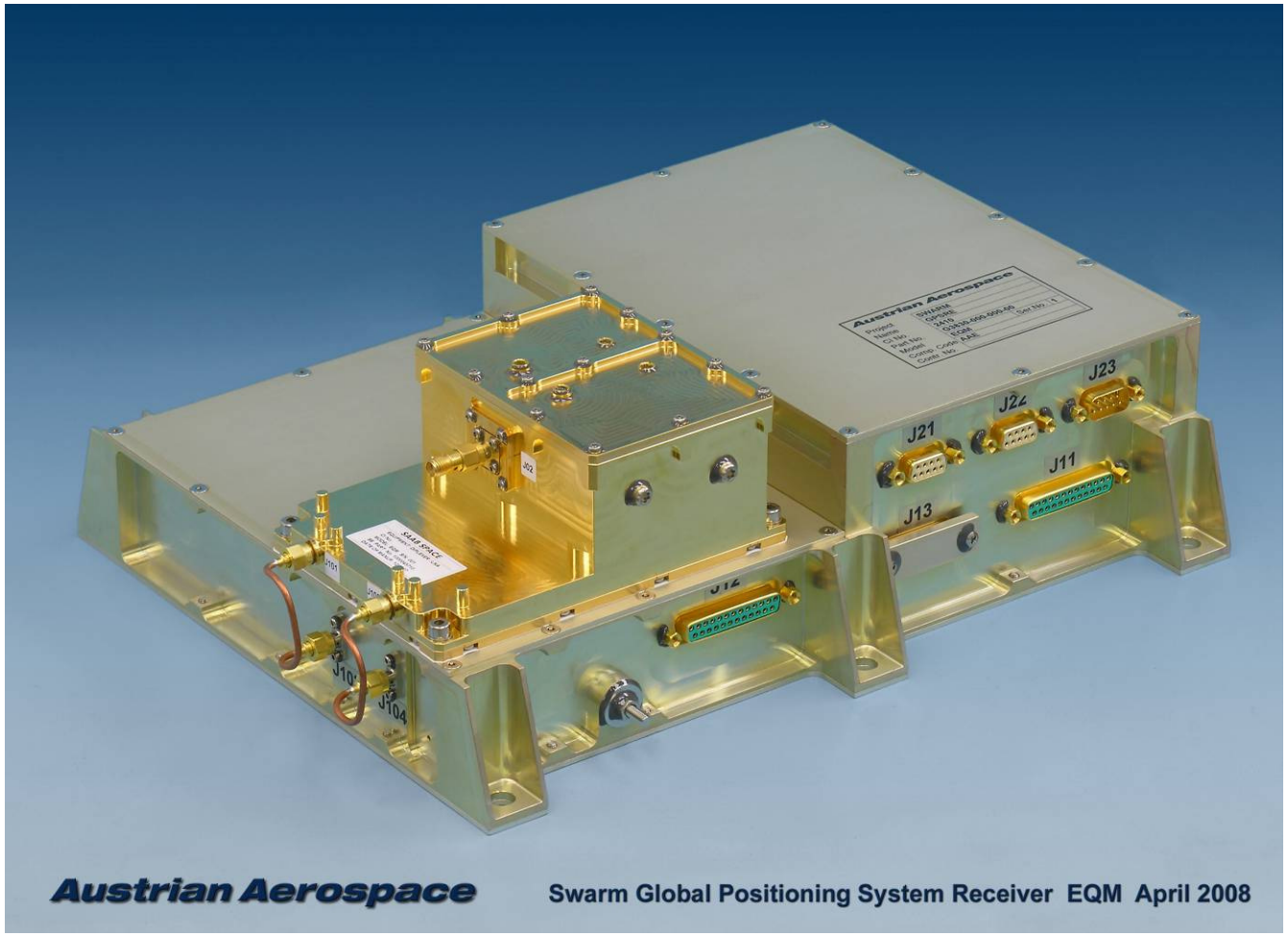
Overview of G3 chip set Lot Validation

- Project started in 2007
- Lot Validation based on ESCC9000 including
  - Wafer Manufacturing
  - Wafer Lot Acceptance including Total Ionizing (TID) Dose testing
  - Packaging of Evaluation Lot
  - Evaluation Test
  - Packaging of Flight Lot
  - Screening of Flight Lot
  - Lot validation of Flight Lot
- Completion expected early 2009

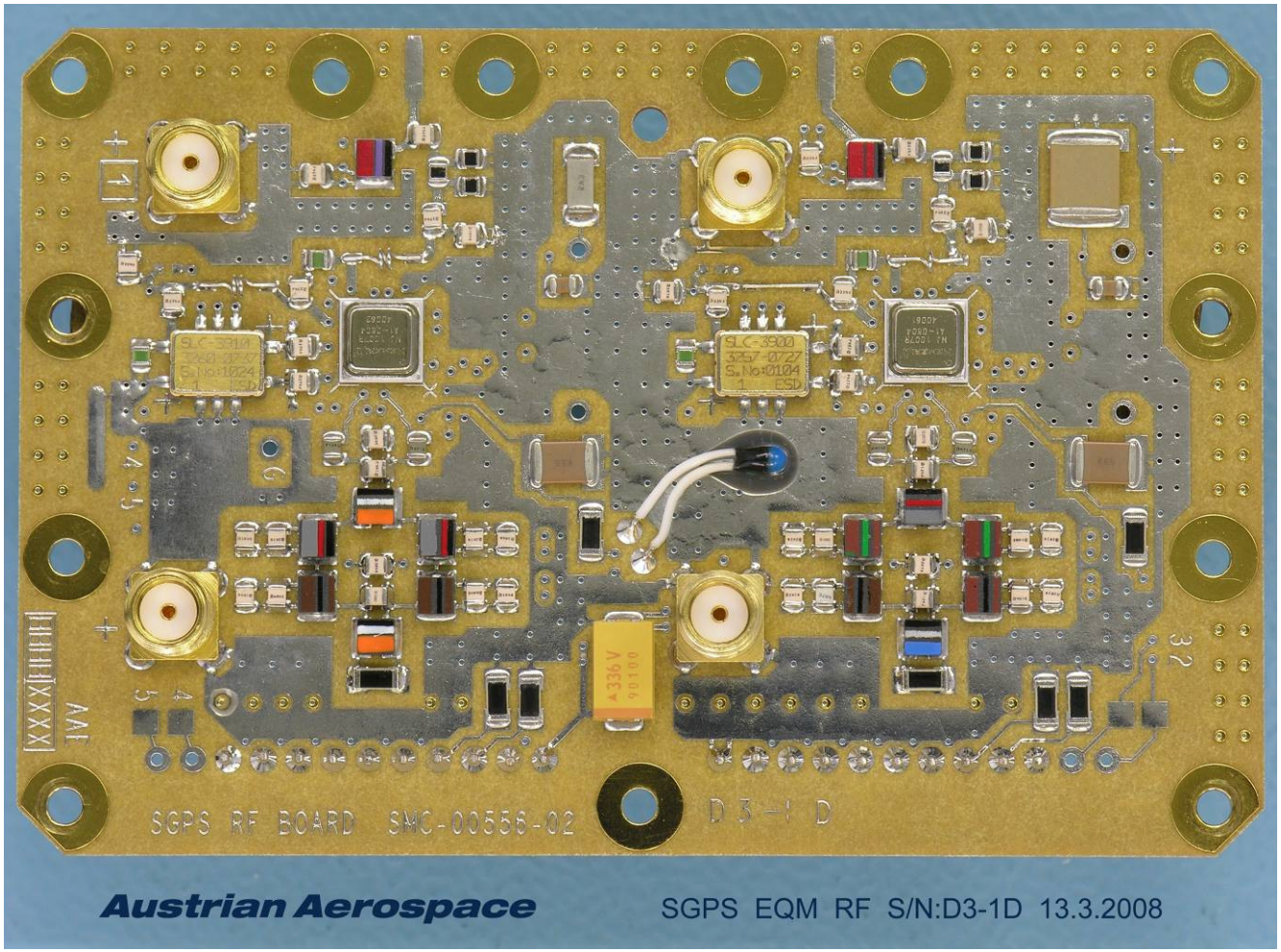
G3 chip set First Application

- GPS based Precise Orbit Determination (POD) Receiver for ESA-SWARM Mission
- Down-converts and digitizes the GPS L1 and L2 signals by means of Nj1007R and NJ1017R, RF- and mixed-signal ASICs
- AGGA-2 chips and a LEON processor form the heart of the digital signal processing

G3 chip set First Application



G3 chip set First Application



G3 chip set First Application

- Interfaces
  - UART (RS-422) TC/TM interface
  - MIL-STD-1553B TC/TM interface extension
- Electronic Box
  - Box Size: 322x240x104 mm^3
  - Weight: < 3.5 kg including antenna
  - Power Consumption: < 10W
- Antenna
  - Patch Excited Cup Antenna with improved multipath suppression from Saab Space

Conclusions

- G3 Chipset consists of RF Front-End and AD Converter
- Chipset is Radiation Tolerant (120 krad(Si); 84 MeV/mg/cm^2)
- G3 ASICs are Being Qualified to ESCC9000
- First Application for SWARM Mission (under construction)

Thank you for your attention