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First radiation test results of the SiGe Technology SGB25V of IHP

September 2nd, 2008 – 14:15

Kayser-Threde GmbH, Munich / Heinz-Volker Heyer

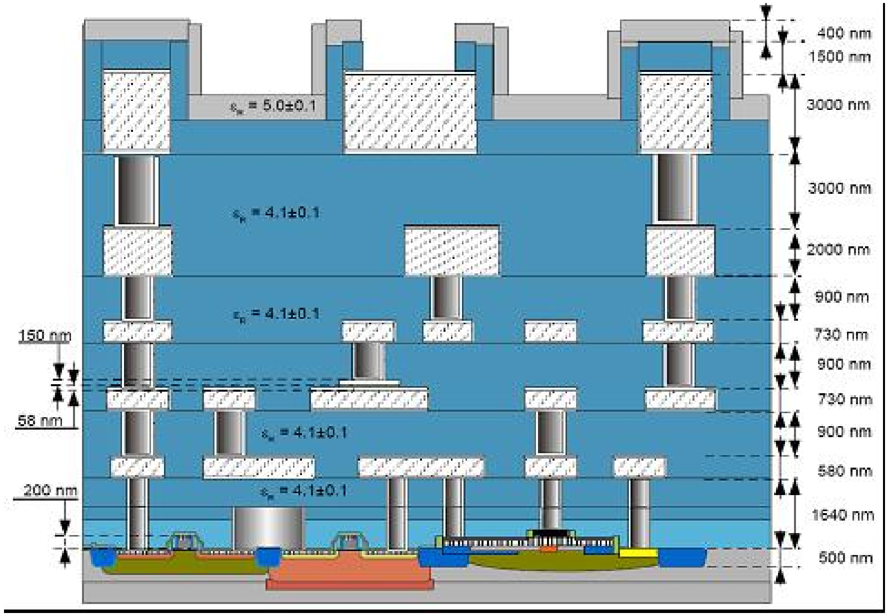
Contents

Overview radiation test

- **Baseline:** **Characterization of the IHP SiGe SGB25VD BiCMOS process regarding its sensitivity to a radiation environment.**
- **Goal:** **Derive inputs for the design of the local oscillator and future applications.**

- **Test program:**
  - **Total dose tests (7 samples biased, 3 samples unbiased, 1 reference sample)**
    - **High dose rate**
    - **Low dose rate**
  - **SEE tests (2 samples, 1 reference sample)**
    - **Single Event Effects**
    - **Latch-up**
  - **Displacement damage tests (4 samples, 1 reference sample)**
    - **Degradation**

Overview SGB25V technology



Parameter	High Performance	Standard	High Voltage
Bipolar Section			
A_E	0.42 x 0.84 µm^2		
Peak f_{max}	95 GHz	90 GHz	70 GHz
Peak f_T	75 GHz	45 GHz	25 GHz
BV_{CE0}	2.4 V	4 V	7 V
BV_{CB0}	>7 V	>15 V	>20 V
V_A	>50 V	>80 V	>100 V
ß	190		

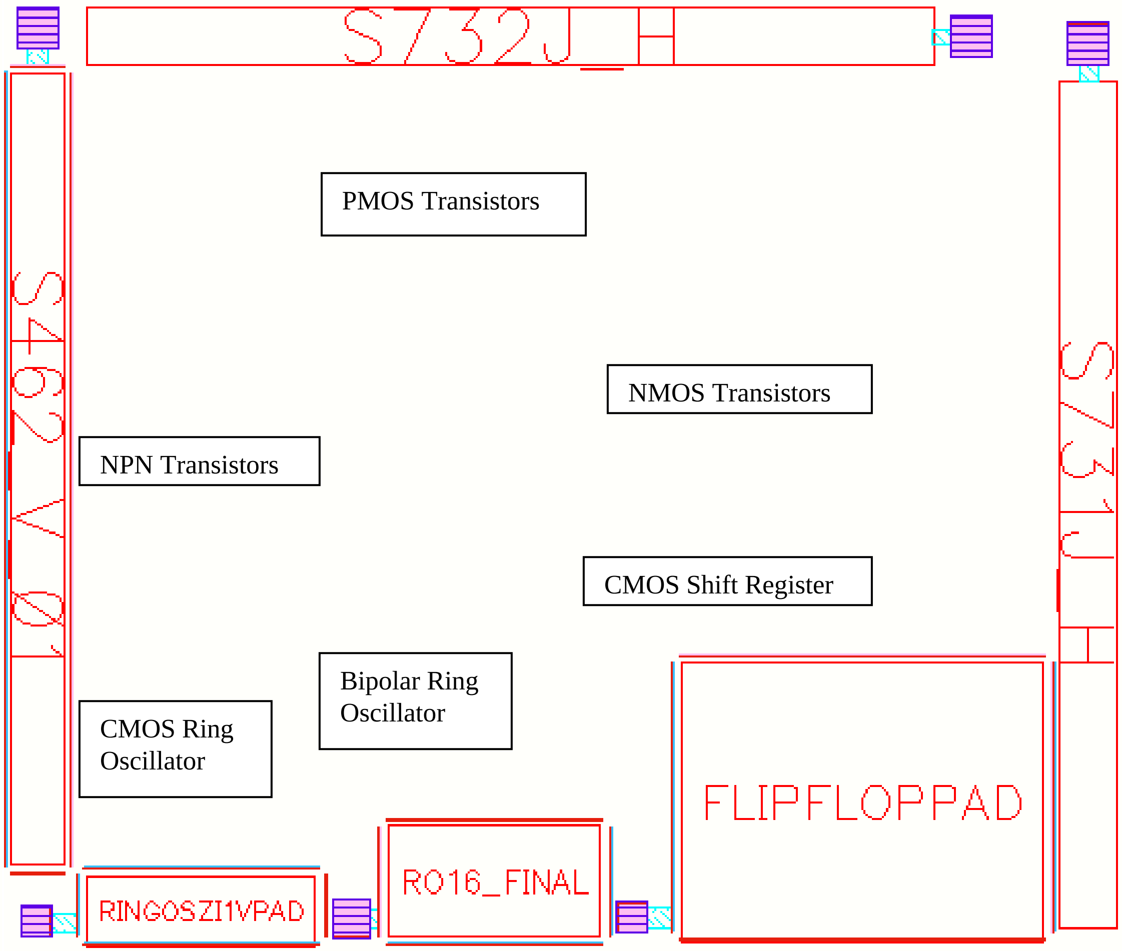
Parameter	SGB25VD
CMOS Section (0.25 µm)	
Core Supply Voltage	2.5 V
nMOS V_{th}	0.6 V
nMOS I_{Dsat}	570 µA/µm
nMOS I_{off}	3 pA/µm
pMOS V_{th}	-0.51 V
pMOS I_{Dsat}	290 µA/µm
pMOS I_{off}	3 pA/µm

Test samples (1)

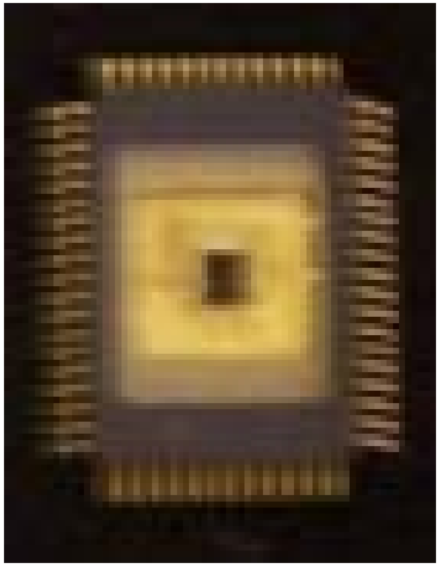
- **Each chip with test structures included:**
  - **3 bipolar NPN transistors of type npnVh (standard)**
  - **3 bipolar NPN transistors of type npnVp (increased V_{CE} breakthrough voltage)**
  - **3 bipolar NPN transistors of type npnVs (speed optimized)**
  - **1 NMOS transistor 25 x 0.24µm^2 (W x L), 1 NMOS transistor 25 x 25µm^2 (W x L) >>> common gate and common source**
  - **1 PMOS transistor 25 x 0.24µm^2 (W x L), 1 PMOS transistor 25 x 25µm^2 (W x L) >>> common gate and common source**
  - **1 CMOS ring oscillator (CRO) with 100 inverters plus 1 NAND logic (transistors: 0.24 x 0.48µm$^{2)}$**
  - **1 bipolar ring oscillator (BRO) with 53 CML circuits (transistors: type npnVp)**
  - **1 CMOS shift register (SR) with 10 blocks of 100 D-FF plus 1 inverter (transistors: 0.24 x 0.48µm^2 and 0.24 x 1.1µm^2)**

- **Each structure is protected by guard rings which are all connected to power GND.**

Test samples (2)

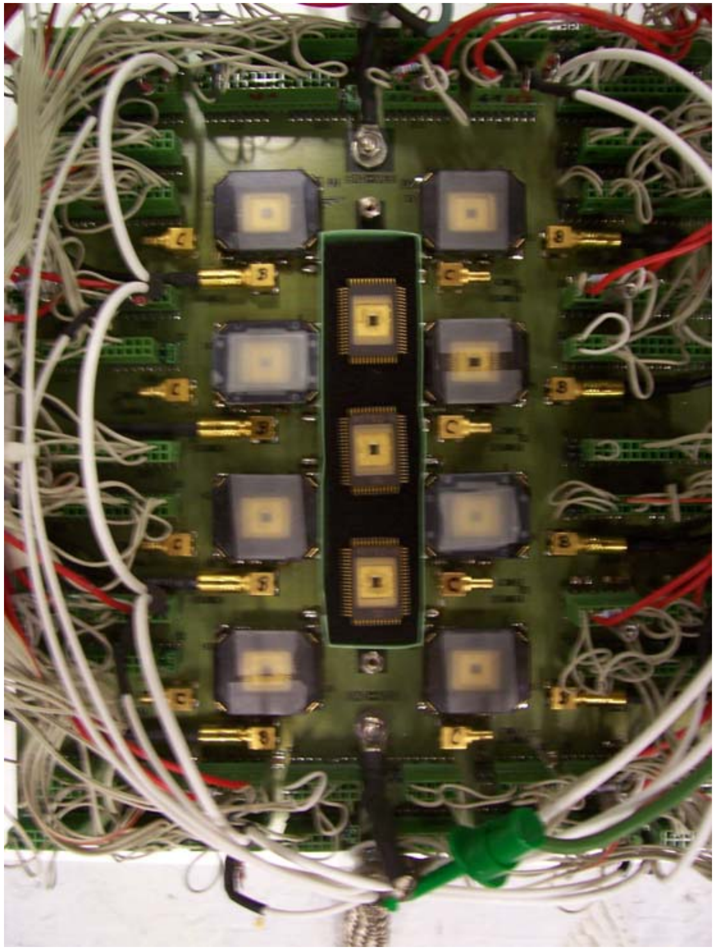


Chips are wire bonded to a 64 CQFP carrier with open lid.



Test board TID (1)

- **Up to 8 samples could be installed and tested at the same time.**
- **Test sockets were used to take up the test samples.**
- **Unbiased samples were placed on conductive foam in between the two rows of biased ones.**
- **The distance between biased and unbiased samples to the board was equalized.**
- **SMB connectors were used to get access to the outputs of the CMOS ring oscillators and shift registers.**
- **The area to be irradiated was about 15 x 10 cm^2.**

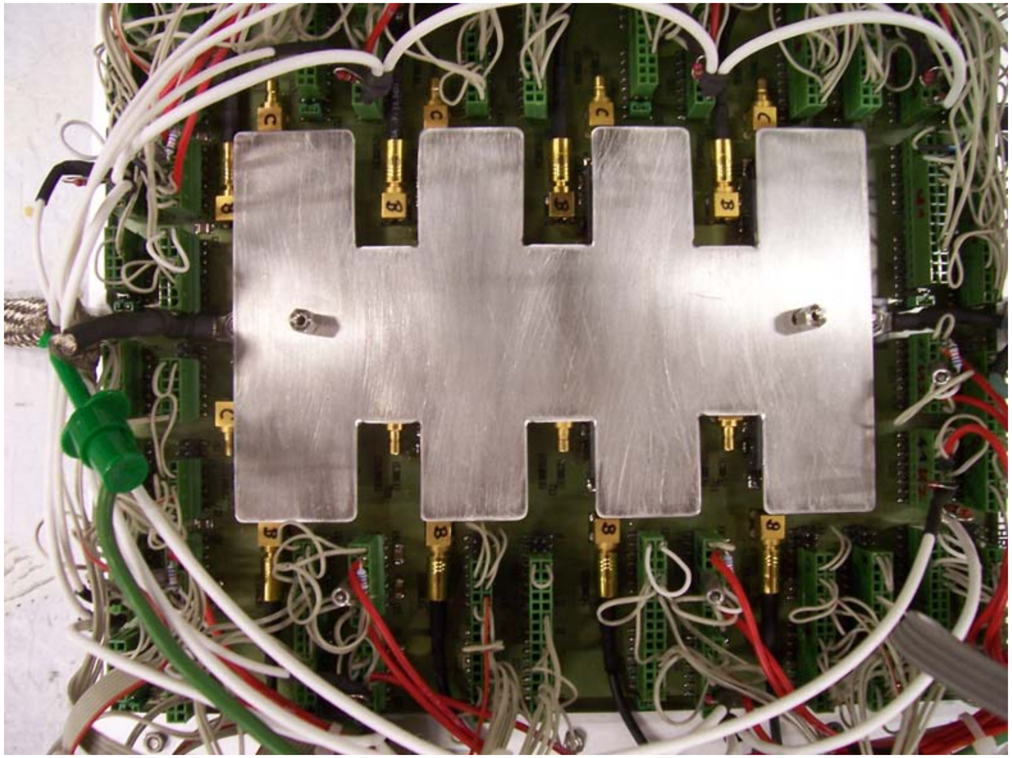


Test board with samples

Test board TID (2)

- **Charged particle equilibrium was ensured by an aluminum plate of 2 mm in front of the samples.**

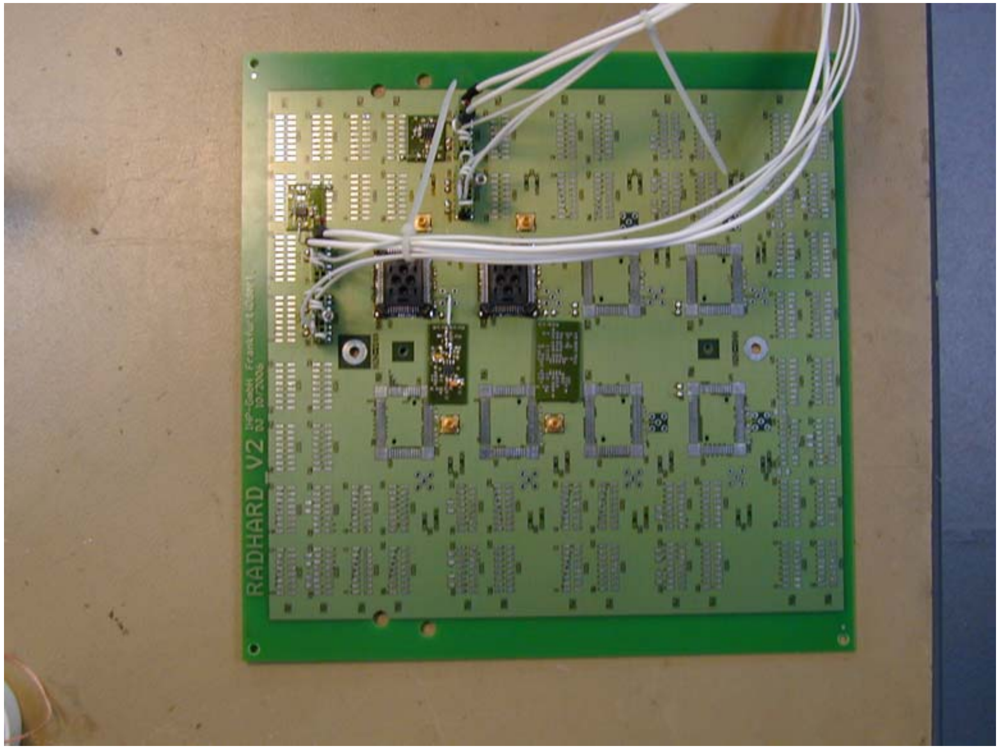
- **The distance to the samples was minimized but determined by the RF connectors.**



Test board with cover

Test board SEE

- **The board was designed to fit to a sample board holder as defined in ECSS 25100.**
- **Test sockets were used to take up 2 test samples.**
- **For online measurement of output signals, level shifter and line driver were installed close to shift registers and oscillators.**
- **Only one sample was irradiated, biased, and verified at a time.**
- **Transistors were not biased during irradiation.**
- **For verification of all structures after irradiation the TID sample board and unit tester were used.**

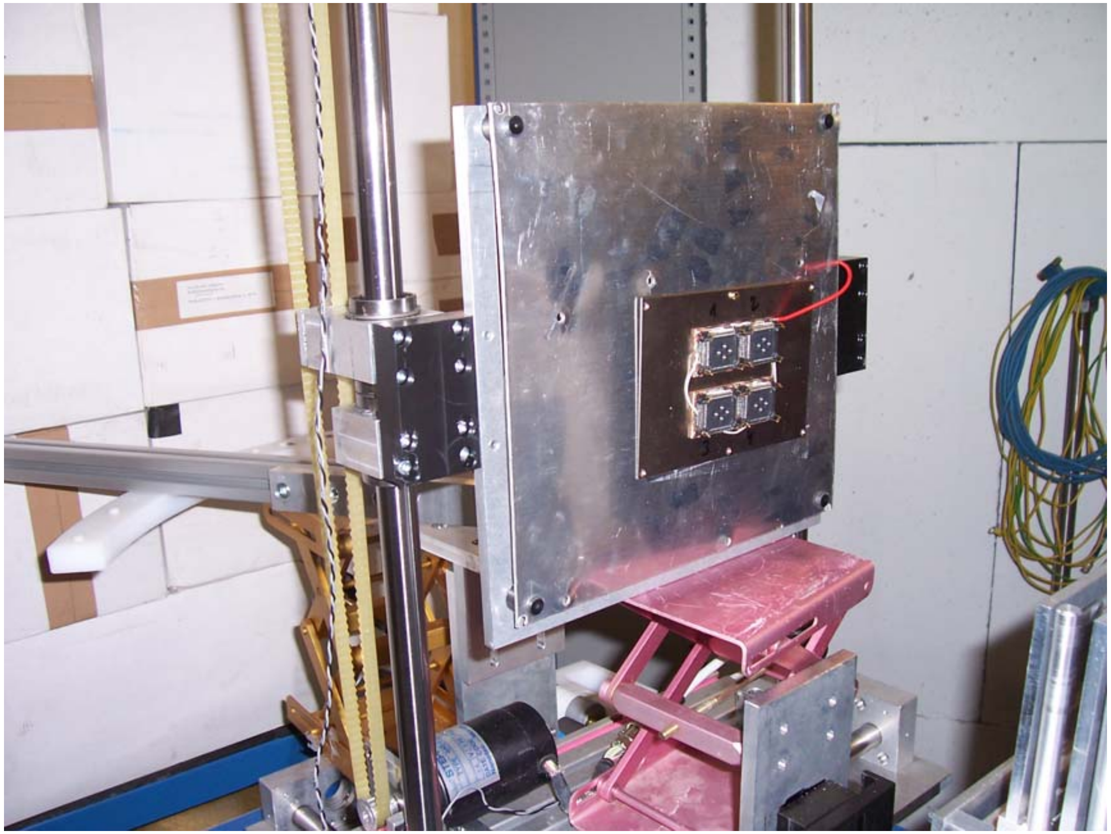


Test board

Test board DD

- **A dedicated board was designed to take up 4 passive samples on test sockets.**

- **The area was limited to 5 x 5cm² to ensure a uniform proton density across the samples.**

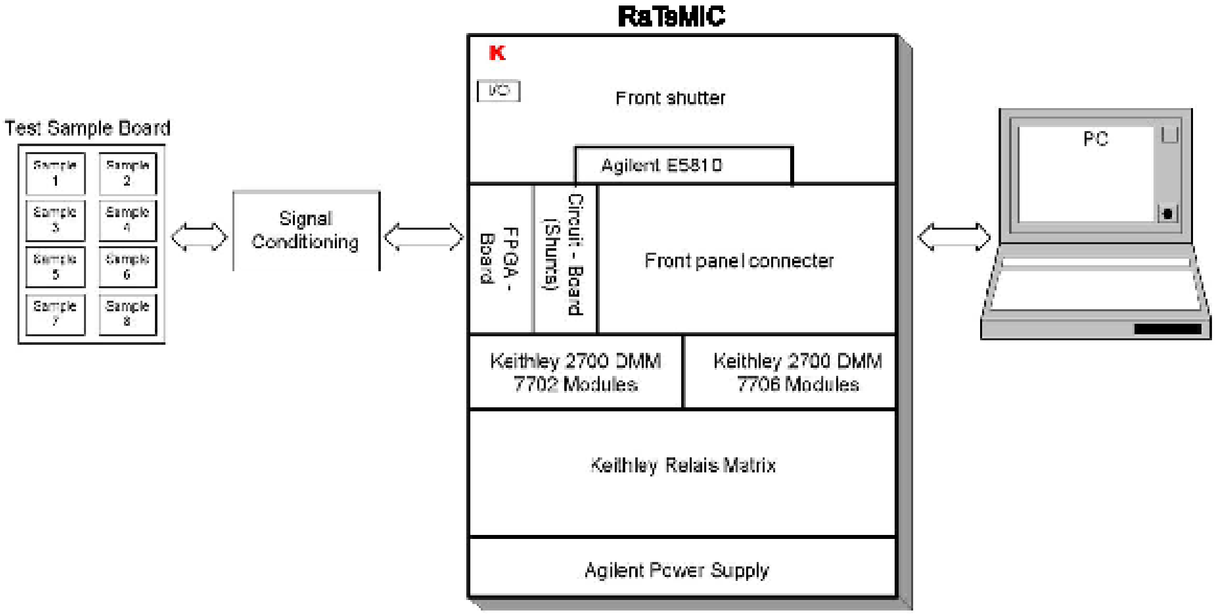


Test board

Test equipment

Unit tester:

- **Laptop**
  - **Control, data storage**
- **Measurement equipment**
  - **Biasing, data acquisition**
- **Signal conditioning electronics**
  - **Filters, buffers**



- **Interfaces:**
  - **Laptop – rack: LAN (30m)**
  - **Rack – signal conditioner: about 2.5m**
  - **Signal conditioner – sample board: about 1m**

- **Monitoring of measurements via VPN tool**

TID verification (1)

Measured parameters

- **Shift registers: time delay, power supply current**
- **Ring oscillators: frequency, power supply current**
- **Transistors: see tables below**

Verification of NPN-Transistors

Modes:	**Basic**	**“Gummel - 0V”**	**“Gummel - 1V”**	**“Break Through”**
U_{CE}	1V	0V	1V	open
U_{BE}	0.7V	0…1V in steps of 0,1V	0…1V in steps of 0,1V	0…5V in steps of 0,1V
Measured Parameters		U_{CE}, U_{BE}, I_C, I_B	U_{CE}, U_{BE}, I_C, I_B	U_{CE}, U_{BE}, I_C, I_B
Plots		I_C and I_B over U_{BE} @ different TID levels	I_C and I_B over U_{BE} @ different TID levels	I_B over U_{BE} @ different TID levels

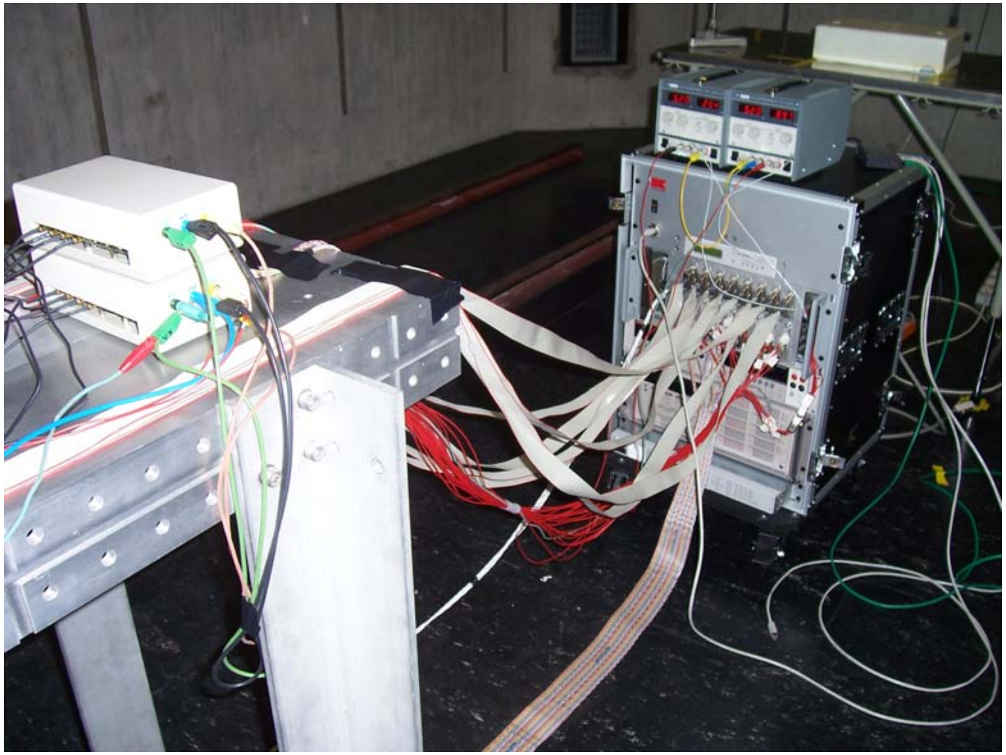
Verification of P-/NMOS-Transistors

Modes:	**Basic**	**“Threshold”**	**“Saturation”**	**“Leakage”**
U_{DS}	-0,1V / 0,1V	-0,1V / 0,1V	-2,5V / +2,5V	-2,5V / +2,5V
U_{GS}	-2V / 2V	0…-2,5 / +2,5V in steps of 0,25V	0…-2,5 / +2,5V in steps of 0,25V	0V
Measured Parameters		U_{GS}, U_{DS}, I_D	U_{GS}, U_{DS}, I_D	U_{GS}, U_{DS}, I_D
Plots		I_D over U_{GS} @ different TID levels	I_D over U_{GS} @ different TID levels	I_G @ different TID levels

TID verification (2)

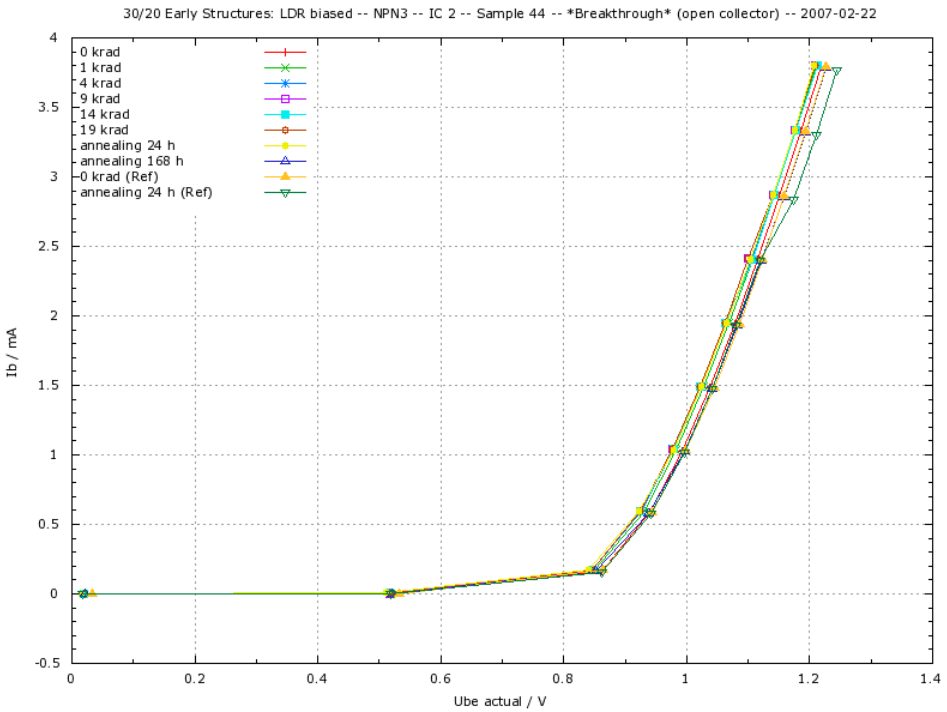
- **Test facility: GSF, Neuherberg/München**
- **Test program:**
  - **High dose rate – 200krad @ 2rad/s**
  - **24h annealing @ ambient temperature**
  - **168h annealing @ 100°C**

  - **Low dose rate – 20krad @ 0.02rad/s**
  - **24h annealing @ ambient temperature**
  - **168h annealing @ ambient temperature**
- **Summary of test results:**
  - **All structures passed the irradiation tests.**
  - **No distinct ELDR effects were seen.**
  - **Only low drifts were detected on transistor elements as well as on complex structures.**

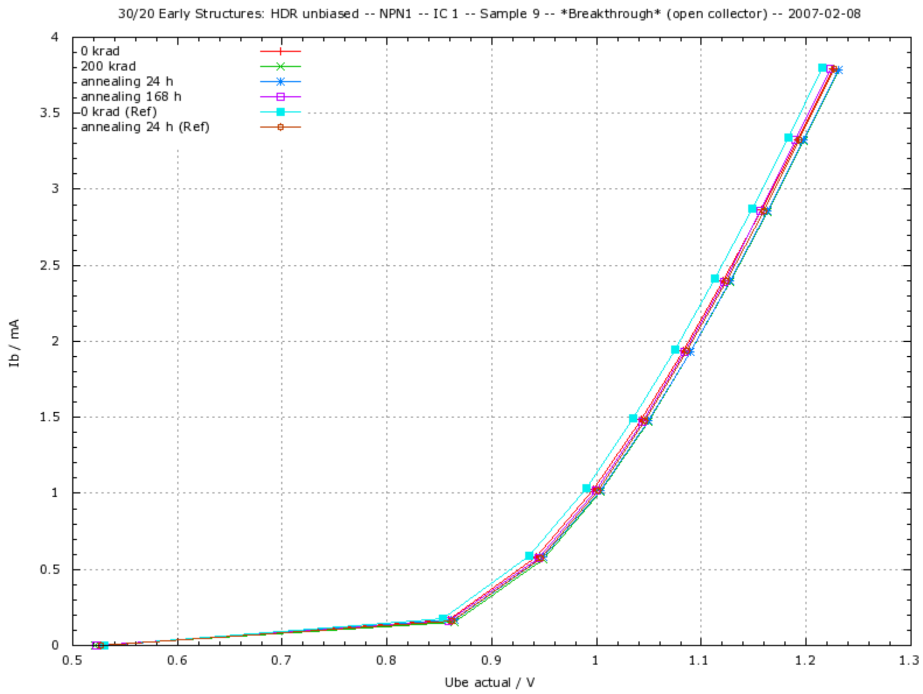


Test set-up

TID verification (3)

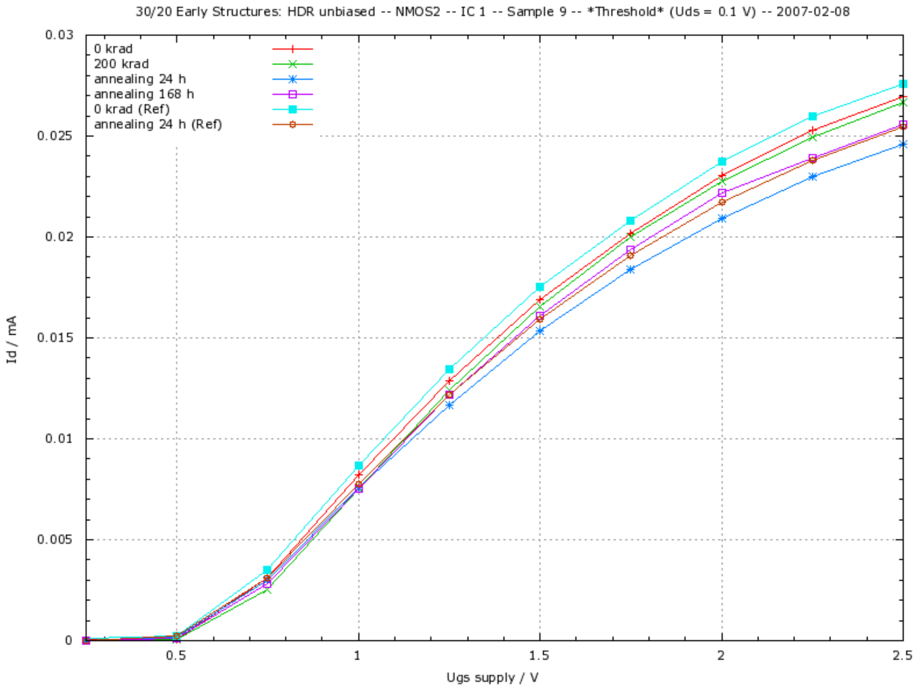


Low Dose Rate Tests (biased)
Plots of NPN-T3 transistors with no degradation after annealing (yellow and blue curves)



High Dose rate tests (unbiased)
Plots of NPN-T1Transistors

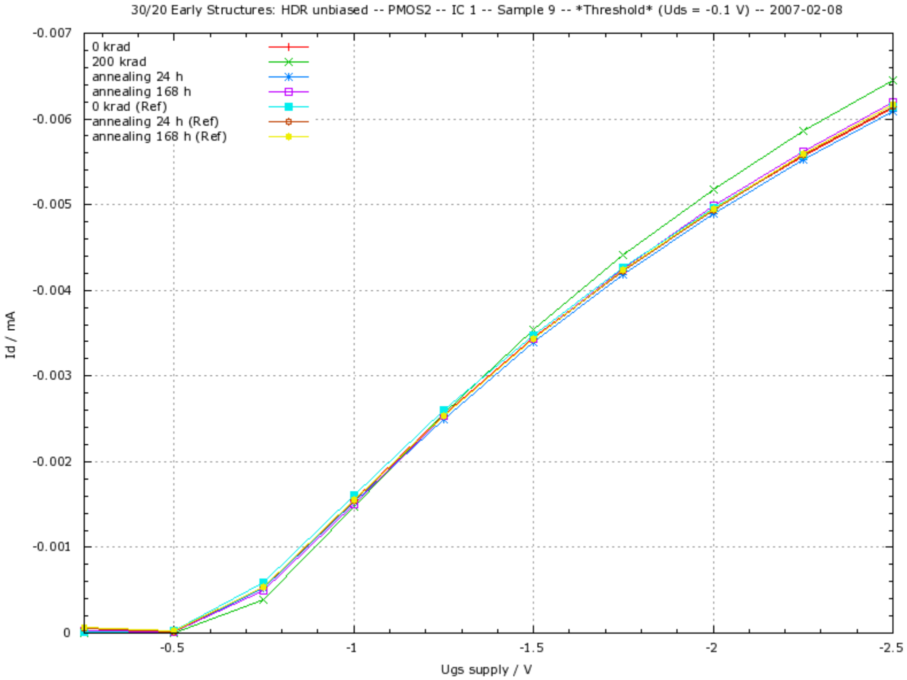
TID verification (4)



High Dose Rate Tests

Plots of N-MOS T2-transistors

(Threshold measurements)



High Dose Rate Tests

Plots of P-MOS T2-transistors

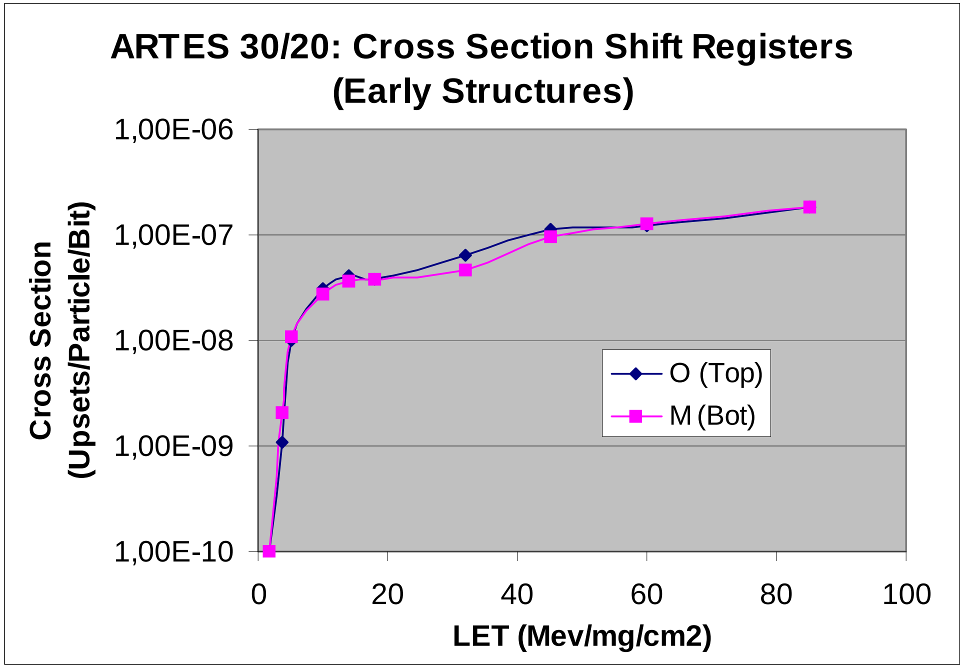
(Threshold measurements)

SEE verification (1)

- **Test facility: RADEF, Jyvaskyla/Finland**
- **Test program:**
  - **Determination of the cross-section in the LET range of 1.8 to 85MeV/mg/cm^2**
  - **Verification of latch-up sensitivity at elevated temperature (about 60°C)**
  - **Test of dynamic and static mode of shift registers**
  - **Check for transients at oscillator outputs.**
- **Summary of test results:**
  - **All structures passed the irradiation tests**
  - **The upset threshold is rather low. Upsets could already be detected at 3.6MeV/mg/cm^2**
  - **No latch-up occurred up to 85MeV/mg/cm^2**
  - **Error rates of static and dynamic modes correspond**
  - **No transients were detected on oscillator output signals with the given set-up (limited resolution).**

Test facility

SEE verification (2)

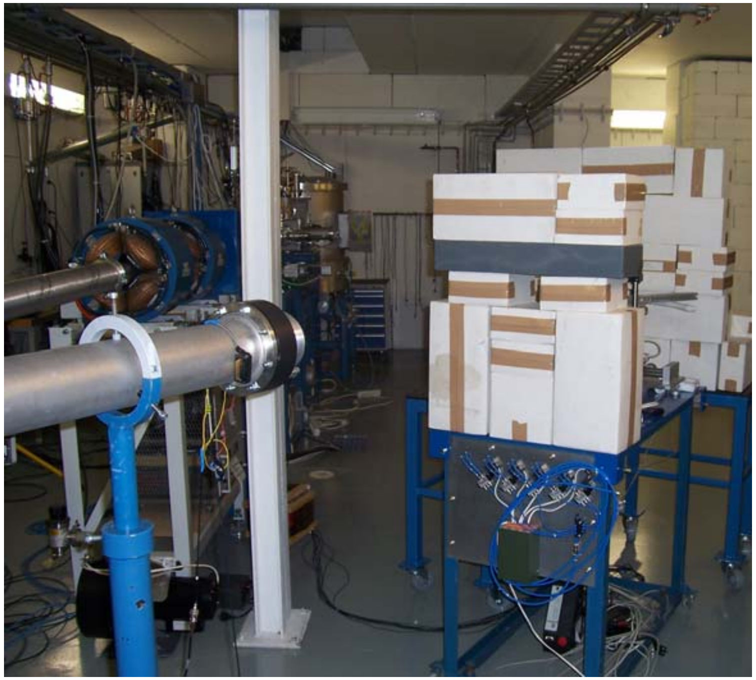


			TOP	Sample "O"			
Particles	LET	Angle	Fluence	Dose	Upsets	Cross Section	Remarks
N	1,8	0	1,00E+07	288,396	1	1,00E-10	
Ne	3,6	0	1,00E+07	576,792	11	1,10E-09	
Ne	5	45	1,00E+07	801,1	99	9,90E-09	
Ar	10,1	0	5,00E+06	809,111	156	3,12E-08	
Ar	14,1	45	5,00E+06	1129,551	203	4,06E-08	
Fe	18	0	2,00E+06	576,792	67	3,35E-08	
Fe	18	0	1,00E+07	2883,96	422	4,22E-08	Control Measurement
Fe mean	18					3,79E-08	
Kr	32,1	0	1,00E+07	5143,062	648	6,48E-08	
Kr	45	45	1,00E+06	720,99	108	1,08E-07	
Kr	45	45	1,00E+06	720,99	122	1,22E-07	Control Measurement
Kr mean	45					1,15E-07	
Xe	60	60	1,10E+07	10574,52	1338	1,22E-07	
Xe	85	45	1,00E+07	13618,7	1804	1,80E-07	
TID	krad			37843,964			

Displacement damage verification (1)

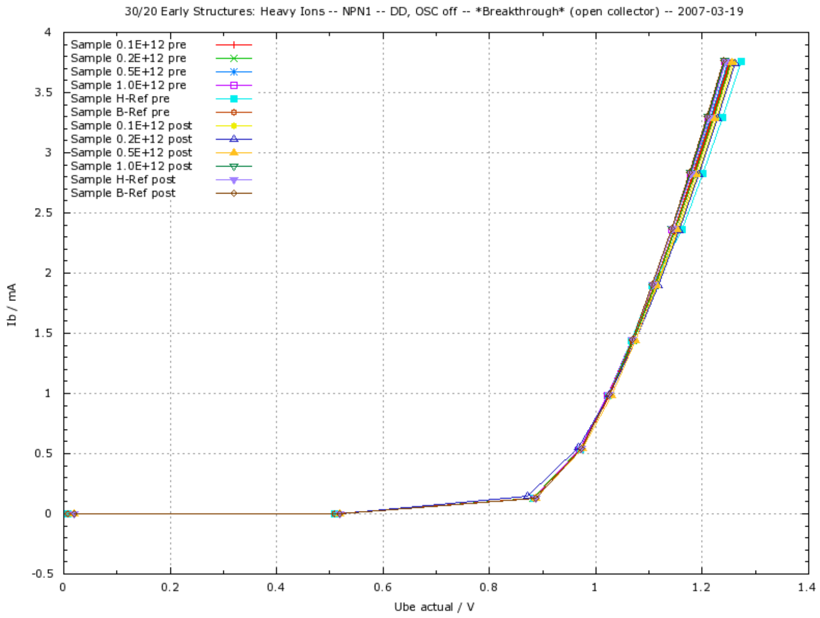
- Test facility: RADEF, Jyvaskyla/Finland
- Test program:
  - **Determination of degradation after 1E+11, 2E+11, 5E+11 and 1E+12 protons**
  - **Application of protons of 30MeV**
  - **Applied flux was about 1E+8 particles/cm²/s.**

- Summary of test results:
  - **All structures passed the irradiation tests**
  - **No distinct degradation effects could be identified.**



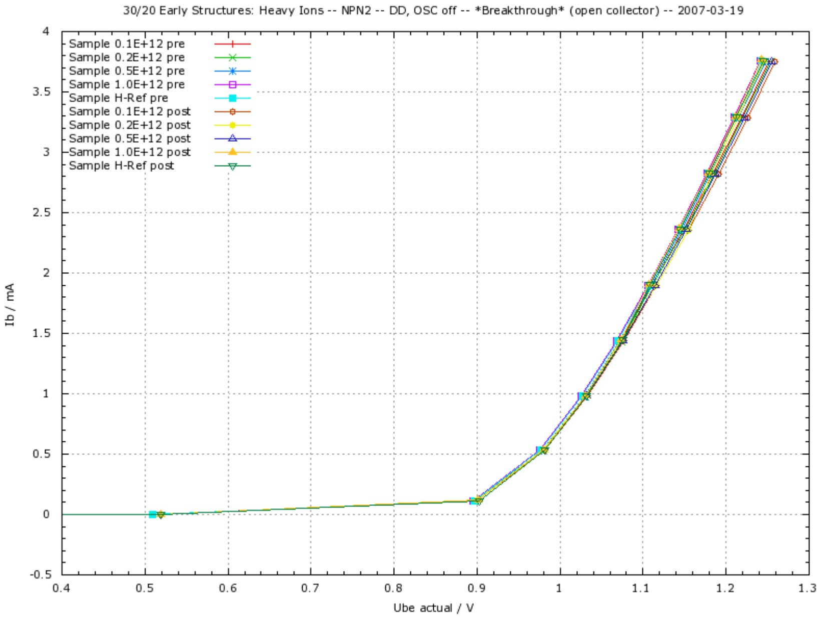
Test setup

Displacement damage verification (2)



Plots of NPN-T1transistors

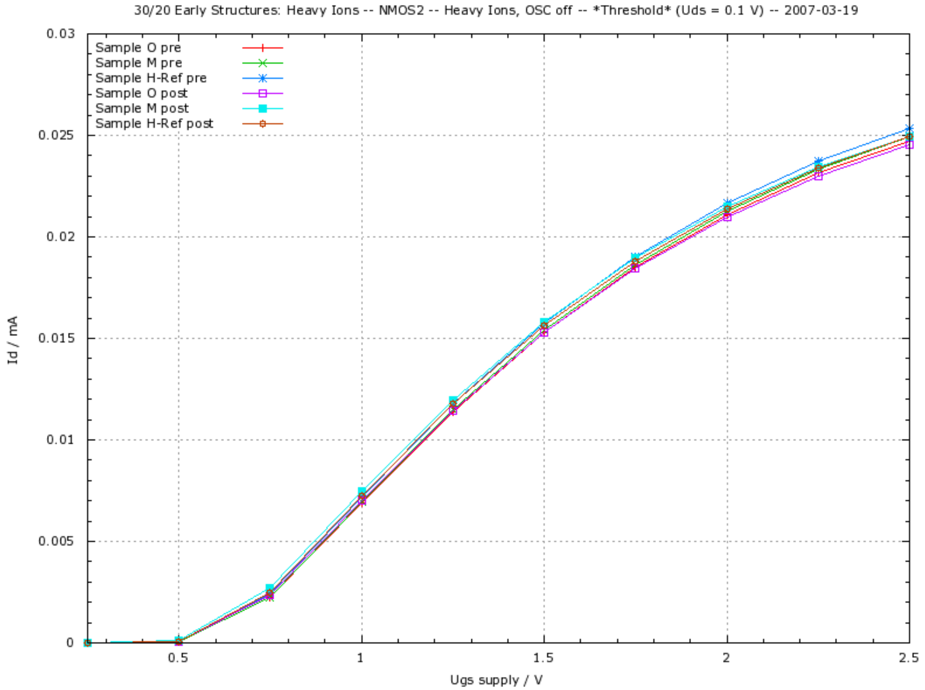
(Breakthrough measurements)

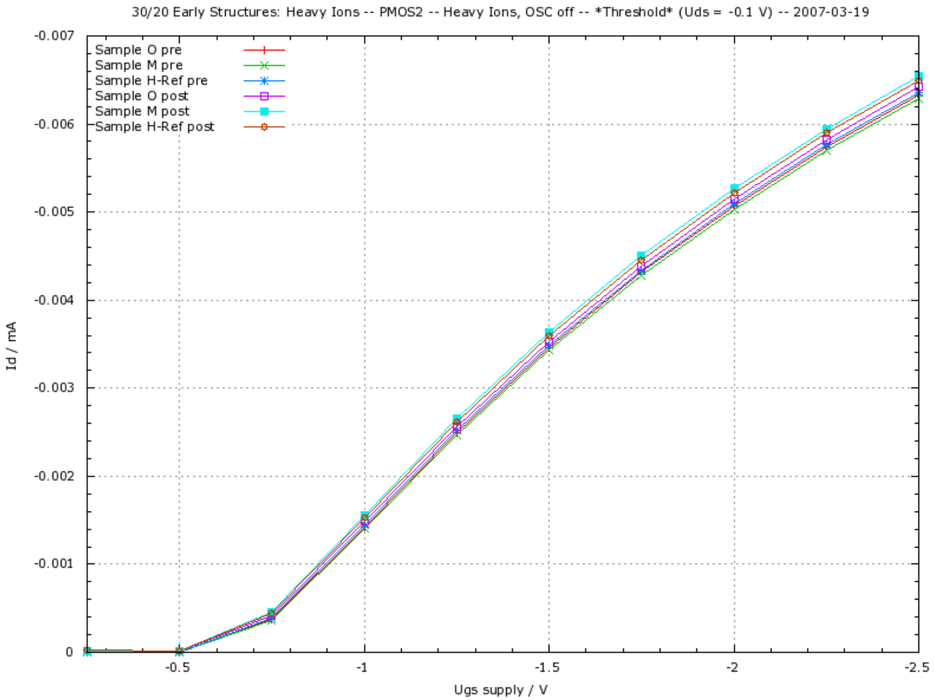


Plots of NPN-T2 transistors

(Breakthrough measurements)

Displacement damage verification (3)





Plots of NMOS-2 transistors
(Threshold measurements)

Plots of PMOS-2 transistors
(Threshold measurements)

Conclusion

- **TID**
  - The technology only shows minor degradation up to the maximum tested level of 200krad.
  - No distinct ELDR effects were detected.
- **SEE**
  - No latch-up occurred up to the tested value of 85MeV/mg/cm^2.
  - The technology is sensitive to bit-flips. The SEU threshold is below 3.6MeV/mg/cm^2.
- **DD**
  - The technology only shows negligible degradation effects up to the tested value of 1E+12 protons/ cm^2.