A 10-bit, 1.8-GS/s Time-Interleaved Pipeline ADC

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Business from technology

Outline

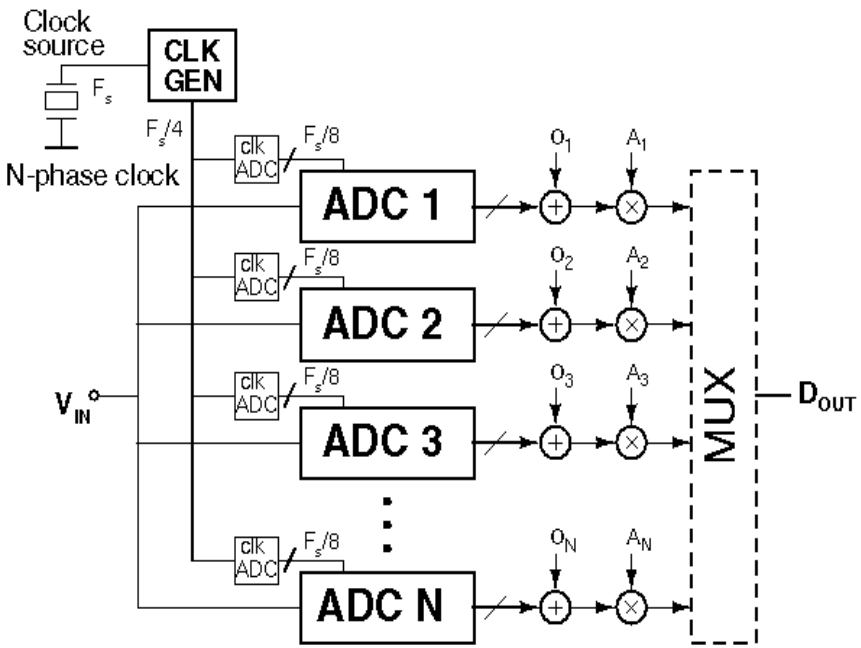
- Specifications for ADC
- Time-interleaved Pipeline ADC
  - Nonidealities, calibration
  - Architecture
  - Circuit block design
- Experimental results
- Summary

Specifications for ADC

- A satellite communicational system for ESA (European Space Agency)
- 1.8 GS/s , 10 bit resolution
- Signal bandwidth up to 500 MHz
- As low power consumption as possible
- A time- interleaved pipeline ADC topology was selected
    - A conventional flash topology was found to have too high power consumption @ 10 bit

Time-Interleaved (TI) Pipeline ADC

- Conversion rate can be increased by using time-interleaved pipeline ADC
- Resolution range (8-10 bits) suitable for pipeline topology
- Calibration is needed to overcome device mismatch and nonidealities



Nonidealities of the TI ADC, #1

- Offset
  - Device mismatch in opamps
  - Charge injection of sampling switches
    → Tones $f_s \cdot k/M$
    → Constant error
- Gain mismatch
  - Capacitor mismatch
  - Limited performance of opamp
    → Unwanted sidebands to the output spectrum
    $\pm f_{in} \pm f_s \cdot k/M$, k=1, 2, 3, …, M-1

CALIBRATION

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Multiplying output data by proper coefficients

(M = number of channels)

Nonidealities of the TI ADC, #2

- Timing mismatch
  - Timing skew causes spurs at the same frequencies as gain mismatch
    - input frequency dependent
    - Can be avoided by using a full speed sample-and-hold (S/H) circuit or tunable delay locked loop (DLL)
  - Sampling clock jitter degrades SNR by increasing noise floor

CALIBRATION

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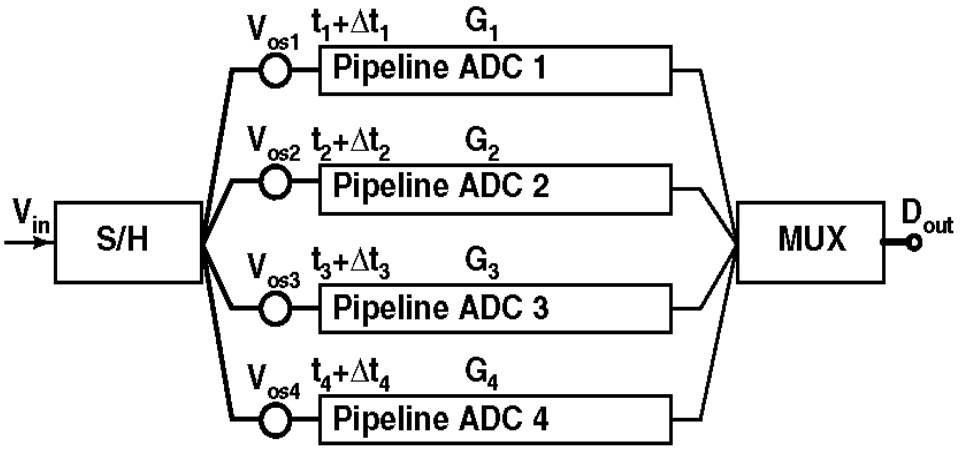
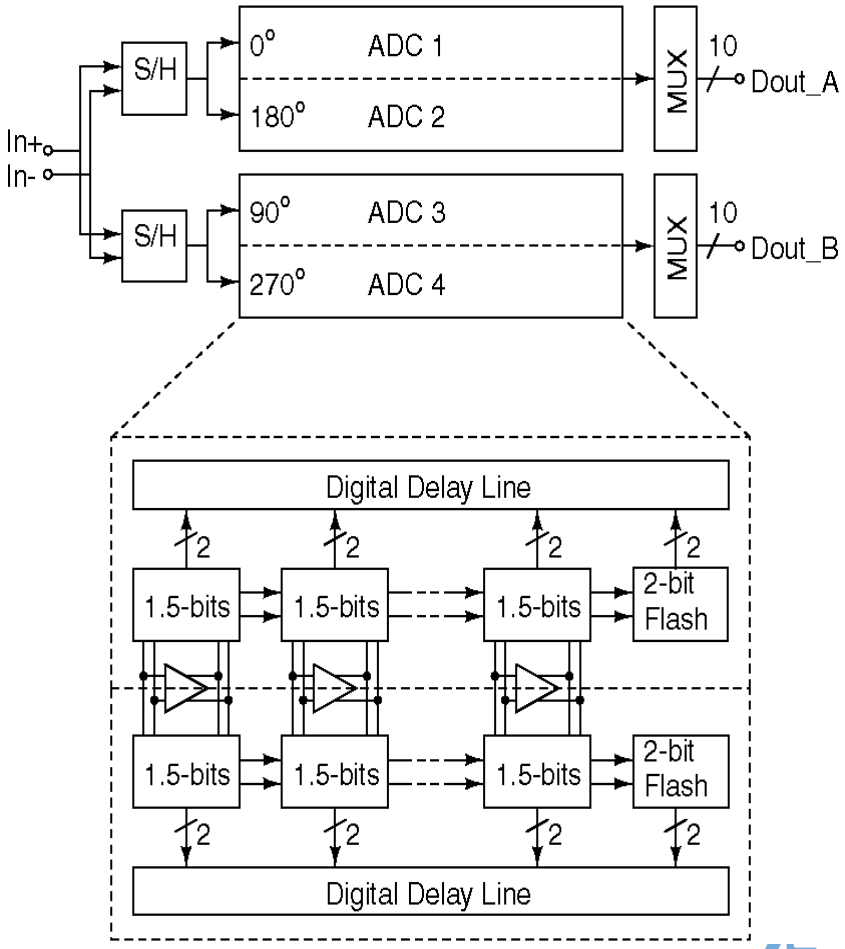
The goal is to minimize skew in the clock path to the sampling switches
This can be done by adjusting the delay of DLL



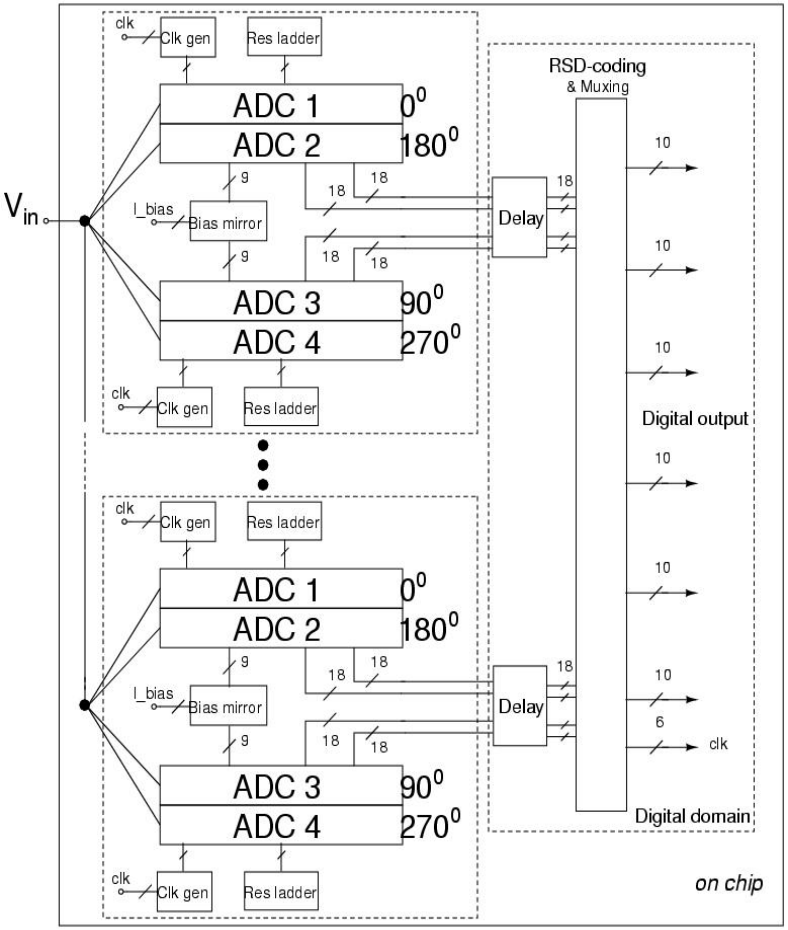
24-Channel ADC, #1

- 6x4 10-bit 80MS/s pipeline ADCs
- ADC pair utilize double-sampling and shares same front-end S/H circuit
- Resolution
  - Stage : 1.5 bits+ 2 bits (flash)
  - Number of stages : 8+1



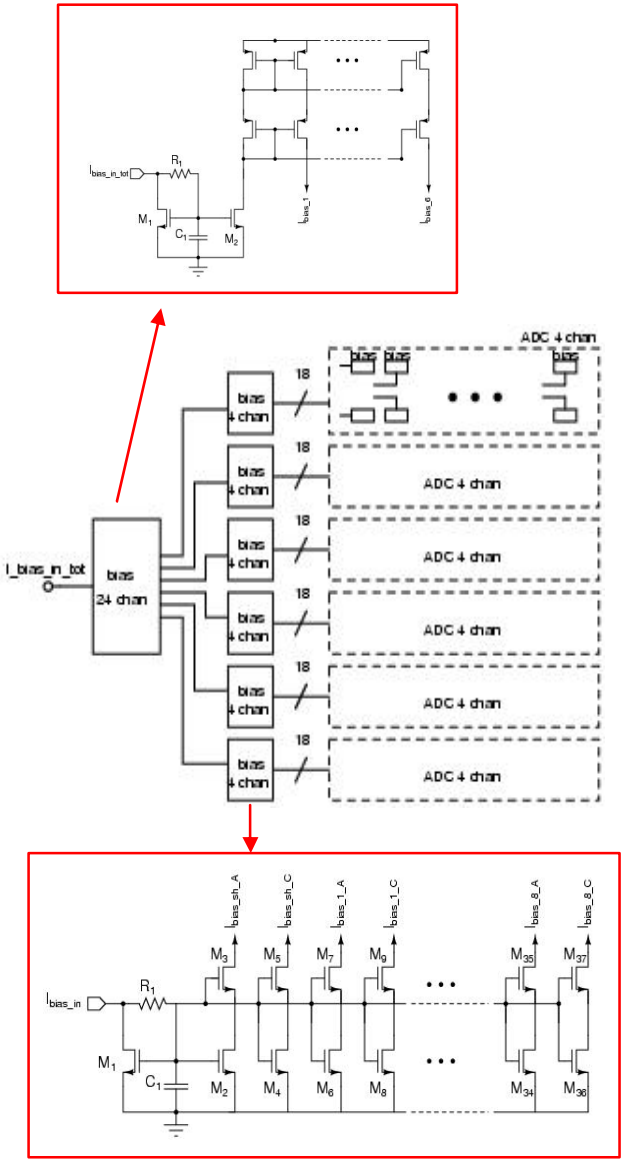
24-Channel ADC, #2

- Performance vs. power consumption
- Large die size causes problems
  - Parasitics (matching)
  - Power supply
  - Clock feedthrough



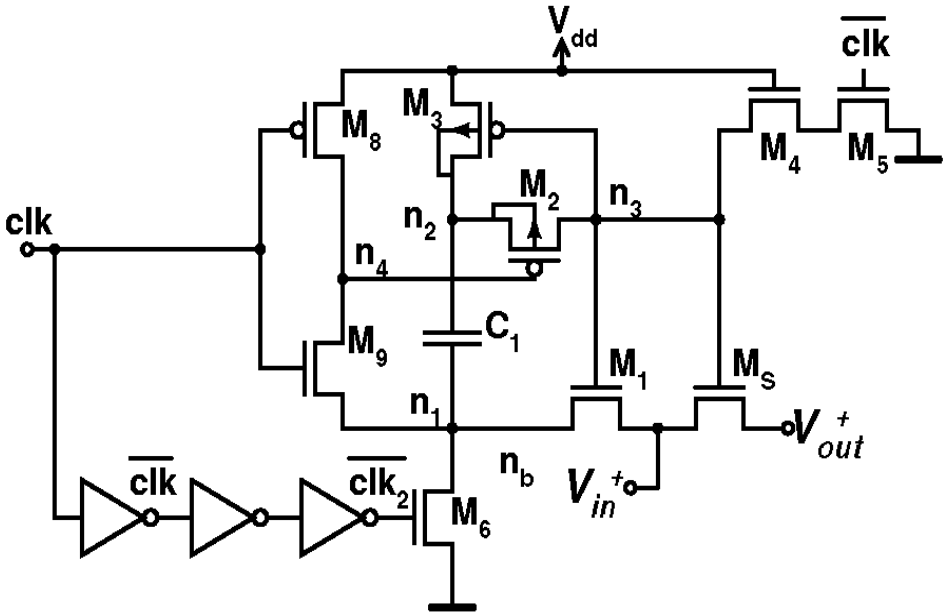
Biasing of ADC channels

- Bias circuit for each stage
- Local current mirrors for 4 channel ADCs
- Current mirrors for reference (input) current
- A single off-chip bias current
- Tolerance against parasitics from long distances



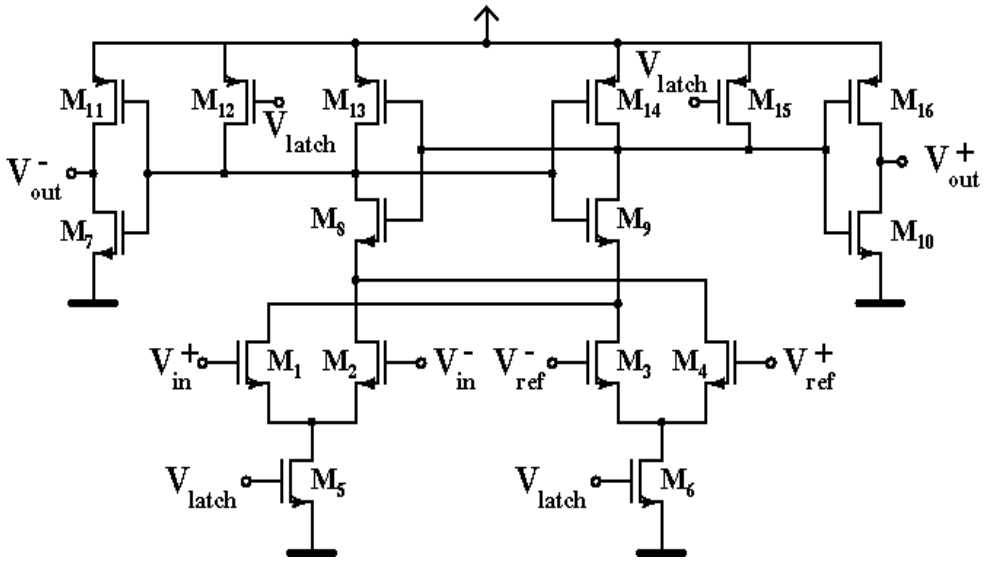
Bootstrapped Input S/H Switch

- Used in first stage as sampling switch
- Insensitive to input voltage amplitude variations
- Gate voltage of switch transistor is connected to follow the input voltage



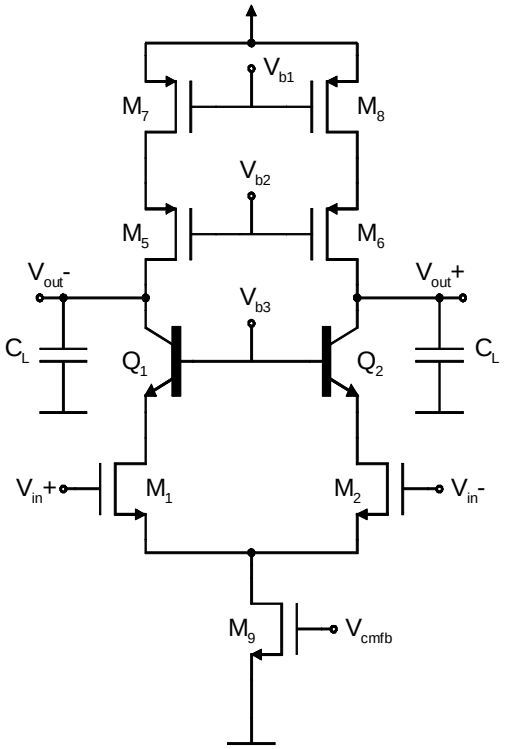
Differential pair comparator Input Switch

- A cross connected differential pairs generate a differential current
- Cross coupled inverters are used as latch
- The clock signal V_{latch} zeros the outputs every half of the clock cycle
- Benefits:
  - Fast operation & low power consumption



Operational amplifier

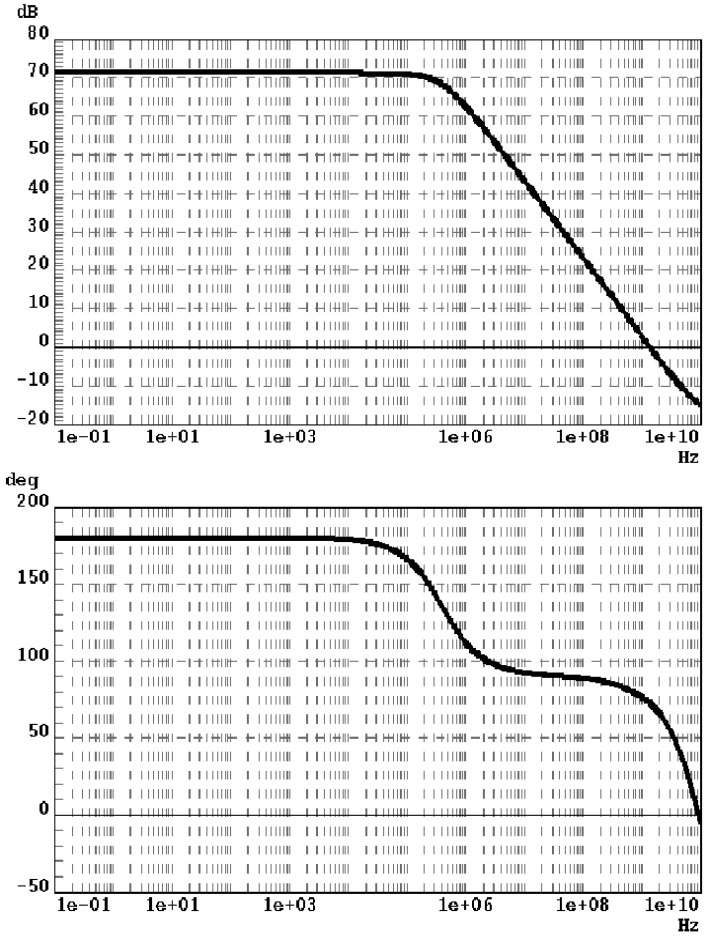
- BiCMOS telescopic OTA
- Relatively low current consumption
- The CMFB-loop is realised using standard SC-circuit
- NPN-transistors better vs. nMOS-transistors
  - Larger g_m & lower V_{sat}
- Swing is maximised by separating the common mode levels of the input and output
- Gain > 70 dB and high bandwidth can be achieved
- Slewing limited
  - determines power consumption by setting the minimum current



Operational amplifier, simulation results

- 1st stage OpAmp

PWR	6.6 mW
A_0	71 dB
GBW	1385 MHz
$V_{in,pp}$	0.5 V
PM	72.4°



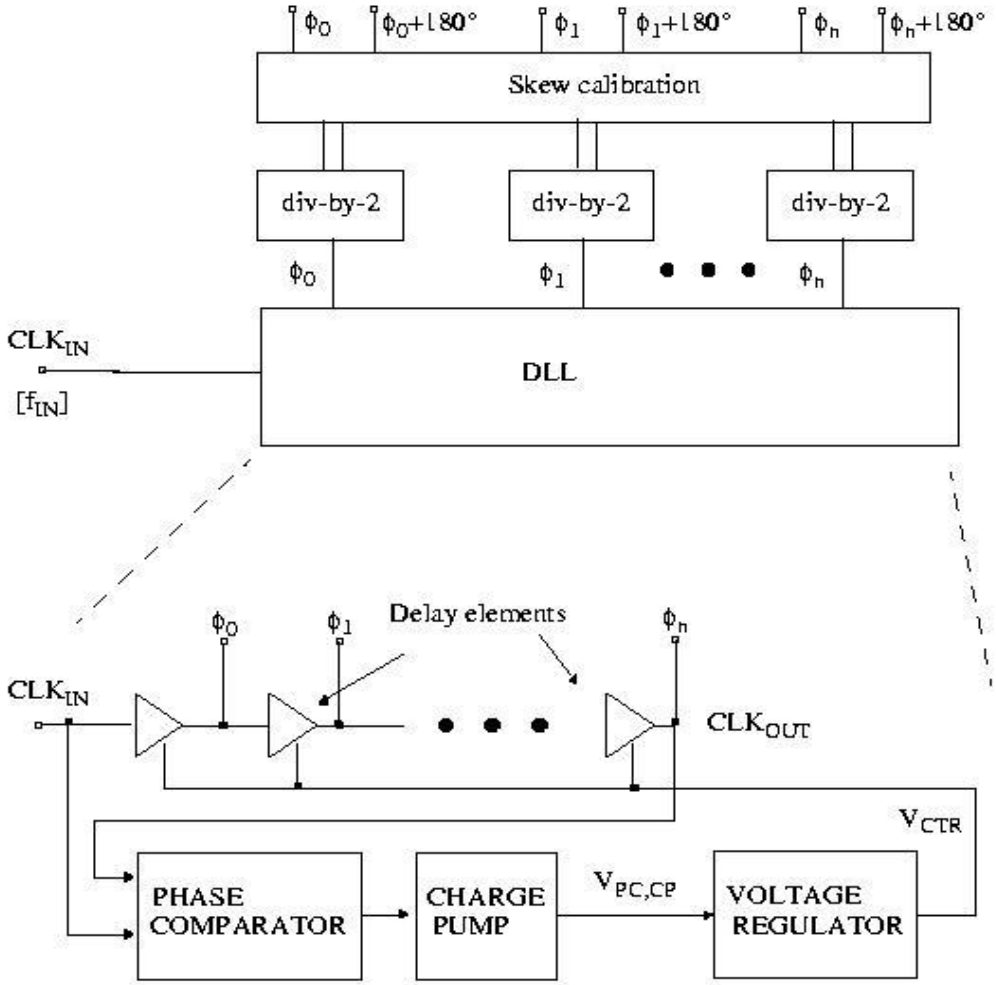
Clock generation for ADC

- 24 clock signals required
- A phase shift of 15 deg between signals
- High requirements for timing errors
  - Jitter
  - Skew
- DLL based clock generator
- Digital skew calibration for each phase

Clock generation for ADC, DLL

- A high performance external clock
  - Mtron, M650
  - 311 Mhz, Jitter below 0.5 ps

  (BW= 12 kHz -80 MHz)
- A DLL (delay locked loop)
  - 6 differential stages
  - Cross coupled inverters
  - div-by-2 circuits
- Digital skew calibration of each phase



Clock generation for ADC, skew calibration #1

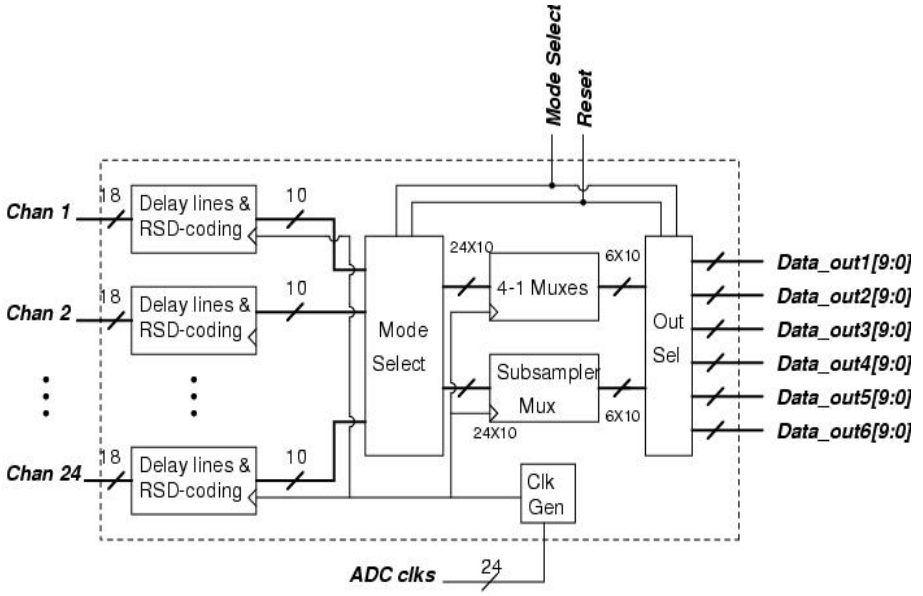
- Matching of delays between phases extremely critical
  - 0.5 ps timing accuacy required
- Delay between signals is affected by
  - Matching of active components
  - Asymmetry of parasitics (also power lines !!)
- A maximum symmetry was utilized for all components
  - Component/wiring size & orientation
  - Multiple power supply pads
  - Dummy components/wiring in all 'asymmetric' nodes

Clock generation for ADC, skew calibration #2

- Some skew elements can not be removed
  - Matching due to process tolerance
  - Asymmetric routing between DLL and ADC channels
- Delay verniers were designed for each phase signal
  - Tiny capacitors (10 fF) were coupled to signal metallization
  - Capacitive loading to signal line was altered with MOS-switch
- A 8-bit capacitance array to each line
- A resolution of 0.5 ps

Digital Domain, #1

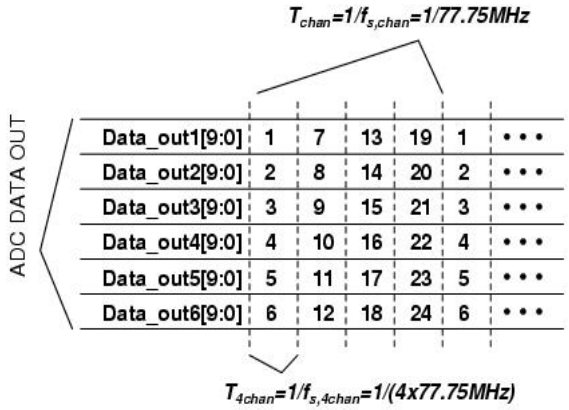
- Data synchronization
- RSD-coding
- Two alternative output modes
  - 4-to-1 muxes (@ 311MS/s)
  - Sub-sampling (@ 77MS/s)

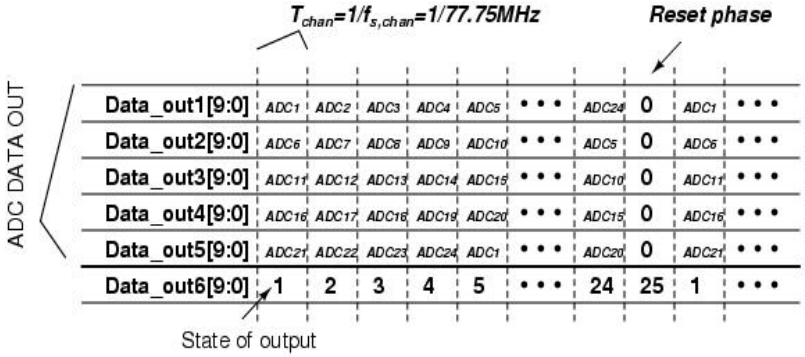


Digital Domain, #2

Output modes:

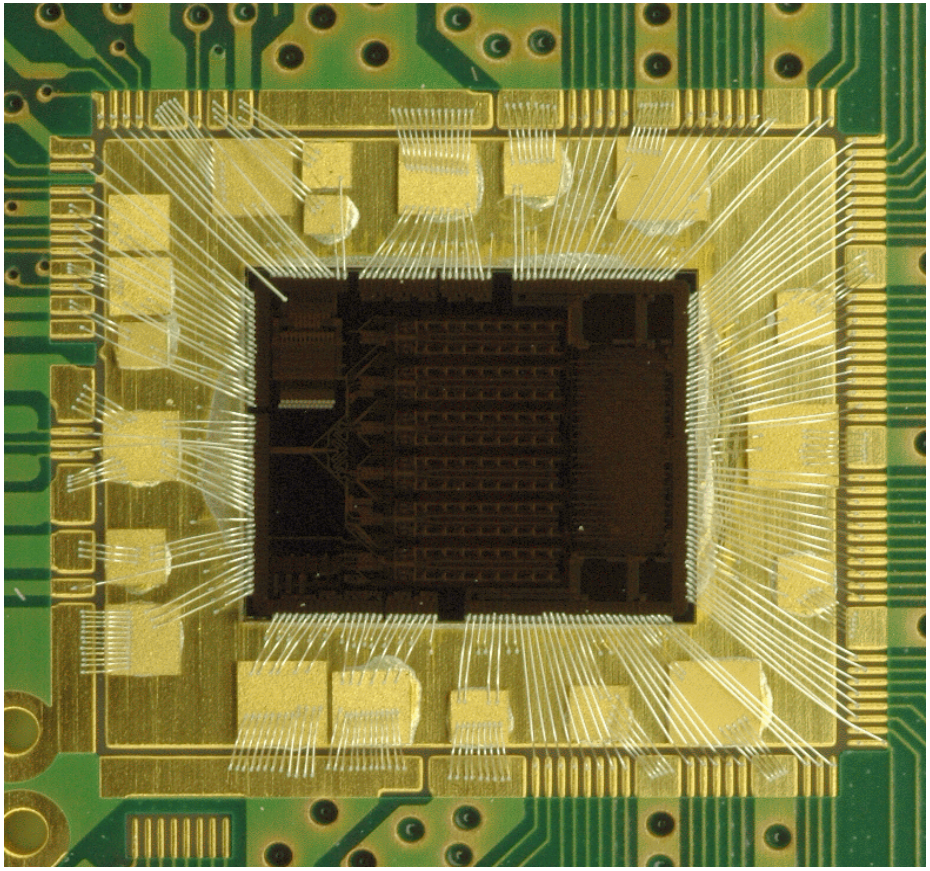
- High speed
  - 4-to-1 muxing
  - ~ 320 MS/s data rate
  - Sensitive to process variations, temperature
- Sub-sampling
  - Every 5th sample is driven to outputs





Experimental results, background

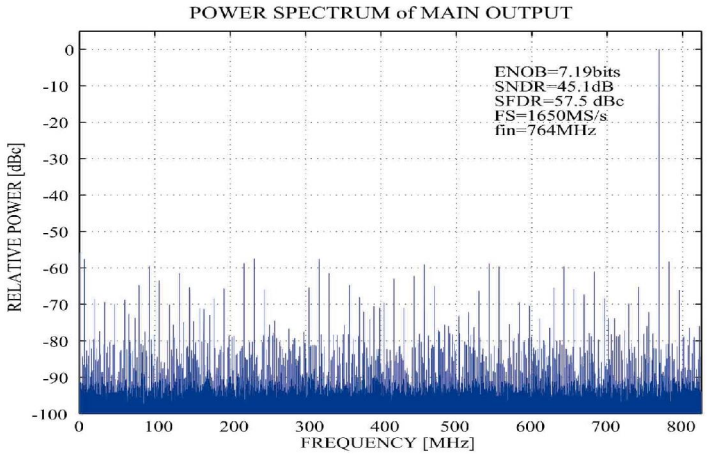
- A 0.35 µm SiGe BiCMOS technology (AMS)
  - BJT's were only utilized in OPAMP's
- Area 5.8 x 6.9 mm^2 ,
- 215.000, devices
- Wirebonded directly to PCB
  - 4 layer, fine pitch
  - Microcaps for decoupling supplies
  - A heat sink applied top of gloptop

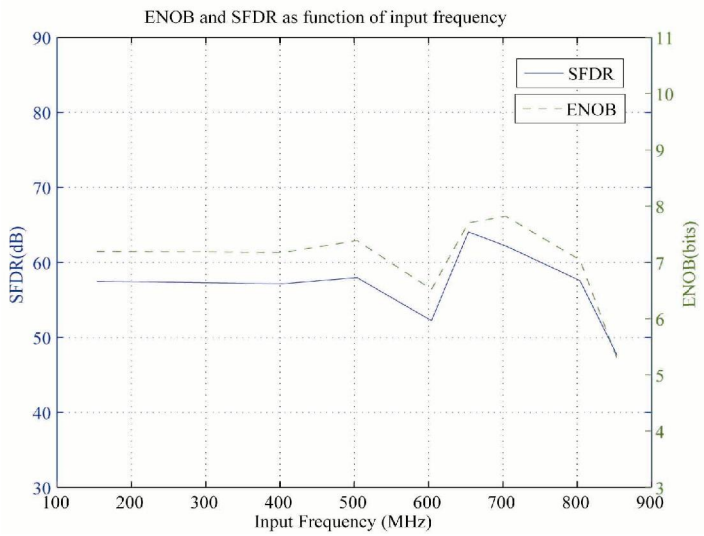


Experimental results, summary(1)

TABLE I. PERFORMANCE SUMMARY

Resolution	10 bits
Sample Rate	1.8GS/s
Power cons.	3.5W
SFDR	
@f_{in}=29.7MHz	66.2dB
@ f_{in}=764MHz	57.5dB
ENOB	
(@f_{in}=29.7MHz)	8.31 bits
(@f_{in}=764MHz)	7.19 bits
Technology	0.35-µm BiCMOS
Area	5.8x6.9 mm^2





Experimental results, summary (2)

- Power consumption 3.5…3.9 W
  - analog part 2.2…2.6 W (variation from chip to chip)
  - digital part 1.3…1.8 W
    - depends heavily on switching frequency of the data
    - main power eater: output pad buffers
  - the circuit at the limits of the process digital performance
- Calibration: manual
  - for a production version on-chip calibration circuit recommended

Experimental results, summary (3)

- Yield and Reliability
  - *the circuit is not radiation tested*
  - large chip ð limited yield?
  - high power ð high operating temperature
    - needs a heat sink
    - reduces performance in terms of SNR
    - increases gain errors
  - circuit at the speed limit of the process
    - variations and changes in the delays critical
  - parasitic capacitances limit the pipeline performance
    - and define the maximum reasonable analog power consumption
  - the process has only 4 metal layers
    - analog power supply lines non-symmetrical
    - non-optimum data or clock lines

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