Evaluation of a 10-bit 2.2 Gsps ADC for Space Applications

D. Bellin
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J. Bellefet (e2v)
C. Carmona (e2v)
F. Malou (CNES)
P. Ribeiro (TRAD)
Outline

- e2v grenoble presentation
- Overview of 10-bit 2.2 Gsps AT84AS008 ADC
- Architecture and Process
- Package description
- Space Evaluation with CNES
  - Electrical characterization
  - ESD tests
  - Package tests (mechanical, thermal and reflow)
  - Quality and reliability tests
- Radiation tests
  - Total dose tests
  - Heavy ions tests
- Radiation assessment of AT84CS001 DEMUX (companion chip)
  - Total dose tests
  - SEL tests
- Conclusion
1- Overview of e2v Grenoble

- Atmel Grenoble became **e2v grenoble starting** August 1st, 2006
  - Atmel motivation: to focus on its core technologies
  - e2v motivation:
    - very good strategic fit
    - will allow to extend markets with broader range of products

- In-house skills cover all aspects of:
  - Design
  - Electrical characterization
  - Package design / thermal modelling
  - Assembly
  - Test
  - Burn-in
  - All tasks required by space level production
2- Overview of 10-bit 2.2 Gsps AT84AS008 ADC

- 10-bit 2.2 Gsps ADC
  - 8 bit ENOB at 1.7 Gsps in 1st Nyquist
  - 7.7 bit ENOB at 2.2 Gsps in 1st Nyquist
  - SFDR = $-54$ dBc / SNR = 50 dB at 2.2 Gsps
  - 3.3 GHz input bandwidth
    ⇒ performances are flat over the full 1st Nyquist zone.
  - Same features than previous TS83102G0B 10-bit 2 Gsps ADC:
    → AT84AS008 is fully pin-to-pin compatible with TS83102G0B ADC
    → Performance improvements are significant
      ✓ better SNR and ENOB performances above $\text{Fin} = 1$ GHz
      ✓ flatter spectrally ‘pure’ FFT response throughout 1st and 2nd Nyquist.
3- Architecture of AT84AS008 ADC

- Track/Hold
- Analog quantizer (folding & interpolation)
- Regeneration of analog residues into logical levels
- Synchronization stage before output buffers
- Fully differential architecture
4- Process of AT84AS008 ADC

- AT84AS008 is designed on a SiGe process
  - INFINEON process (Germany)
  - 75 GHz cut-off frequency
  - High voltage NPN bipolar transistors
  - 3 layers AlCu metallization
  - Only vertical transistors and poly resistors to be rad tolerant
  - Insulation concept: LOCOS and deep trench
5- Package description (1/4)

- High Reliability Hermetic Ceramic cavity down package (CI-CGA152)
- Solder Column Interposer (SCI) for good resistance to temperature cycling
- Column finish is Sn10Pb90
- Good thermal dissipation by columns
The die is directly attached to the CuW heatspreader.
5- Package description (3/4)

Thermal simulation results of $R_{th}$ from junction to bottom of columns

$$R_{th,j-bottom of columns} = 7.4^\circ C/W$$

Hypothesis used for ANSYS simulations:
- Body 21 x 21 mm 1.55 mm thick glue 0.050 mm
- Die 3.8 x 3.8 mm$^2$ 380 um thick heating zone: 1.9 x 1.9 mm$^2$ 1 watt
- Infinite heatsink at bottom of columns
- No external heatsink on top.
5- Package description (4/4)

Simplified thermal network of CI-CGA152 package

Typical values, with assumption of uniform power dissipation over 25% of die top surface.

Assumptions:
- Die 3.75x3.84=14.4 mm²
- 50 µm thick Epoxy/Ag glue
- Pb90Sn10 columns diameter 0.86 mm, 2.1 mm length under bottom of LGA, 21x21 mm CLGA, 18.5x18.5 mm CuW on top

Silicon Junction

0.80 °C/Watt

Epoxy/Ag glue

3.0 °C/Watt

CuW heatspreader

0.25 °C/Watt

CuW heatspreader

0.6 °C/Watt

Ceramic package

0.56 °C/Watt

Ceramic columns PbSn

0.205 °C/Watt

Bottom of 44 internal columns

0.6 °C/Watt

Bottom of 52 between columns

0.25 °C/Watt

To external heatsink if any

1.7 °C/Watt

Bottom of 56 external columns

0.5 °C/Watt

Infinite heatsink at bottom of columns

0.25 °C/Watt

Silicon Junction

Case were all Bottom of Columns are connected to infinite heatsink at bottom and no external heatsink on top:

Reduction

(Result using SPICE, thermal to electrical equivalent model)

Infinite heatsink at bottom of columns

7.4 °C/Watt

Silicon Junction

7.4 °C/Watt

To external heatsink if any

0.25 °C/Watt

0.5 °C/Watt

0.25 °C/Watt

0.25 °C/Watt

0.80 °C/Watt

0.56 °C/Watt

0.47 °C/Watt

0.44 °C/Watt

2.61 °C/Watt

2.22 °C/Watt

2.04 °C/Watt

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6- Space Evaluation with CNES

- Evaluation according to ESCC no 226900 with CNES support.
- Parts were manufactured and screened according to ESCC no 9000 chart F3
- Complete evaluation test program to demonstrate the high reliability of the ADC for space applications
  - Electrical characterization
  - ESD tests
  - Package tests (mechanical, thermal tests and reflow simulation)
  - Quality (construction analysis) and reliability tests (life test)
  - Radiation assessment (refer to chap. 7)
6- Space Evaluation with CNES

Electrical characterization (1/2)

- Electrical characterization at full speed (2.2 Gsps, \(\text{Fin} = 1.098\text{GHz} \ @ -1\text{dBFS}\))
  - measurement on 5 socketed parts
  - over power supply range
  - over military temperature range
    (\(\text{Tcase} = -55\text{°C} \text{ to } Tj = 125\text{°C}\))
  - Static parameters :
    - Power consumption
    - \(\text{VOL}/\text{VOH}\)
    - \(\text{INL} / \text{DNL}\)
  - Dynamic parameters (FFT)
    - \(\text{SFDR, SINAD, ENOB, SNR and THD}\)
6- Space Evaluation with CNES

*Electrical characterization & ESD tests*

- **Electrical characterization**
  - FFT @2.2Gsps / 1098MHz –1dBFS (ambient – Vnom)
  - H1 Fundamental (Fin = 1098 MHz)
  - Fs = 2.2 Gsps
  - SFDR (H3)

- **ESD tests**
  - On 10 devices according to MIL STD 883 TM 3015
  - All parts successfully passed 750 Volts stress
  - Device is compliant to ESD class 1
Objective: find out the package robustness
  ⇒ tests were pushed beyond ESCC no 226900 in term of number of cycles

Mechanical tests
  • On 4 devices
    • 50 mechanical shocks cycles according to MIL-STD 883 TM 2002 cond. B
    • 120 vibrations cycles according to MIL-STD 883 TM 2007 Cond. A

Thermal tests
  • On 4 devices
    • Temperature cycling : 500 cycles A/A according to MIL-STD 883 TM 1010 cond. C
    • Thermal shock : 100 cycles L/L according to MIL-STD 883 TM 1011 cond. C

Reflow simulation (according to conditions Sn/Pb eutectic assembly)
  • On 2 devices
    • 5 reflow cycles according to J-STD-020C (peak 225°C)

Conclusion of package tests: no electrical drift neither package damage
It confirms the package robustness
Reliability test:
- 3000 hours endurance Life test at $T_j = 125^\circ$C
- On 20 devices running at 625 Ksps with maximum power supplies

- No electrical drift neither functional failure after 3000 hours
- It demonstrates SiGe process high reliability
6- Space Evaluation with CNES

Quality tests

- SEM analysis of die
  - Bipolar transistors

All metal layers with CMP planarisation

Deep trench
6- Space Evaluation with CNES

**Quality tests**
- Back end construction analysis

Good coplanarity of columns
7- Radiation Tests

*Total dose test of AT84AS008 ADC*

- **Total dose tests**
  - Tests on 10 ADC AT84AS008 (6 parts ON / 4 parts OFF)
  - 2 reference parts
  - Low dose test (50 rad/hr)
  - Co$_{60}$ source of the ONERA DESP (Toulouse – France)
  - Test up to 150 Krad with intermediate measurements at 10, 25, 50 and 100 Krad(Si)
  - 24 hours annealing at ambient and 168 hrs annealing at 100°C
  - Tests performed by TRAD (Toulouse – France)
7- Radiation Tests

Total dose test of AT84AS008 ADC

Parameters monitored

<table>
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<tr>
<th>PARAMETERS</th>
<th>SYMBOLS</th>
<th>TEST CONDITIONS (TA = 25°C)</th>
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<td>V_{diff_{d9}}, V_{diff_{d7}}</td>
<td>V_{diff} = VOH - VOL</td>
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<tr>
<td>Common Mode Output Voltage for D9 &amp; D7</td>
<td>CM_{d9}, CM_{d7}</td>
<td>CM = (VOH + VOL)/2</td>
</tr>
<tr>
<td>Ivcc Supply current</td>
<td>Ivcc</td>
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</tr>
<tr>
<td>Ivplusd Supply current</td>
<td>Ivplusd</td>
<td></td>
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<tr>
<td>Ivey Supply current</td>
<td>Ivey</td>
<td></td>
</tr>
<tr>
<td>Idvee Supply Current</td>
<td>Idvee</td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td>P</td>
<td>P = Ivcc<em>5 + Ivey</em>5 + IIdvee<em>2.2 + Iplusd</em>1.45</td>
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<tr>
<td>Leakage current for VIN input</td>
<td>Ibias_{vin}+</td>
<td>Vin = 0V</td>
</tr>
<tr>
<td>Leakage current for VIN input</td>
<td>Ibias_{vin}-</td>
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<td>INL_{rms}</td>
<td>Vin = full scale (saturation)</td>
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</table>
7- Radiation Tests

Total dose test of AT84AS008 ADC

- Some test results versus TiD and annealing (1/3)
  - Power dissipation

![Power dissipation graph]

Max = 4.8
7- Radiation Tests
Total dose test of AT84AS008 ADC

Some test results versus TiD and annealing (2/3)

Swing on output bit 9 (MSB)

Common mode on bit 9 (MSB)
7- Radiation Tests

Total dose test of AT84AS008 ADC

- Some test results versus TiD and annealing (3/3)

INL max

SFDR
7- Radiation Tests

Total dose test of AT84AS008 ADC

- Conclusion on total dose tests
  - Currents, voltages and dynamic performances are preserved at least at 150 Krad(Si)
  - AT84AS008 ADC can be considered as not sensitive to cumulated total dose of at least 150 Krad (Si)

- Good Results can be explained by the following design rules used:
  - Fully bipolar process with only vertical insulated transistors:
    -> no lateral active components
    -> no PNP transistors
    -> it avoids leakage between the different transistors
  - Only oxyde insulated polysilicon resistors (ie. no diffused resistors whose doping may be modified by radiations)
  - Strictly fully differential architectures which allows good rejection of common mode effects drift
7- Radiation Tests
Heavy ions tests

- AT84AS008 Heavy ions tests
  - Tests performed on 2 parts soldered on evaluation boards (with a hole to provide direct access to the die)
  - Tests at UCL (Belgium)
  - By TRAD company (Toulouse – France)

- Irradiation cocktail used
  - Fluency up to $10^6$ ions/cm$^2$ for SEU
  - Fluency of $10^7$ ions/cm$^2$ for SEL detection

<table>
<thead>
<tr>
<th>Ion</th>
<th>Energy (MeV)</th>
<th>Range (µm)</th>
<th>LET ((MeV.cm$^2$)/mg)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$^{49}$Xe</td>
<td>459</td>
<td>43</td>
<td>55.9</td>
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<tr>
<td>$^{84}$Kr</td>
<td>316</td>
<td>43</td>
<td>34.0</td>
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<td>$^{150}$Ar</td>
<td>150</td>
<td>42</td>
<td>14.1</td>
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<tr>
<td>$^{78}$Ne</td>
<td>78</td>
<td>45</td>
<td>5.9</td>
</tr>
<tr>
<td>$^{62}$N</td>
<td>62</td>
<td>64</td>
<td>2.97</td>
</tr>
</tbody>
</table>

Cocktail 1
7- Radiation Tests

Heavy ions tests

- Test procedure
  - An acquisition board is connected to a Computer
  - Events are detected in comparing DUT outputs to a reference ADC
  - It counts the number of successive wrong conversions
    - 1 wrong conversion = SEU
    - successive wrong conversions
      - long Single Event Upset (SEU)
      - or Single Event Functional Interrupt (SEFI) if it does not recover
  - Test is performed at 100 Msp
  - Detection of Single Event Latchup (SEL)
7- Radiation Tests

Heavy ions tests

- SEL test results
  - No SEL at a LET of 55.9 MeV cm$^2$/mg with a fluence of 9.00 E6 particles/cm$^2$
  - AT84AS008 ADC is therefore immune to SEL

- SEU test results
  - SEU were monitored for 2 output codes:
    - 000
    - 3FF
  - Same results for the 2 codes
  - No SEFI was detected
  - Only SEU and long SEU with a maximum of 15 successive wrong conversion errors at a LET of 55.9 MeV cm$^2$/mg
7- Radiation Tests

Heavy ions tests

- Calculation Rate

  - Results were computed using OMERE 3.0 free software developed by TRAD:
    “OMERE 2.0: A TOOLKIT FOR SPACE ENVIRONMENT”, P. F. Peyrard, T. Beutier et al., RADECS 2003, Noordwijk, Hollande”.

  - LET threshold = 1.49 MeV.cm².mg⁻¹
  - Saturation cross section is 1.29E-4 cm²

<table>
<thead>
<tr>
<th>Project</th>
<th>Altitude Km</th>
<th>Inclination deg</th>
<th>CREME 86 m =</th>
<th>SEU/Cell.day</th>
<th>SEU/Device.day</th>
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<tbody>
<tr>
<td>Geostationary</td>
<td>35870</td>
<td>0</td>
<td>3</td>
<td>3.42E-4</td>
<td>3.42E-3</td>
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<td>SPOT</td>
<td>852</td>
<td>98</td>
<td>3</td>
<td>1.108E-4</td>
<td>1.108E-3</td>
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<td>LEO-1</td>
<td>600</td>
<td>98</td>
<td>3</td>
<td>1.036E-4</td>
<td>1.036E-3</td>
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<tr>
<td>LEO-2</td>
<td>1000</td>
<td>53</td>
<td>3</td>
<td>4.98E-5</td>
<td>4.98E-4</td>
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<tr>
<td>Inmarsat-P</td>
<td>10300</td>
<td>45</td>
<td>3</td>
<td>1.962E-4</td>
<td>1.962E-3</td>
</tr>
</tbody>
</table>
8- Radiation Tests on DEMUX AT84CS001

- DEMUX AT84CS001
  - Companion chip of ADC AT84AS008
  - 10-bit 2.2 Gsps 1:4 DEMUX
  - Si BiCMOS process (Ft=25GHz) but only bipolar transistor are used
  - EBGA240 package (industrial temperature range)
  - In the frame of ADC evaluation, it was decided to evaluate the radiation behavior of this DEMUX (that could be introduced in a spatial version with hermetic package)
8- Radiation Tests on DEMUX AT84CS001

Total dose test

➢ Total dose tests

➢ Tests on 10 DEMUX AT84CS001 (6 parts ON / 4 parts OFF)
➢ 1 reference part
➢ Low dose test (50 rad/hr)
➢ Co^{60} source of the ONERA DESP (Toulouse – France)
➢ Test up to 150 Krad with intermediate measurements at 10, 25, 50 and 100 Krad(Si)
➢ 24 hours annealing at ambient and 168 hrs annealing at 100°C
➢ Tests performed by TRAD (Toulouse – France)

➢ Intermediate measurements were performed using a AT84AS008 ADC driving the DEMUX at 2 Gsps
Parameters monitored

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<tr>
<td>Ivplusd Supply current</td>
<td>Ivplusd</td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td>P</td>
<td>P = Ivcc<em>3.3+Iplusd</em>2.5</td>
</tr>
<tr>
<td>Leakage current for I₀ and I₉ inputs</td>
<td>I₀, I₀b, I₉, I₉b</td>
<td>Vin = 0V</td>
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(1) Measurements were performed on each port (A, B, C and D).
8- Radiation Tests on DEMUX AT84CS001

Total dose test

- Some test results versus TiD and annealing

  - ENOB on port A

  ![Graph showing ENOB on port A versus dose and annealing temperature](image)

- Conclusion
  - DEMUX AT84CS001 is not affected by a total dose of at least 150 Krad (Si)

  ![Graph showing SFDR on port A versus dose and annealing temperature](image)
Single Event Latchup test

- To confirm it is SEL immune. (BiCMOS process, but only bipolar transistor are used)
- Tests performed on 2 delidded parts at UCL (Belgium)
- Tests performed by TRAD company (Toulouse – France)

- The test principle is the same than for AT84AS008 ADC

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<th>Range (μm Si)</th>
<th>LET (MeV.cm².mg⁻¹)</th>
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<td>43</td>
<td>55.9</td>
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<td>⁸³Kr²⁺</td>
<td>756</td>
<td>92</td>
<td>32.4</td>
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</table>

- Conclusion:
  - No SEL was detected for these two ions.
  - The AT84CS001 is Latchup free at a LET of 55.9 MeV.cm².mg⁻¹
Conclusion

- AT84AS008 ADC **successfully passed the CNES space evaluation** in terms of:
  - radiation tolerance
  - reliability
  - quality and assembly process

- The innovative architecture leads to **unprecedented dynamic performance** at a sampling rate of **2.2 GHz** and over the full military temperature range

- These **performances are preserved** with a total dose of at least **150 Krad (Si)**

- This confirms e2v position as a European partner for **high-speed data converters in space applications.**